Not Recommended for New Designs

This product was manufactured for Maxim by an outside wafer foundry using a process that is no longer available. It is not recommended for new designs. The data sheet remains available for existing users.

A Maxim replacement or an industry second-source may be available. Please see the QuickView data sheet for this part or contact technical support for assistance.

For further information, contact Maxim's Applications Tech Support.

19-4701; Rev 1; 7/95

High-Speed Video Multiplexer/Amplifier

MAX440/MAX441

General Description

The MAX440 and MAX441 combine a unity-gain stable, wideband video amplifier with a high-speed, 8- or 4-channel multiplexer (mux). The mux's fast 15ns switching time and the amplifier's low differential gain and phase errors (0.04% and 0.03°, respectively) make the MAX440/MAX441 ideal for broadcast-quality video applications. Both devices operate from ±5V power supplies and typically consume only 350mW.

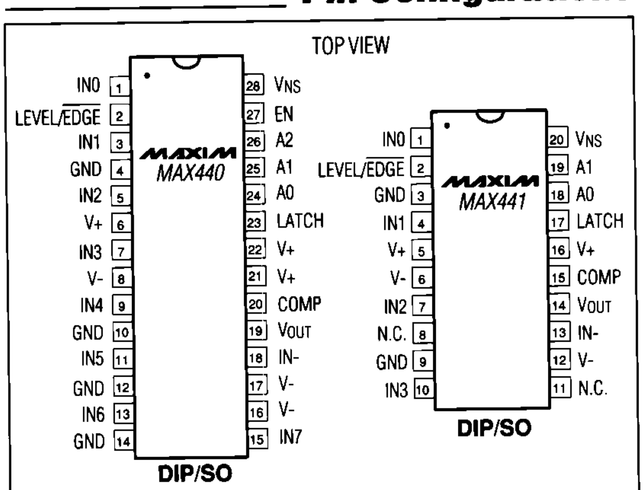
The on-board video amplifier features a 160MHz unity-gain bandwidth, 250V/µs slew rate, and directly drives a 150Ω load to ±3V. Pin-selectable frequency compensation allows the amplifier's AC response to be optimized without external compensation components or complex calculations. Slew rates of 370V/µs are obtainable for applications with a closed-loop gain of 6dB or greater. An enable control on the MAX440 places the amplifier output into a high-impedance state, allowing multiple devices to be paralleled to form larger switch matrices.

The mux's low channel-input capacitance (4pF with channel on or off) maximizes high-speed performance. No input channels are located on adjacent package pins, minimizing crosstalk and simplifying board layout.

Applications

- Video Signal Multiplexing
- Video Crosspoint Switches
- Coaxial-Cable Drivers
- Video Editing
- Video Security Systems
- Medical Imaging
- High-Speed Signal Processing

Pin Configurations



Features

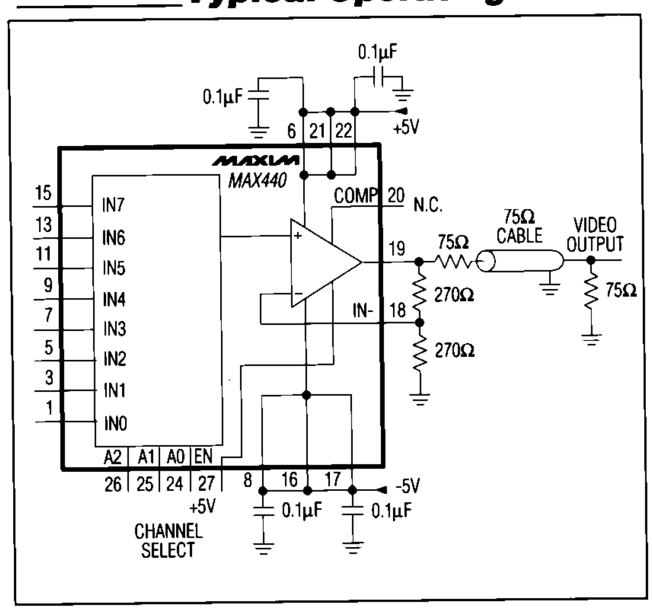
- ♦ 160MHz Unity Gain Bandwidth
- ♦ 110MHz Bandwidth (Av = 6dB)
- ♦ 0.03°/0.04% Differential Phase/Gain Error
- ♦ 15ns Channel Switch Time
- ♦ 370V/µs Slew Rate
- ♦ Directly Drives 50Ω Cables
- ♦ 4pF On/Off Input Capacitance
- ♦ No External Compensation Components
- ♦ Pin-Selectable Frequency Compensation
- ♦ Expandable for Larger Switch Matrices

Ordering Information

PART	TEMP. RANGE	PIN-PACKAGE
MAX440CPI	0°C to +70°C	28 Plastic DIP
MAX440CWI	0°C to +70°C	28 Wide SO
MAX440C/D	0°C to +70°C	Dice*
MAX440EPI	-40°C to +85°C	28 Plastic DIP
MAX440EWI	-40°C to +85°C	28 Wide SO
MAX440MDI	-55°C to +125°C	28 Ceramic SB**
MAX441CPP	0°C to +70°C	20 Plastic DIP
MAX441CWP	0°C to +70°C	20 Wide SO
MAX441EPP	-40°C to +85°C	20 Plastic DIP
MAX441EWP	-40°C to +85°C	20 Wide SO

** Dice are specified at +25°C, DC parameters.*
***Contact factory for availability and processing to MIL-STD-883.*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

Supply Voltage (V+ to V-) 12V
Analog Input Voltage .... (V+ + 0.3V) to (V- - 0.3V)
Digital Input Voltage .... -0.3V to (V+ + 0.3V)
Short-Circuit Current Duration .... 1 minute
Input Current to Any Pin, Power On or Off .... ±50mA
Continuous Power Dissipation (T_A = +70°C)
20-Pin Plastic DIP (derate 8.00mW/°C above +70°C) ... 640mW
20-Pin Wide SO (derate 10.00mW/°C above +70°C) ... 800mW
28-Pin Plastic DIP (derate 9.09mW/°C above +70°C) ... 727mW
28-Pin Wide SO (derate 12.50mW/°C above +70°C) ... 1000mW
28-Pin Ceramic SB (derate 16.67mW/°C above +70°C) . 1333mW

Operating Temperature Ranges:
MAX44_C__ .... 0°C to +70°C
MAX44_E__ .... -40°C to +85°C
MAX440MDI .... -55°C to +125°C
Storage Temperature Range .... -65°C to +150°C
Lead Temperature (soldering, 10 sec) .... +300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

($V+$ = 5V, $V-$ = -5V, V_{NS} = -5V, R_L = 150Ω, T_A = +25°C, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DC PERFORMANCE							
Input Voltage Range	V_{IN}	$T_A = T_{MIN}$ to T_{MAX}		-2		2	V
Input Offset Voltage (All Channels)	V_{OS}	T_A = +25°C			±2.5	±10	mV
		0°C to +70°C				±10	
		-40°C to +85°C				±15	
		-55°C to +125°C				±20	
Input Bias Current (Channel On)	I_B	V_{IN} = 0V	T_A = +25°C		±1	±2	µA
			0°C to +70°C			±5	
			-40°C to +85°C			±5	
			-55°C to +125°C			±20	
Input Leakage Current (Channel Off)	I_{LKG}	V_{IN} = 0V	T_A = +25°C		±0.5	±50	nA
			$T_A = T_{MIN}$ to T_{MAX}			±1	µA
Input Resistance (Channel On)	R_{IN}	$-2V \le V_{CM} \le 2V$	T_A = +25°C	0.5	2		MΩ
			$T_A = T_{MIN}$ to T_{MAX}	0.2			
Input Capacitance	C_{IN}	Channel on or off			4		pF
DC Output Resistance	R_{OUT}	A_V = 0dB			25		mΩ
Disabled Output Resistance	R_{OUTdis}	MAX440 only, EN = 0V			130		kΩ
Disabled Output Capacitance	C_{OUTdis}	MAX440 only, EN = 0V			15		pF
Open-Loop Voltage Gain	A_{VOL}	R_L = 75Ω, $-2V \le V_{OUT} \le +2V$	T_A = +25°C	50	60		dB
			$T_A = T_{MIN}$ to T_{MAX}	46			
Common-Mode Rejection Ratio	CMRR	$-2V \le V_{IN} \le +2V$	T_A = +25°C	46	50		dB
			$T_A = T_{MIN}$ to T_{MAX}	40			
Power-Supply Rejection Ratio	PSRR	±4.75V to ±5.25V	T_A = +25°C	54	80		dB
			$T_A = T_{MIN}$ to T_{MAX}	54			
Output Voltage Swing	V_{OUT}	T_A = +25°C		±3			V
		$T_A = T_{MIN}$ to T_{MAX}		±2			

ELECTRICAL CHARACTERISTICS (continued)

($V+ = 5V$, $V- = -5V$, $V_{NS} = -5V$, $R_L = 150\Omega$, $T_A = +25°C$, unless otherwise noted.)

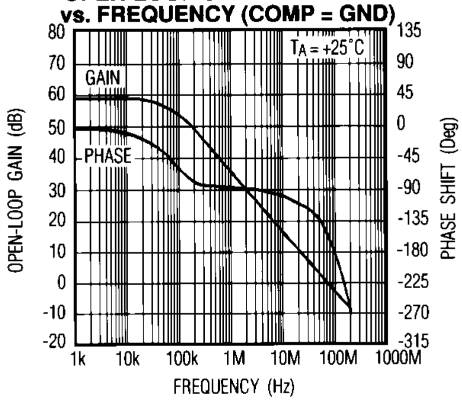
PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
DYNAMIC PERFORMANCE							
-3dB Bandwidth	BW1	A_V = 0dB, COMP = GND, $R_L = 75\Omega$			160		MHz
	BW2	A_V = 6dB, COMP = OPEN, $R_L = 150\Omega$			110		
Slew Rate	SR1	A_V = 0dB, COMP = GND, $R_L = 75\Omega$			250		V/µs
	SR2	A_V = 6dB, COMP = OPEN, $R_L = 150\Omega$			370		
Differential Phase Error (Note 1)	DP	V_{NS} = -2.5V to -5V, COMP = OPEN, A_V = 6dB, $R_L = 150\Omega$			0.03		deg
Differential Gain Error (Note 1)	DG	V_{NS} = -2.5V to -5V, COMP = OPEN, A_V = 6dB, $R_L = 150\Omega$			0.04		%
Settling Time	t_s	To 0.1% of final value, A_V = 6dB, COMP = OPEN, 1V step input			65		ns
Adjacent Channel Crosstalk (Note 2)	X_{TALK}	f = 10MHz, $R_S = 75\Omega$, A_V = 0dB	MAX440		-66		dB
			MAX441		-70		
Non-Adjacent Channel Crosstalk (Note 2)	X_{TALK}	f = 10MHz, $R_S = 75\Omega$, A_V = 0dB			-77		dB
Feedthrough with Amplifier Disabled (Note 2)	FT	MAX440 only, f = 10MHz, A_V = 0dB	CH0 -CH6 driven		-71		dB
			CH0 -CH7 driven		-63		
Input Noise-Voltage Density	e_n	f = 10kHz			12		nV/√Hz
POWER-SUPPLY REQUIREMENTS							
Operating Supply-Voltage Range	V_S			±4.75		±5.25	V
Positve Supply Current	I_{CC}	V_{IN} = 0V	$T_A = +25°C$	33	40	50	mA
			0°C to +70°C	30		52	
			-40°C to +85°C	27		54	
			-55°C to +125°C	27		54	
Negative Supply Current	I_{EE}	V_{IN} = 0V	$T_A = +25°C$	24	30	40	mA
			0°C to +70°C	20		42	
			-40°C to +85°C	17		44	
			-55°C to +125°C	17		44	
SWITCHING CHARACTERISTICS (see Figure 10)							
Logic Low Threshold	V_{IL}	$T_A = T_{MIN}$ to T_{MAX}				0.8	V
Logic High Threshold	V_{IH}	$T_A = T_{MIN}$ to T_{MAX}		2.4			V
Address Setup Time (Note 3)	t_{AS}					10	ns
Address Hold Time (Note 3)	t_{AH}					10	ns
Address Propagation Delay	t_{APD}				20		ns
Latch Propagation Delay	t_{LPD}				20		ns
Channel Switching Time (Note 4)	t_{SW}	V_{NS} = -2.5V			15		ns
		V_{NS} = -5V			25		ns
Enable Propagation Delay	t_{ENPD}	MAX440 only			15		ns
Output Disable Time	t_{DA}	MAX440 only			10		ns
Output Enable Time	t_{EN}	MAX440 only			40		ns
Switching Transient (Note 5)		$R_L = 75\Omega$	V_{NS} = -2.5V		100		mV_{p-p}
			V_{NS} = -5V		800		

Note 1: Input test signal: 3.58MHz sine wave of amplitude 40IRE superimposed on a linear ramp (0IRE to 100IRE). IRE is a unit of video signal amplitude developed by the International Radio Engineers. 140IRE = 1.0V.
Note 2: See Figure 9, *Dynamic Test Circuits.*
Note 3: Guaranteed by design.
Note 4: Channel switching time specified for switching between 2 grounded input channels; does not include signal rise/fall times for switching between channels with different input voltages.
Note 5: Measured while switching between 2 grounded channels.

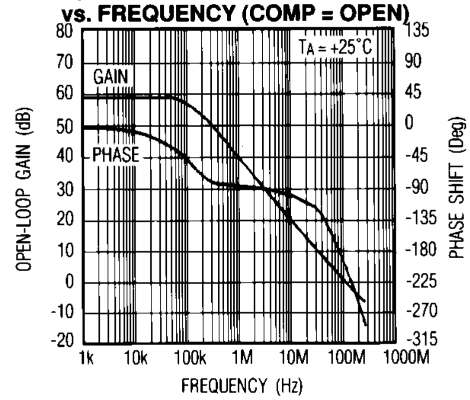
High-Speed Video Multiplexer/Amplifier

Typical Operating Characteristics

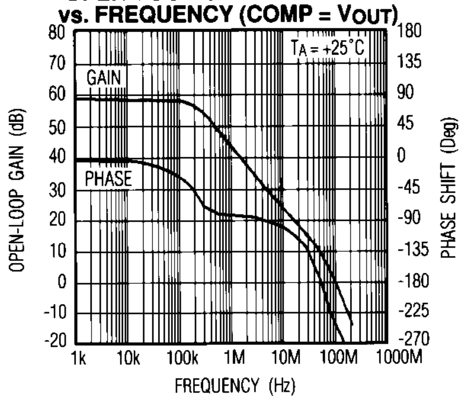
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMP = GND)



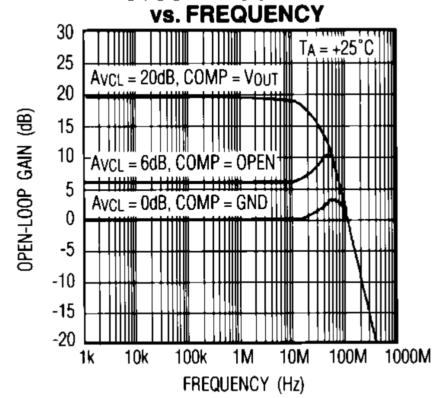
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMP = OPEN)



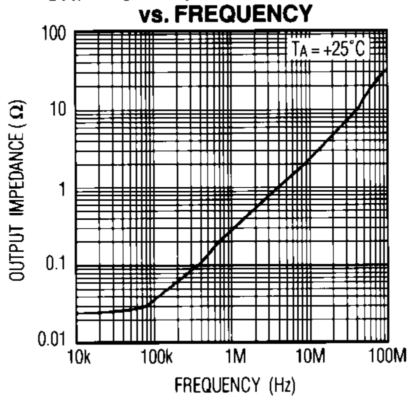
OPEN-LOOP GAIN AND PHASE vs. FREQUENCY (COMP = VOUT)



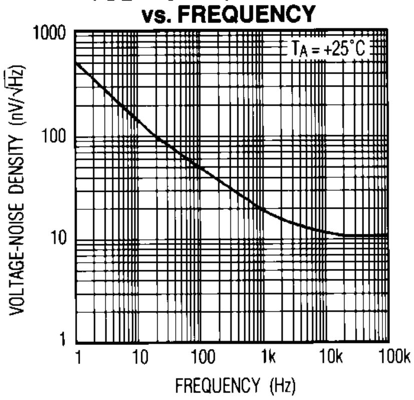
CLOSED-LOOP GAIN vs. FREQUENCY



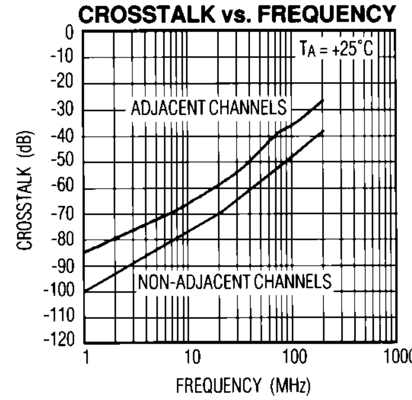
UNITY-GAIN OUTPUT IMPEDANCE vs. FREQUENCY



VOLTAGE-NOISE DENSITY vs. FREQUENCY

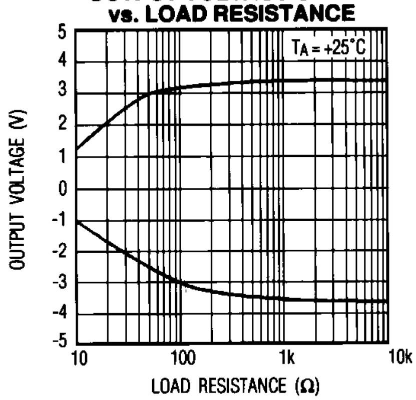


CROSSTALK vs. FREQUENCY

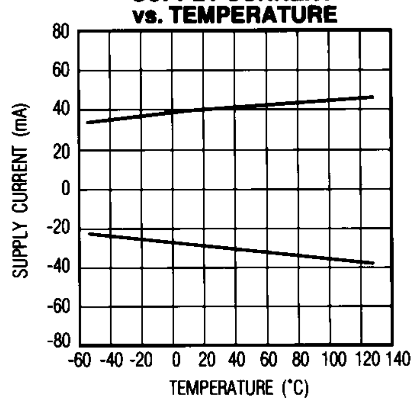


Typical Operating Characteristics (continued)

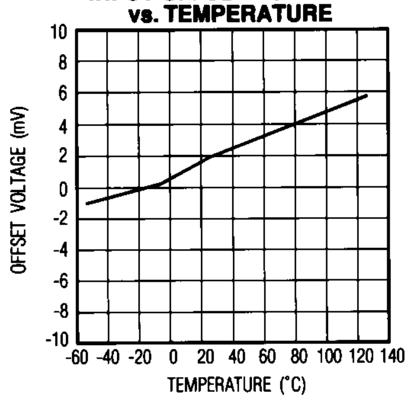
OUTPUT VOLTAGE SWING vs. LOAD RESISTANCE



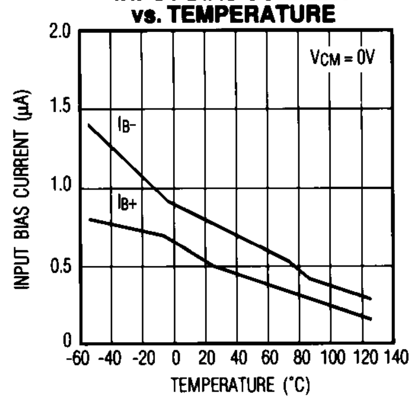
SUPPLY CURRENT vs. TEMPERATURE



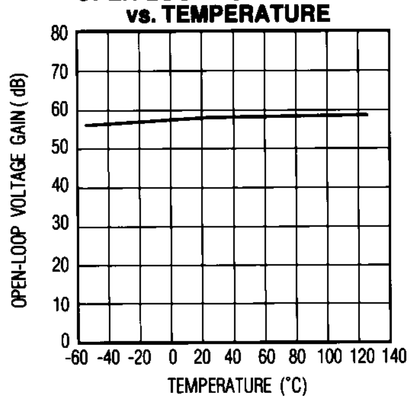
INPUT OFFSET VOLTAGE vs. TEMPERATURE



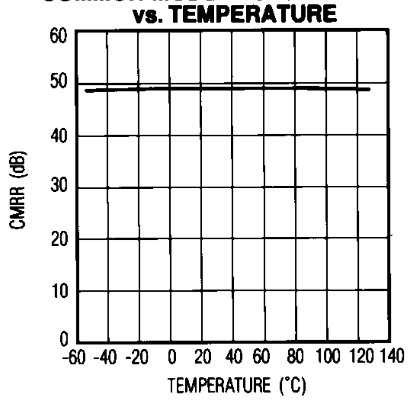
INPUT BIAS CURRENT vs. TEMPERATURE



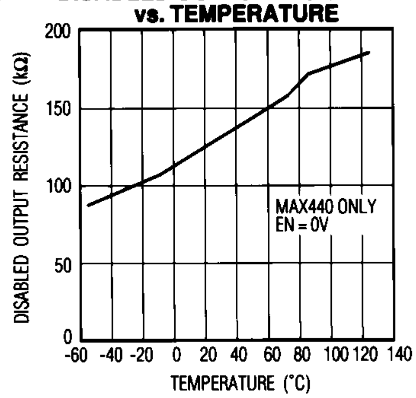
OPEN-LOOP VOLTAGE GAIN vs. TEMPERATURE



COMMON-MODE REJECTION RATIO vs. TEMPERATURE



DISABLED OUTPUT RESISTANCE vs. TEMPERATURE



High-Speed Video Multiplexer/Amplifier

Pin Description

PIN		NAME	FUNCTION
MAX440	MAX441		
1	1	IN0	Analog Input, Channel 0
2	2	LEVEL/EDGE	Digital input that controls the operation of LATCH input as follows: When LEVEL/EDGE = 0V, input data is latched on the rising edge of the LATCH input (edge triggered); when LEVEL/EDGE = 5V, input data is latched when LATCH = 5V (level triggered). Hardwire to +5V or GND for improved crosstalk.
3	4	IN1	Analog Input, Channel 1
4, 10, 12, 14	3, 9	GND	Ground
5	7	IN2	Analog Input, Channel 2
6, 21, 22	5, 16	V+	Positive Power Supply, +5V
7	10	IN3	Analog Input, Channel 3
8, 16, 17	6, 12	V-	Negative Power Supply, -5V
9	–	IN4	Analog Input, Channel 4
11	–	IN5	Analog Input, Channel 5
13	–	IN6	Analog Input, Channel 6
15	–	IN7	Analog Input, Channel 7
18	13	IN-	Amplifier Inverting Input
19	14	V_{OUT}	Amplifier Output
20	15	COMP	Amplifier Compensation Input. Ground for unity-gain application, or use to adjust compensation for higher-gain applications (see text).
23	17	LATCH	Latch control for digital inputs. If LEVEL/EDGE = 0V, data is latched on the rising edge of LATCH. If LEVEL/EDGE = 5V, the input register is transparent when LATCH = 0V and latched when LATCH = 5V.
24	18	A0	Channel Address Input 0, LSB
25	19	A1	Channel Address Input 1, MSB for MAX441
26	–	A2	Channel Address Input 2, MSB
27	–	EN	Amplifier Output Enable control, active high. This is internally latched, along with A0 to A2.
28	20	V_{NS}	Normally -5V, minimize switching time and transients by tying this pin to -2.5V. Analog input voltage must never be more negative than the voltage on this pin.
–	8, 11	N.C.	No Internal Connection

Applications Information

The MAX440/MAX441 are wideband, monolithic video multiplexer/amplifiers with 8 and 4 input channels, respectively. The output amplifier is used in the noninverting configuration and features pin-selectable frequency compensation.

The MAX440/MAX441's bipolar construction results in a typical channel input capacitance of only 4pF, whether the channel is on or off. The mux's input capacitance forms a single-pole RC lowpass filter with the output impedance of the signal source. This filter can limit the system's signal bandwidth if the RC product becomes too large. The MAX440/MAX441's low-channel input capacitance allows the amplifier's full AC performance to be realized, even with source impedances as great as 250Ω.

Feedback resistors should be limited to no more than 500Ω to ensure that the RC time constant formed by the resistors, the circuit board's capacitance, and the capacitance of the amplifier input pins does not limit the system's high-speed performance.

Power-Supply Bypassing and Board Layout

Realizing the full potential AC performance of high-speed amplifiers requires careful attention to power-supply bypassing and board layout. Use a large, low-impedance ground plane with the MAX440/MAX441. With multi-layer boards, the ground plane should be located on the PC board's component side to minimize impedance between the components and the ground plane. For single-layer printed circuit (PC) boards, components should be mounted on the board's copper side and the ground plane should include the entire portion of the PC board that is not dedicated to a specific signal trace.

To prevent oscillation and unwanted signal coupling, minimize trace area at critical high-impedance nodes of the circuit, especially the amplifier summing junction. These critical nodes should also be surrounded by a ground trace. Ground traces should be included between all signal traces to minimize parasitic coupling that can degrade crosstalk and/or stability of the amplifier. Signal paths should be kept as short as possible to minimize inductance, and all input channel traces should be of equal length to maintain the phase relationship between the input channels.

All power-supply pins should be bypassed directly to the ground plane with 0.1μF ceramic capacitors, placed as close to the supply pins as possible. For high-current loads, it may be necessary to include 1μF tantalum or aluminum electrolytic capacitors in parallel with the 0.1μF ceramics. Capacitor lead lengths should be kept as short as possible to minimize series inductance; surface-mount (chip) capacitors are ideal for this application.

Frequency Compensation

Three different frequency compensation modes are available for the MAX440/MAX441. The compensation is determined by the closed-loop gain of the application circuit and is selected by the state of the COMP pin as shown in Table 1. For closed-loop gains below 6dB, the COMP pin should be tied to ground to ensure sufficient phase margin for stable circuit operation.

Table 1. COMP Pin State vs. Closed-Loop Gain

Closed-Loop Gain		COMP Pin State
V/V	dB	
$1 \le A_{VCL} \le 2$	$0 \le A_{VCL} \le 6$	GND
$2 \le A_{VCL} \le 10$	$6 \le A_{VCL} \le 20$	OPEN
$A_{VCL} \ge 10$	$A_{VCL} \ge 20$	V_{OUT}

For closed-loop voltage gains from 6dB up to 20dB, the COMP pin should be left open to maximize the amplifier's AC performance (slew rate, bandwidth, differential gain and phase errors). The COMP pin can also be grounded to increase phase margin for minimizing overshoot and/or ringing of the output pulse response or for driving capacitive loads. The amplifier's AC performance will be slightly degraded if COMP is grounded.

For applications with closed-loop voltage gains of 20dB or more, the COMP pin should be tied to the amplifier output to obtain the maximum high-speed response from the amplifier. Phase margin can be progressively increased by leaving the COMP pin open or tying it to ground.

Plots of the open-loop gain and phase response for the three different compensation modes are shown in the *Typical Operating Characteristics* section. Closed-loop gain plots are also included for each of the three compensation modes at a typical operating closed- loop gain (COMP = GND, A_{VCL} = 0dB; COMP = OPEN, A_{VCL} = 6dB; and COMP = V_{OUT}, A_{VCL} = 20dB).

Figure 1 shows photographs of the amplifier's large-signal pulse response for each of the three compensation modes. In each of these photographs, the MAX440/MAX441 is driving a back-terminated 50Ω cable, so the output amplitude shown at the end of the cable is attenuated by 6dB from the amplifier output.

Differential Gain and Phase Errors

In color-video applications, differential gain and phase errors are critical specifications for an amplifier, because these errors directly correspond to changes in the contrast and color of the displayed picture. The MAX440/MAX441 have a differential gain error of 0.04% and a differential phase error of 0.03°, making them ideal for use in broadcast-quality color-video systems.

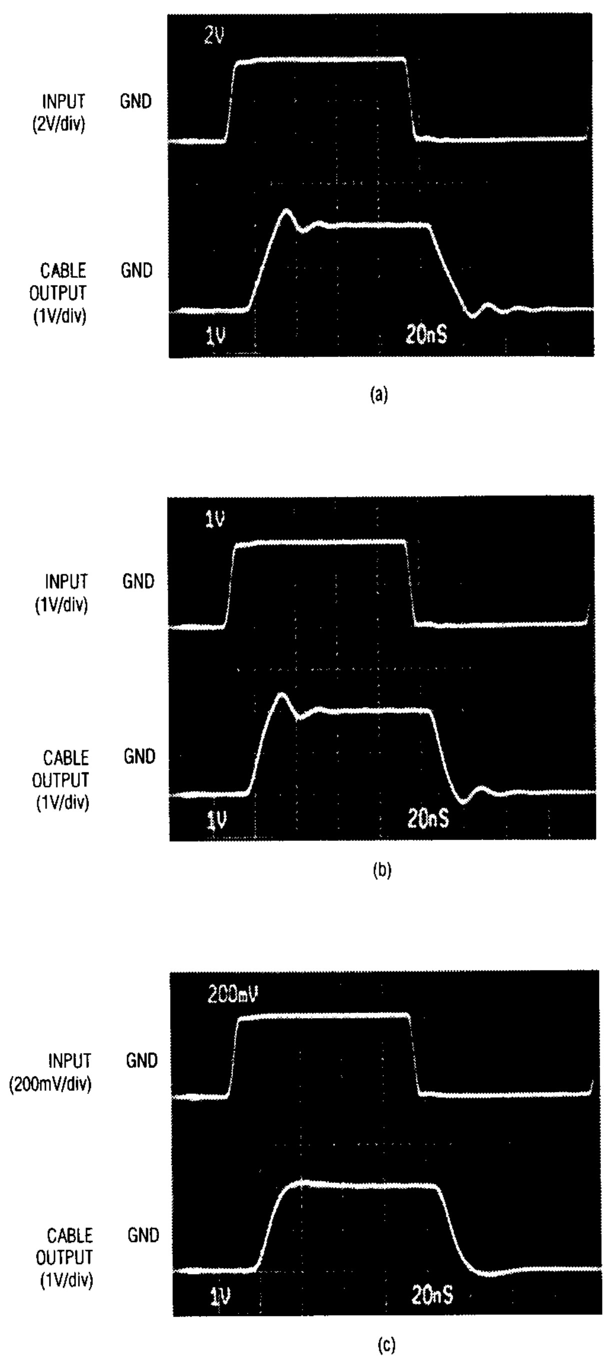


Figure 1. (a) Pulse response with R_L = 100Ω (50Ω back-terminated cable), A_{VCL} = +1V/V, and COMP = GND; (b) Pulse response with R_L = 100Ω (50Ω back-terminated cable), A_{VCL} = +2V/V, and COMP = OPEN; (c) Pulse response with R_L = 100Ω (50Ω back-terminated cable) A_{VCL} = +10V/V, and COMP = V_{OUT}.

The MAX440/MAX441's differential gain and phase error are measured with the Tektronix VM700 Video Measurement Set, with the input test signal provided by the Tektronix 1910 Digital Generator. Figure 2 shows the test circuit used. The level of differential gain and phase error will vary slightly with the voltage applied at the V_{NS} pin, as shown in Table 2.

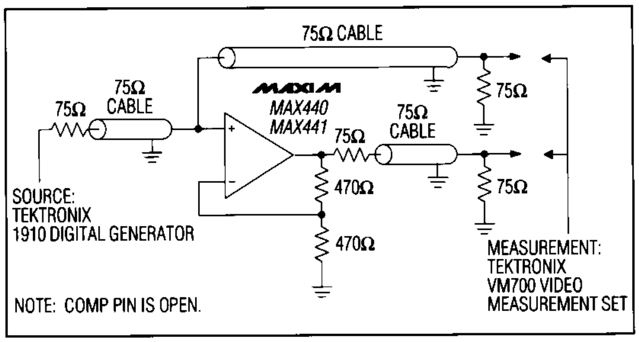


Figure 2. Differential Gain and Phase Error Test Circuit

Table 2. Differential Gain and Phase Error vs. V_{NS} Voltage

V_{NS} VOLTAGE (V)	DIFFERENTIAL GAIN ERROR (%)	DIFFERENTIAL PHASE ERROR (°)
-1.0	0.05	0.04
-1.5	0.04	0.04
-2.0	0.04	0.03
-2.5	0.04	0.03
-5.0	0.04	0.03

Coaxial-Cable Drivers

High-speed performance and excellent output current capability make the MAX440/MAX441 ideal for driving 50Ω or 75Ω coaxial cables. The MAX440/MAX441 will drive a 150Ω load (75Ω back-terminated cable) to ±3V.

Figure 3 shows a MAX440 driving a back-terminated 75Ω video cable. The back-termination resistor (at the MAX440 output) is included to match the impedance at each end of the cable to the characteristic impedance of the cable itself. This practice eliminates signal reflections at the end of the cable. The back-termination resistor forms a voltage divider with the load impedance, which attenuates the signal at the cable output by one-half. The amplifier is operated with a 2V/V closed-loop gain to provide unity gain at the cable's output. The photograph in Figure 1b shows the large-signal pulse response of the MAX440 when driving a back-terminated 50Ω cable, with a 2V/V closed-loop gain and the COMP pin left open.

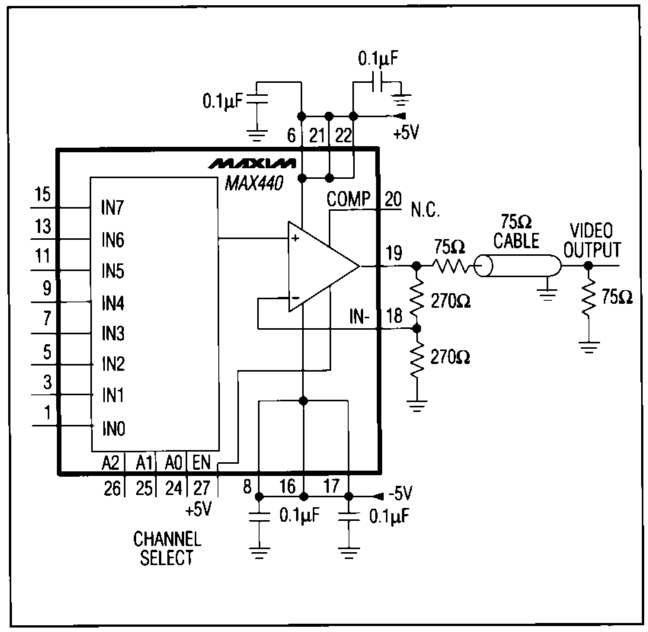


Figure 3. Coaxial-Cable Driver

Capacitive-Load Driving

Driving large capacitive loads increases the likelihood of oscillation in most amplifier circuits. This is especially true for circuits with high loop-gains, like voltage followers. The amplifier's output impedance and the capacitive load form an RC filter that adds a pole to the loop response. If the pole frequency is low enough, as when driving a large capacitive load, the circuit phase margin is degraded and oscillation may occur.

The MAX440/MAX441 phase margin and capacitive-load driving performance is optimized when the amplifier is fully compensated internally. This is accomplished by connecting the COMP pin to circuit ground. When driving large (>50pF) capacitive loads in voltage-follower circuits, an isolation resistor should be added between the amplifier output and the capacitive load, as shown in Figure 4.

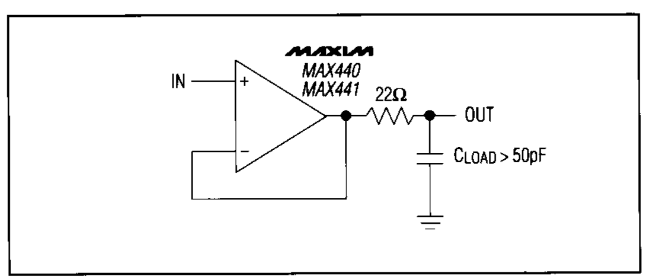


Figure 4. Capacitive-Load Driving Circuit

For improved capacitive-load driving performance without the series isolation resistor, the MAX440/MAX441 should be operated with a closed-loop gain of 6dB (+2V/V) or greater, and the COMP pin should be grounded.

Digital Interface

The multiplexer architecture ensures that no two input channels are ever connected together. Channel selection is performed by applying a binary code to the address inputs A0, A1, and A2 (A0 and A1 only for MAX441). The address decoder selects input channels, as shown in Table 3. All digital inputs are compatible with TTL and CMOS logic levels.

Table 3. Channel Selection

MAX440					MAX441		
EN	**A2**	**A1**	**A0**	**SELECTED CHANNEL**	**A1**	**A0**	**SELECTED CHANNEL**
0	X	X	X	High-Z-Output	0	0	0
1	0	0	0	0	0	1	1
1	0	0	1	1	1	0	2
1	0	1	0	2	1	1	3
1	0	1	1	3			
1	1	0	0	4			
1	1	0	1	5			
1	1	1	0	6			
1	1	1	1	7			

An address latch, which retains channel selection data while the data bus is used for other purposes, is provided on the MAX440/MAX441. The latch is in either an edge-triggered mode or a level-triggered mode, depending on the state of the LEVEL/$\overline{\text{EDGE}}$ control input. If LEVEL/$\overline{\text{EDGE}}$ is low, the latch operates in edge- triggered mode, with the latch occuring on the rising edge of the LATCH input. If LEVEL/$\overline{\text{EDGE}}$ is high, then the latch operates in level-triggered mode and input data is latched when LATCH is high. If LEVEL/$\overline{\text{EDGE}}$ is high and LATCH is low, the input register is transparent.

Channel Switching Time and Transient

When switching between input channels, the transient voltage at the output of the MAX440/MAX441 depends on the voltage level at the V_{NS} pin. The voltage at this pin should lie within the -1V to -5V range, and is adjusted using Figure 5's circuit. **Note: The input voltage must never be allowed to be more negative than the voltage at V_{NS}.**

The switching transient's magnitude and the channel switching time both increase as the V_{NS} voltage gets more negative. The photos in Figures 6 and 7 illustrate this phenomenon. In Figure 6, the V_{NS} voltage is -2.5V, and the switching transient peak level is $100mV_{P-P}$. In Figure 7, with V_{NS} at -5V, the switching transient is about $800mV_{P-P}$. The typical channel switching time increases from 15ns to 25ns as the V_{NS} voltage decreases from

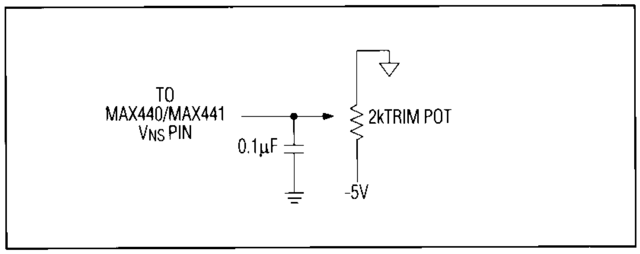


Figure 5. V_{NS} Pin-Voltage Adjustment

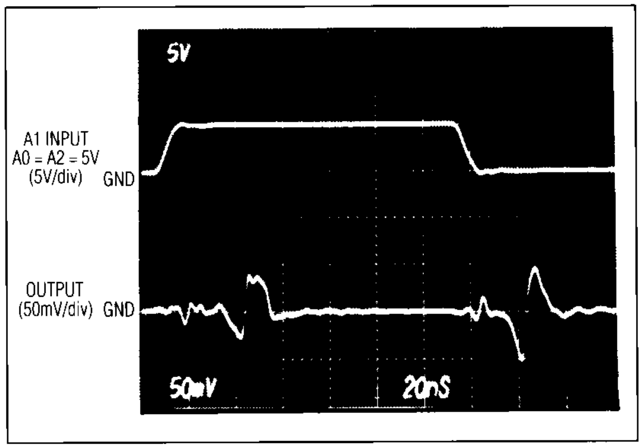


Figure 6. Output Transient When Switching Between Two Grounded Inputs with R_L = 75Ω and V_{NS} = -2.5V

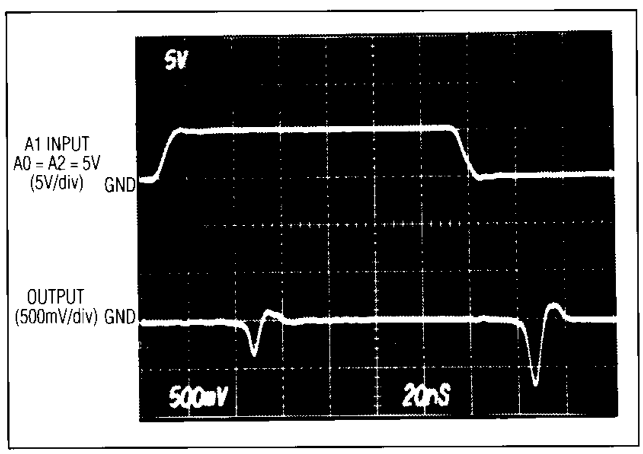


Figure 7. Output Transient When Switching Between Two Grounded Inputs with R_L = 75Ω and V_{NS} = -5.0V

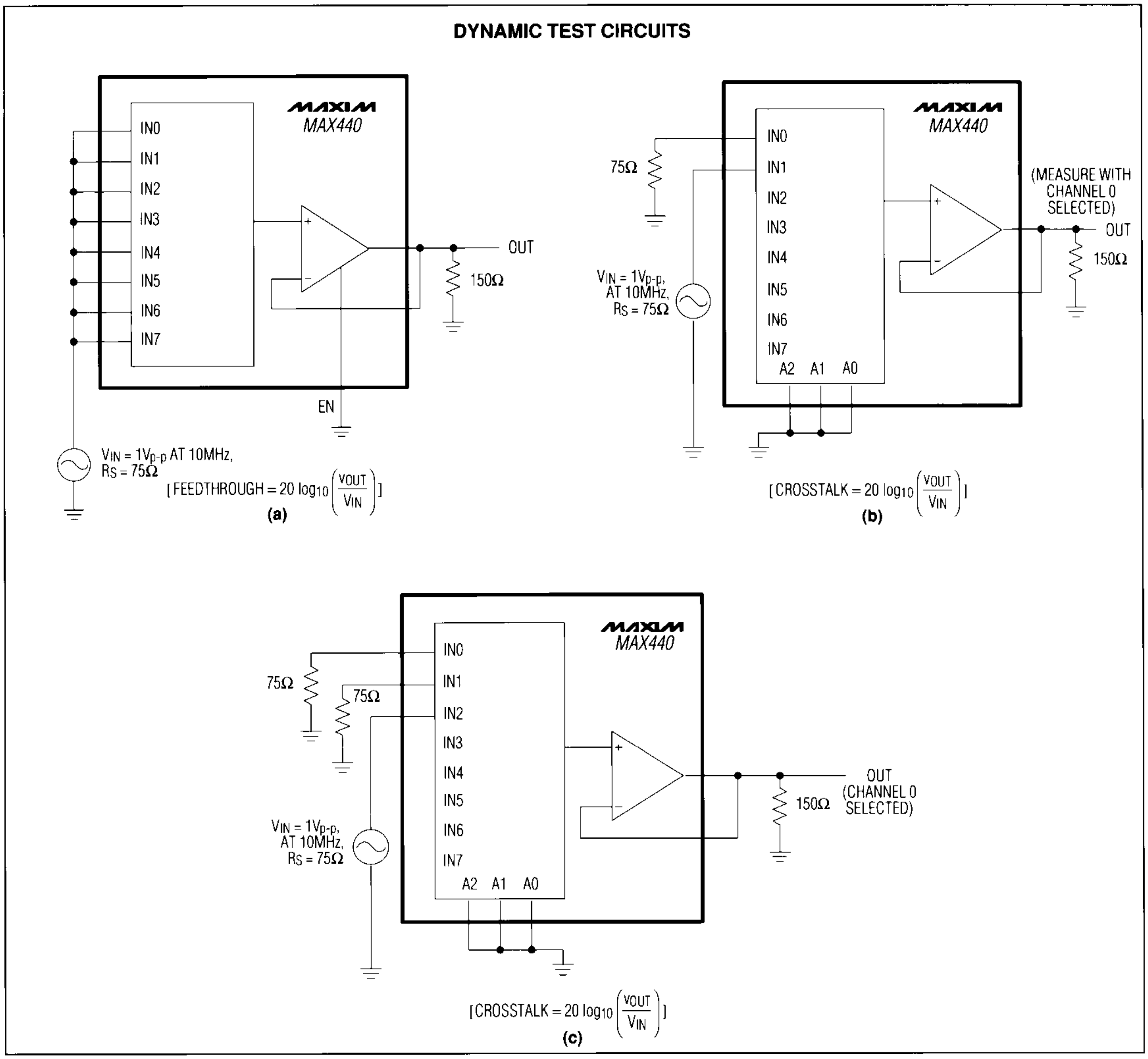


Figure 8. (a) Disabled Amplifier Feedthrough; (b) Adjacent Channel Crosstalk; (c) Non-Adjacent Channel Crosstalk

-2.5V to -5V. Figure 10 shows the MAX440/MAX441 timing diagram.

Output Disable (MAX440 Only)

The EN pin is provided on the MAX440 to enable the amplifier output when driven to a TTL high state. When EN is driven low, the MAX440's output becomes a high-impedance load with a 130kΩ typical resistance and a 15pF typical capacitance. When disabled, the signal feedthrough from the mux inputs to the amplifier output is -63db at 10MHz, with all 8 input channels driven with a $1V_{P-P}$ sine wave and a 150Ω load impedance. Figure 8a shows the test circuit used to measure feedthrough.

The output disable capability allows several MAX440s to be paralleled to form larger switch matrices, by tying the outputs together and disabling all but one of the paralleled amplifier outputs. Figure 9 shows the 1-of-16 video mux/amp circuit that uses this feature. In this example, the EN inputs of the MAX440s are used as a 4th address

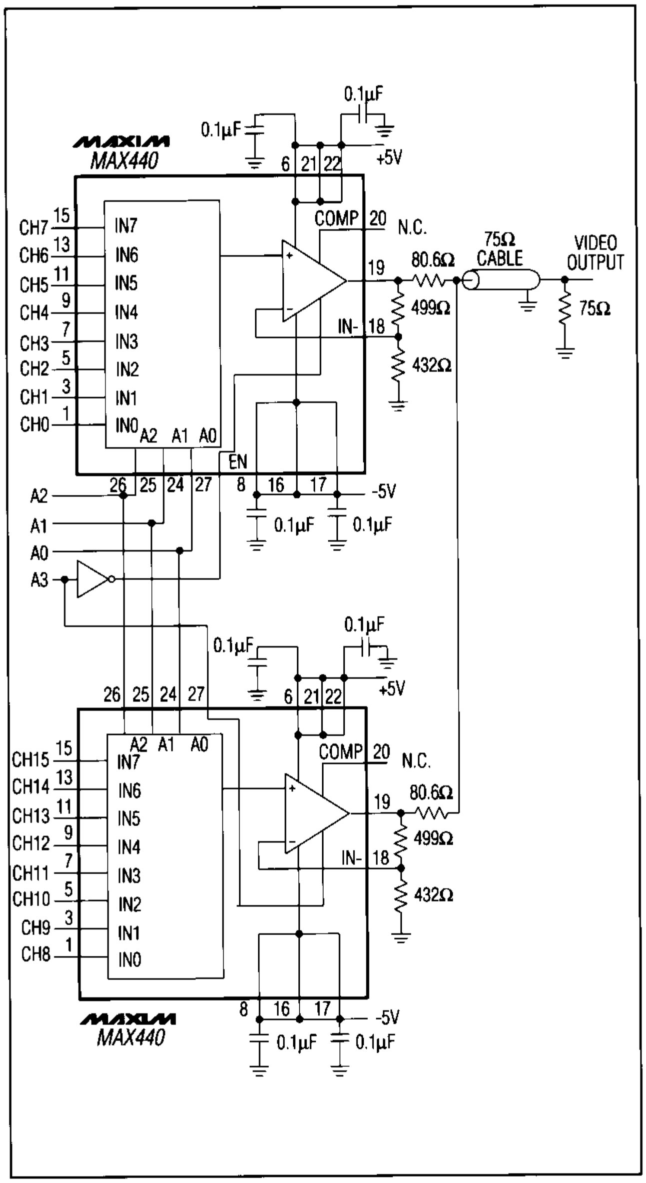


Figure 9. 1-of-16 Video Multiplexer

Table 4. 1-of-16 Video Mux/Amp Channel Selection

A3	A2	A1	A0	SELECTED CHANNEL
0	0	0	0	0
0	0	0	1	1
0	0	1	0	2
0	0	1	1	3
0	1	0	0	4
0	1	0	1	5
0	1	1	0	6
0	1	1	1	7
1	0	0	0	8
1	0	0	1	9
1	0	1	0	10
1	0	1	1	11
1	1	0	0	12
1	1	0	1	13
1	1	1	0	14
1	1	1	1	15

bit (A3), with an inverter added to ensure the amplifiers are not simultaneously enabled. The amplifier outputs are connected after the back-termination resistors, so that the active amplifier output is isolated from the capacitive load (15pF typ) presented by the inactive output of the second MAX440. This will minimize ringing in the output signal.

The disabled amplifier's back-termination and gain resistors form a voltage divider with the back-termination resistor at the active amplifier's output. The amplifier closed-loop gains have been set slightly greater than 6dB to compensate for the signal attenuation caused by this divider. The value of the back-termination resistors has been increased to 80.6Ω so the parallel combination of the resistors at the cable's input equals 75Ω.

With proper selection of resistor values, this configuration can be expanded to form larger switch matrices. The number of paralled devices is limited primarily by the MAX440's disabled feedthrough. Table 4 shows the relationship between the digital input code and the selected output channel for Figure 9's circuit.

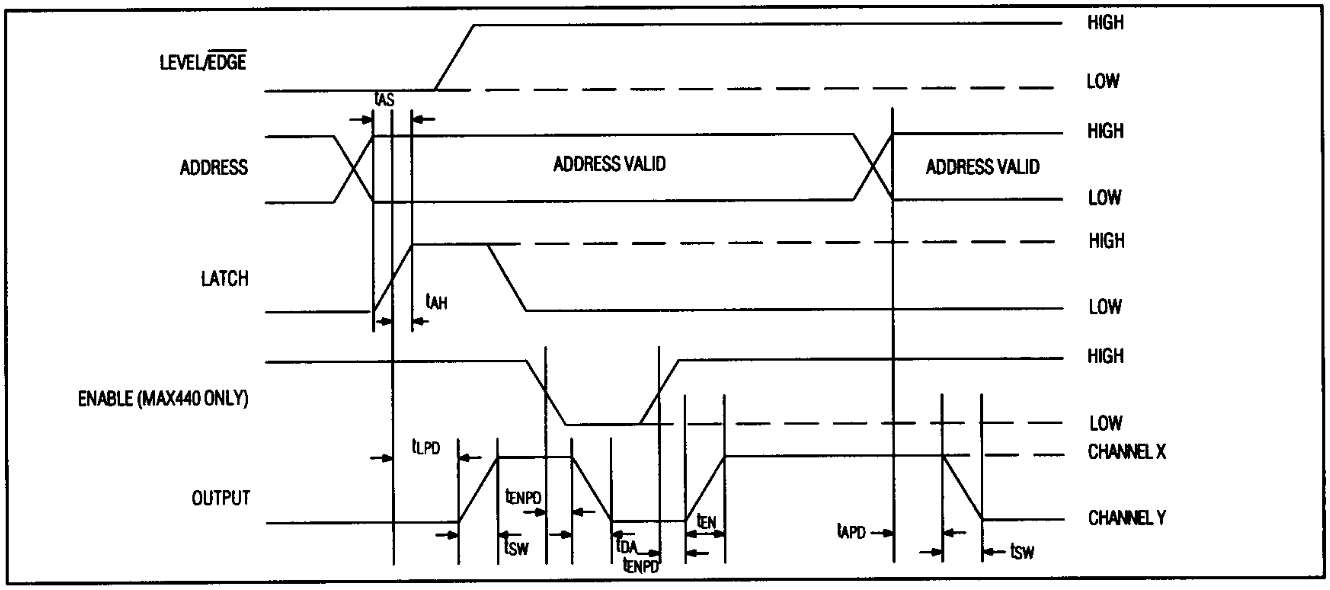
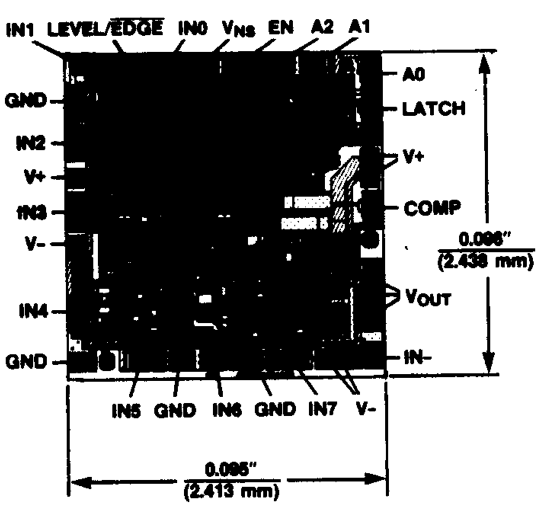


Figure 10. MAX440/MAX441 Timing Diagram

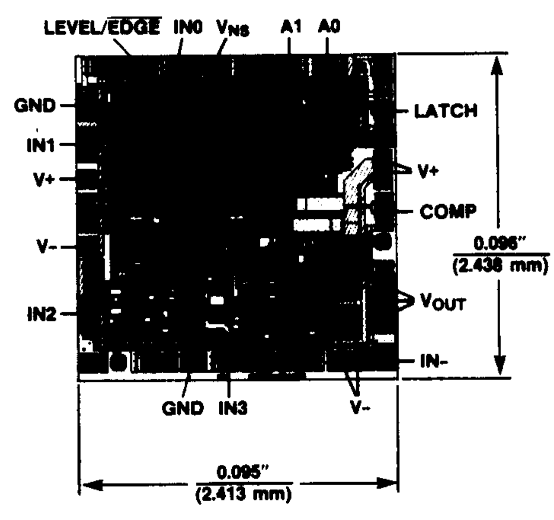
Chip Topographies

MAX440



TRANSISTOR COUNT: 564

MAX441



TRANSISTOR COUNT: 564

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