

Power MOSFET

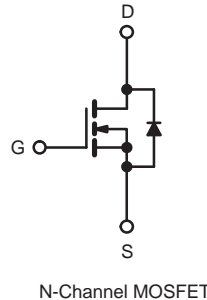
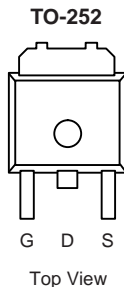
PRODUCT SUMMARY		
V_{DS} (V)	600	
$R_{DS(on)}$ (Ω)	$V_{GS} = 10\text{ V}$	4.4
Q_g (Max.) (nC)	18	
Q_{gs} (nC)	3.0	
Q_{gd} (nC)	8.9	
Configuration	Single	

FEATURES

- Halogen-free According to IEC 61249-2-21 Definition
- Dynamic dV/dt Rating
- Repetitive Avalanche Rated
- Surface Mount (IRFRC20, SiHFRC20)
- Straight Lead (IRFUC20, SiHFUC20)
- Available in Tape and Reel
- Fast Switching
- Ease of Paralleling
- Compliant to RoHS Directive 2002/95/EC



Available
RoHS*
COMPLIANT
HALOGEN
FREE
Available



ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$, unless otherwise noted					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		V_{DS}	600	V	
Gate-Source Voltage		V_{GS}	± 20		
Continuous Drain Current	V_{GS} at 10 V	I_D	$T_C = 25\text{ }^\circ\text{C}$	2.0	A
			$T_C = 100\text{ }^\circ\text{C}$	1.3	
Pulsed Drain Current ^a		I_{DM}	8.0	W/ $^\circ\text{C}$	
Linear Derating Factor			0.33		
Linear Derating Factor (PCB Mount) ^e			0.020		
Single Pulse Avalanche Energy ^b		E_{AS}	74	mJ	
Repetitive Avalanche Current ^a		I_{AR}	2.0	A	
Repetitive Avalanche Energy ^a		E_{AR}	4.2	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	P_D	42	W	
	$T_A = 25\text{ }^\circ\text{C}$		2.5		
Peak Diode Recovery dV/dt^c		dV/dt	3.0	V/ns	
Operating Junction and Storage Temperature Range		T_J, T_{stg}	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s		260 ^d		

Notes

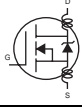

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- $V_{DD} = 50\text{ V}$, starting $T_J = 25\text{ }^\circ\text{C}$, $L = 37\text{ mH}$, $R_g = 25\text{ }\Omega$, $I_{AS} = 2.0\text{ A}$ (see fig. 12).
- $I_{SD} \leq 2.0\text{ A}$, $dI/dt \leq 40\text{ A}/\mu\text{s}$, $V_{DD} \leq V_{DS}$, $T_J \leq 150\text{ }^\circ\text{C}$.
- 1.6 mm from case.
- When mounted on 1" square PCB (FR-4 or G-10 material).

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS						
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	
Maximum Junction-to-Ambient	R_{thJA}	-	-	110	°C/W	
Maximum Junction-to-Ambient (PCB Mount) ^a	R_{thJA}	-	-	50		
Maximum Junction-to-Case (Drain)	R_{thJC}	-	-	3.0		

Note

a. When mounted on 1" square PCB (FR-4 or G-10 material).

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX. UNIT	
Static							
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	- V	
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}, I_D = 1\text{ mA}$		-	0.88	- $V/^\circ\text{C}$	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		2.0	-	4.0 V	
Gate-Source Leakage	I_{GSS}	$V_{GS} = \pm 20\text{ V}$		-	-	$\pm 100\text{ nA}$	
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	100 μA	
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	500 μA	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 1.2\text{ A}^b$	-	4.4	- Ω	
Forward Transconductance	g_{fs}	$V_{DS} = 50\text{ V}, I_D = 1.2\text{ A}$		1.4	-	- S	
Dynamic							
Input Capacitance	C_{iss}	$V_{GS} = 0\text{ V}, V_{DS} = -25\text{ V}, f = 1.0\text{ MHz}, \text{ see fig. 5}$		-	350	-	
Output Capacitance	C_{oss}			-	48	-	pF
Reverse Transfer Capacitance	C_{rss}			-	8.6	-	
Total Gate Charge	Q_g	$V_{GS} = 10\text{ V}$	$I_D = 2.0\text{ A}, V_{DS} = 360\text{ V}, \text{ see fig. 6 and 13}^b$	-	-	18	
Gate-Source Charge	Q_{gs}			-	-	3.0	nC
Gate-Drain Charge	Q_{gd}			-	-	8.9	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 2.0\text{ A}, R_g = 18\text{ }\Omega, R_D = 135\text{ }\Omega, \text{ see fig. 10}^b$		-	10	-	
Rise Time	t_r			-	23	-	ns
Turn-Off Delay Time	$t_{d(off)}$			-	30	-	
Fall Time	t_f			-	25	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	
Internal Source Inductance	L_S			-	7.5	-	nH
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	2.0	
Pulsed Diode Forward Current ^a	I_{SM}			-	-	8.0	A
Body Diode Voltage	V_{SD}	$T_J = 25\text{ }^\circ\text{C}, I_S = 2.0\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.6 V	
Body Diode Reverse Recovery Time	t_{rr}	$T_J = 25\text{ }^\circ\text{C}, I_F = 2.0\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$		-	290	580 ns	
Body Diode Reverse Recovery Charge	Q_{rr}			-	0.67	1.3 μC	
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\text{ }\%$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

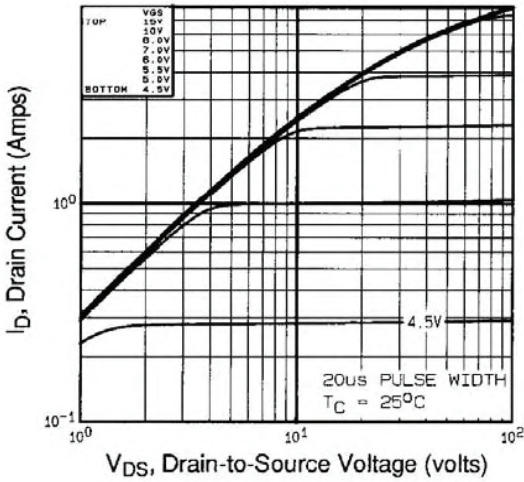


Fig. 1 - Typical Output Characteristics, $T_C = 25\text{ }^\circ\text{C}$

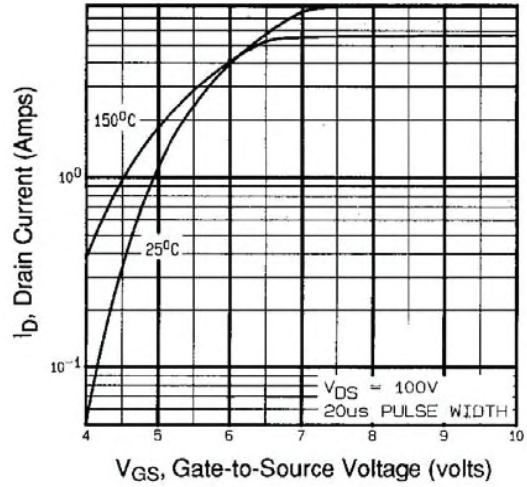


Fig. 3 - Typical Transfer Characteristics

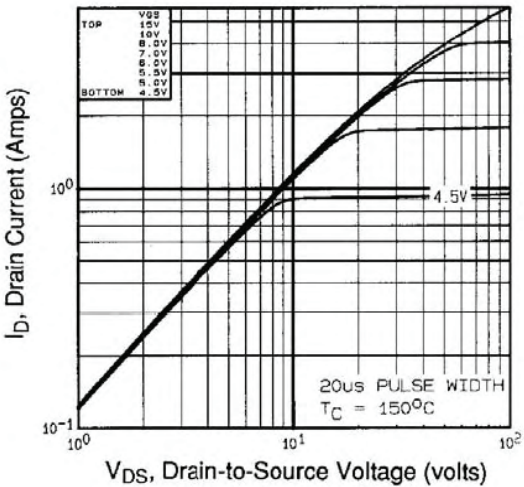


Fig. 2 - Typical Output Characteristics, $T_C = 150\text{ }^\circ\text{C}$

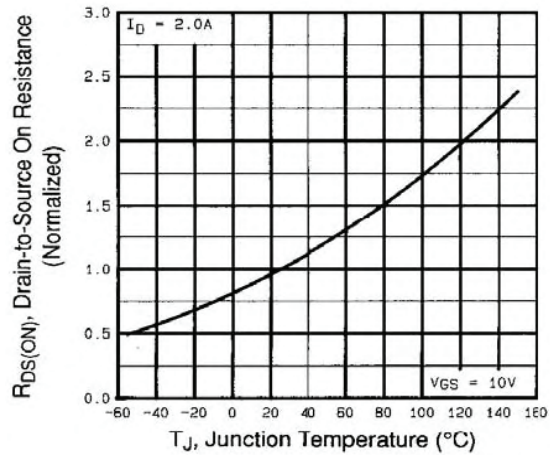


Fig. 4 - Normalized On-Resistance vs. Temperature

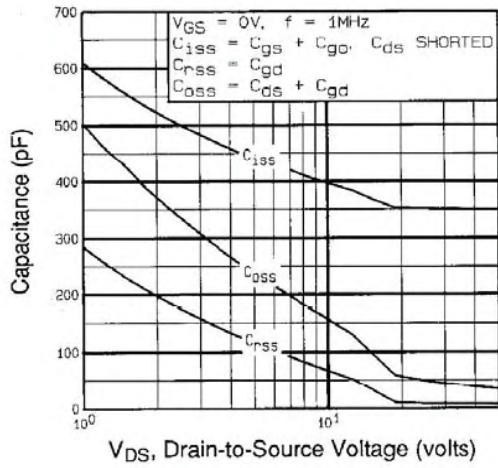


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

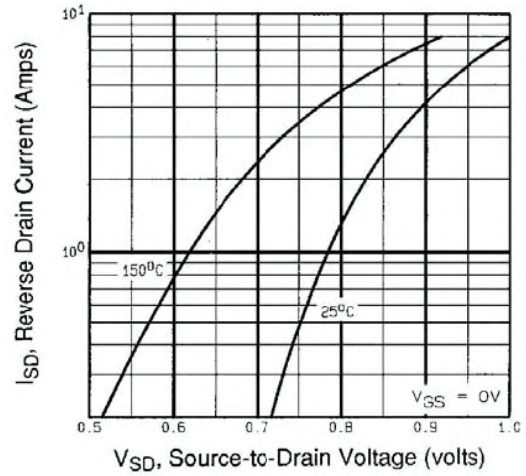


Fig. 7 - Typical Source-Drain Diode Forward Voltage

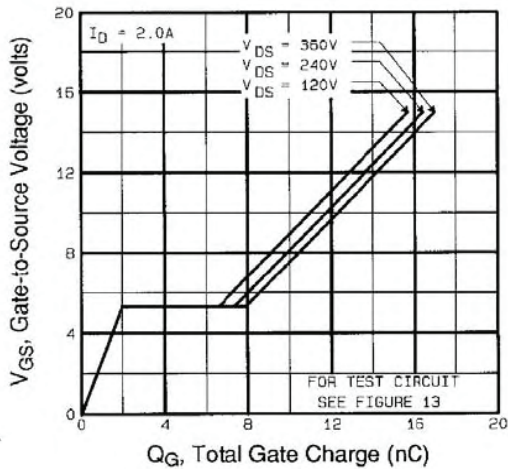


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

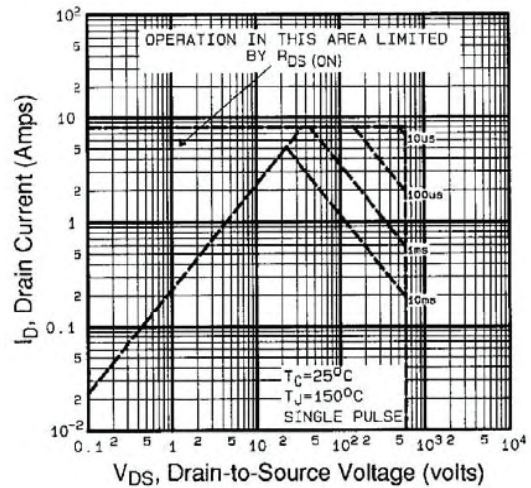


Fig. 8 - Maximum Safe Operating Area

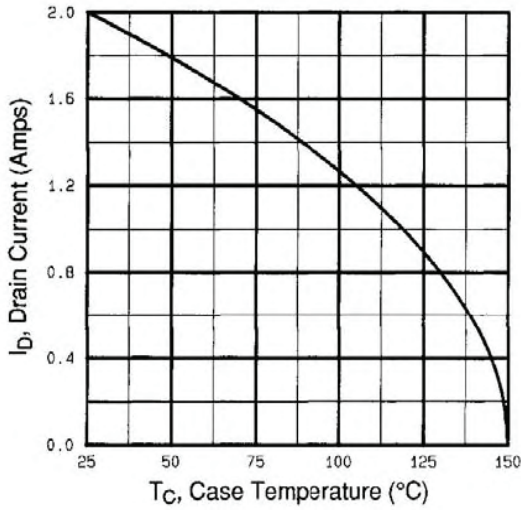


Fig. 9 - Maximum Drain Current vs. Case Temperature

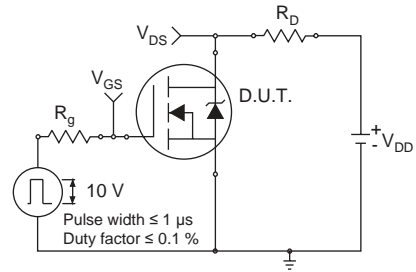


Fig. 10a - Switching Time Test Circuit

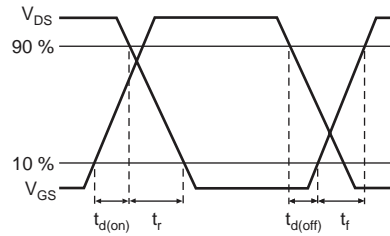


Fig. 10b - Switching Time Waveforms

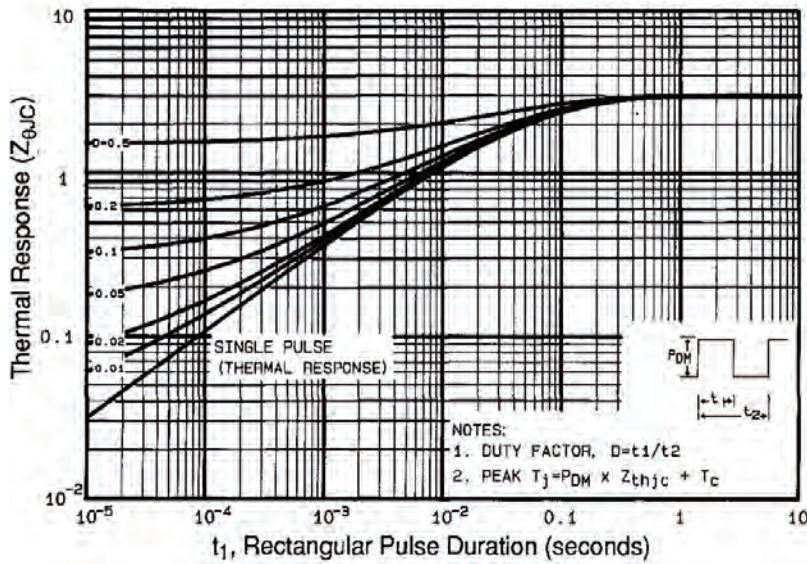


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

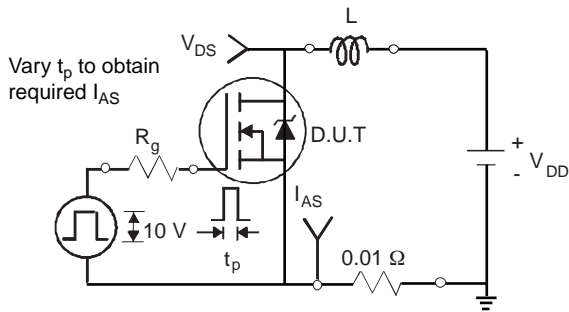


Fig. 12a - Unclamped Inductive Test Circuit

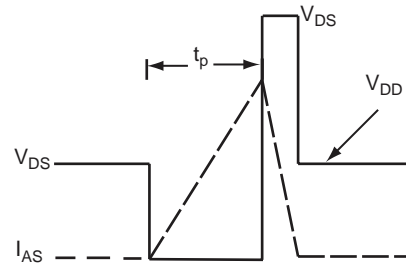


Fig. 12b - Unclamped Inductive Waveforms

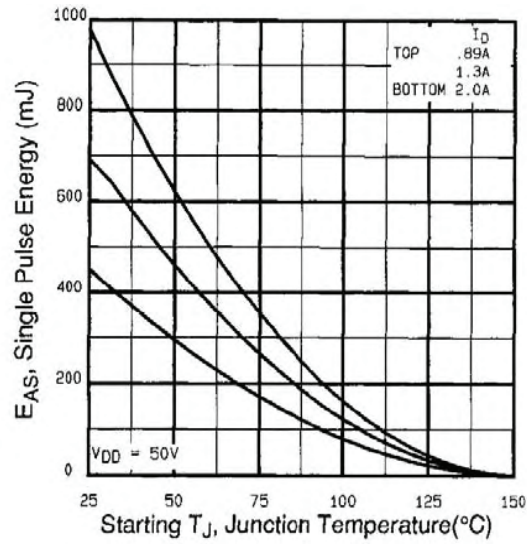


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

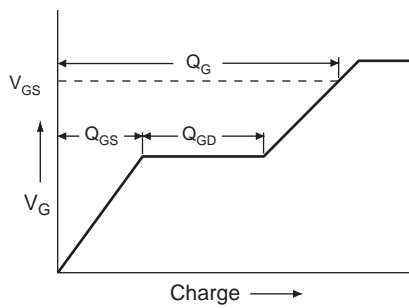


Fig. 13a - Basic Gate Charge Waveform

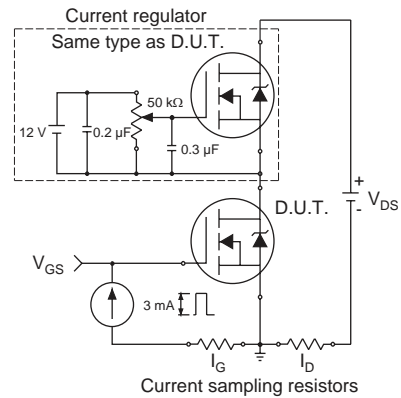
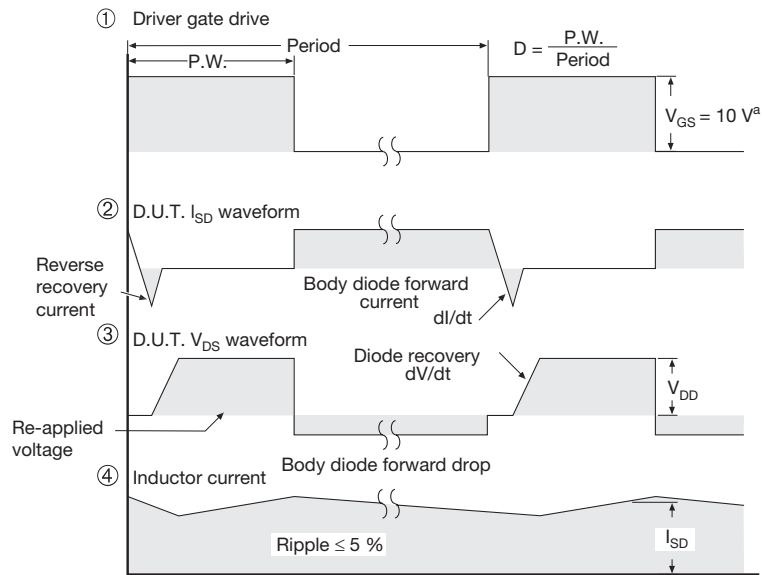
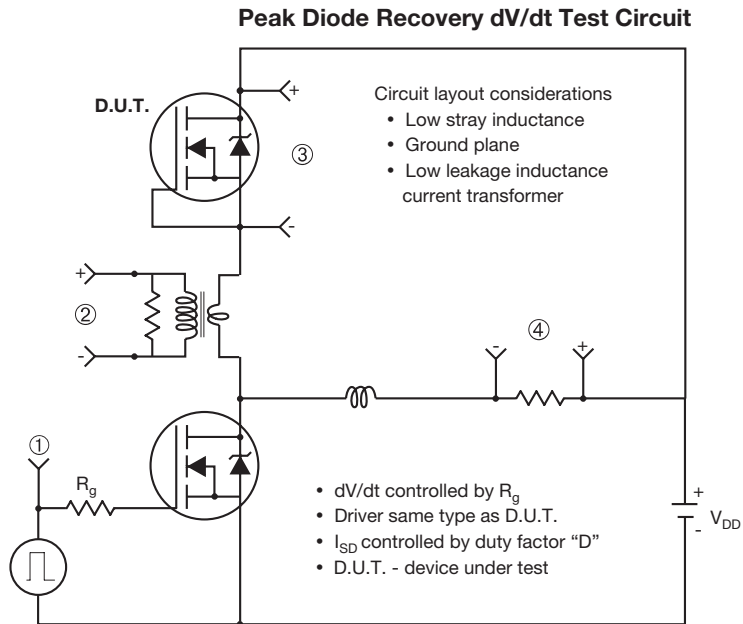


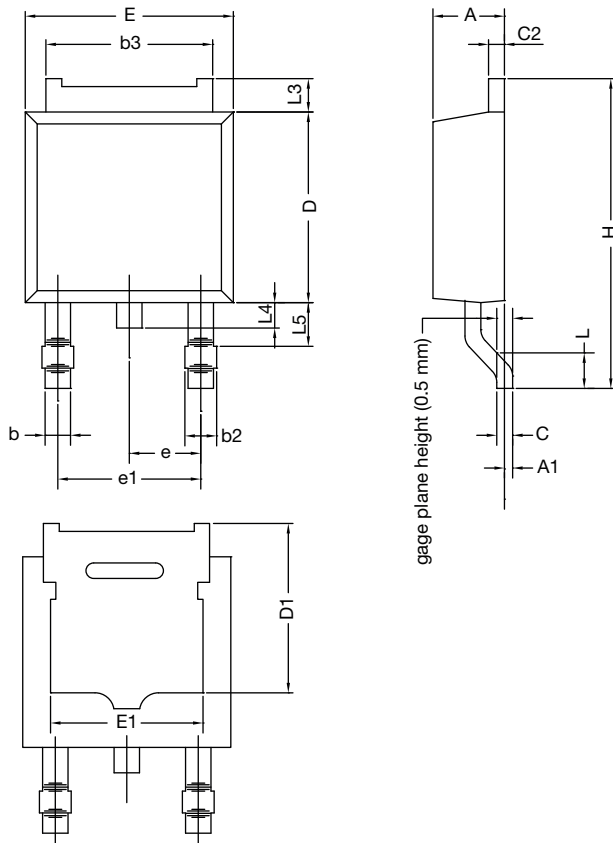
Fig. 13b - Gate Charge Test Circuit



Note
 a. $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-252AA CASE OUTLINE



DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	5.21	-	0.205	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.14	1.52	0.045	0.060
ECN: X12-0247-Rev. M, 24-Dec-12 DWG: 5347				

Note

- Dimension L3 is for reference only.

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