# ADS8168EVM-PDK

The ADS8168 evaluation module (EVM) performance demonstration kit (PDK) is a platform for evaluating the performance of the ADS8168 successive approximation register analog-to-digital converter (SAR ADC). The ADS8168EVM-PDK includes the ADS8168EVM board, the PHI controller board, and accompanying computer software that enables the user to communicate with the ADC over a universal serial bus (USB), capture data, and perform data analysis. This user's guide includes complete circuit descriptions, schematic diagrams, and a bill of materials.

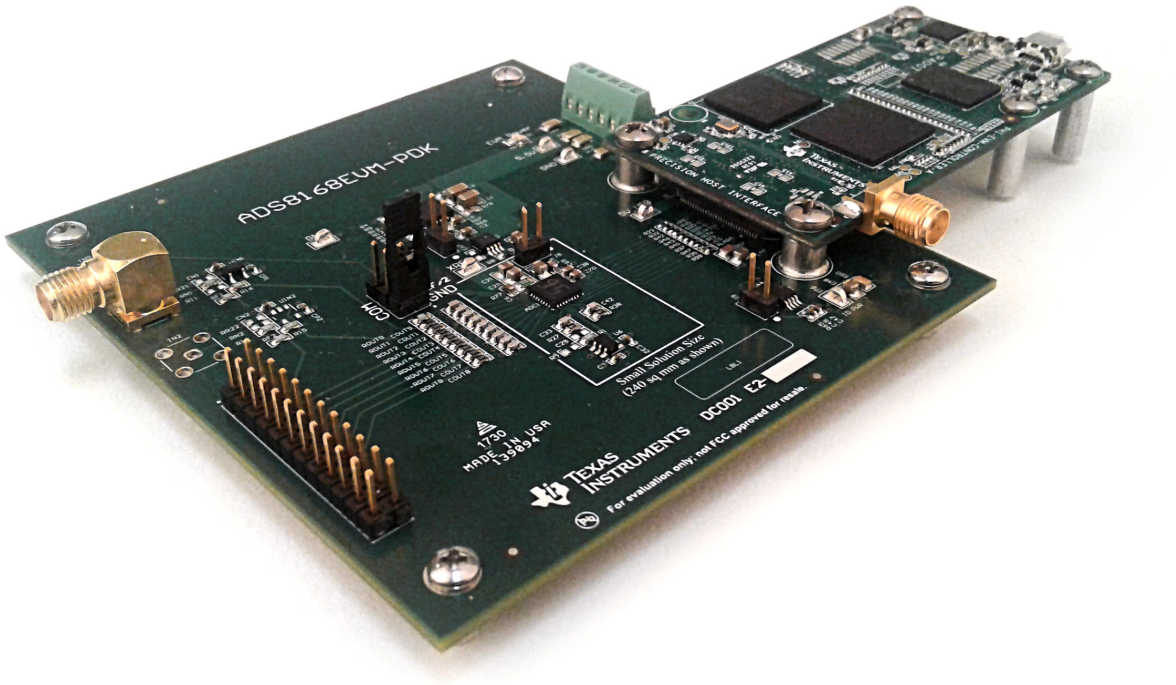


**Figure 1. ADS8268EVM-PDK**

The following related documents are available through the Texas Instruments web site at www.ti.com.

**Related Documentation**

| Device | Literature Number |
|---|---|
| ADS8168 | SBAS817 |
| REF5050 | SBOS410 |
| OPA320 | SBOS513 |

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# 1 Overview

The ADS8168EVM-PDK is a platform for evaluating the performance of the ADS8168 SAR ADC, which is a 8-channel, 16-bit, 1-MSPS device. The evaluation kit includes the ADS8168EVM board and the precision host interface (PHI) controller board that enables the accompanying computer software to communicate with the ADC over USB for data capture and analysis.

The ADS8168EVM board includes the ADS8168 SAR ADC, all the peripheral analog circuits, and components required to demonstrate performance of the ADC.

The PHI board primarily serves three functions:

- Provides a communication interface from the EVM to the computer through a USB port
- Provides the digital input and output signals necessary to communicate with the ADS8168EVM
- Supplies power to all active circuitry on the ADS8168 board

Along with the ADS8168EVM and PHI controller board, this evaluation kit includes an A-to-micro-B USB cable to connect to a computer.

## 1.1 ADS8168EVM-PDK Features

The ADS8168EVM-PDK includes the following features:

- Hardware and software required for diagnostic testing as well as accurate performance evaluation of the ADS8168 ADC
- USB powered—no external power supply is required
- The PHI controller that provides a convenient communication interface to the ADS8168 ADC over a USB 2.0 (or higher) for power delivery as well as digital input and output
- Easy-to-use evaluation software for Microsoft® Windows® 7 and above, 32- and 64-bit operating systems
- The software suite includes graphical tools for data capture, histogram analysis, spectral analysis, and linearity analysis. This suite also has a provision for exporting data to a text file for post-processing.

## 1.2 ADS8168EVM Features

The ADS8168EVM includes the following features:

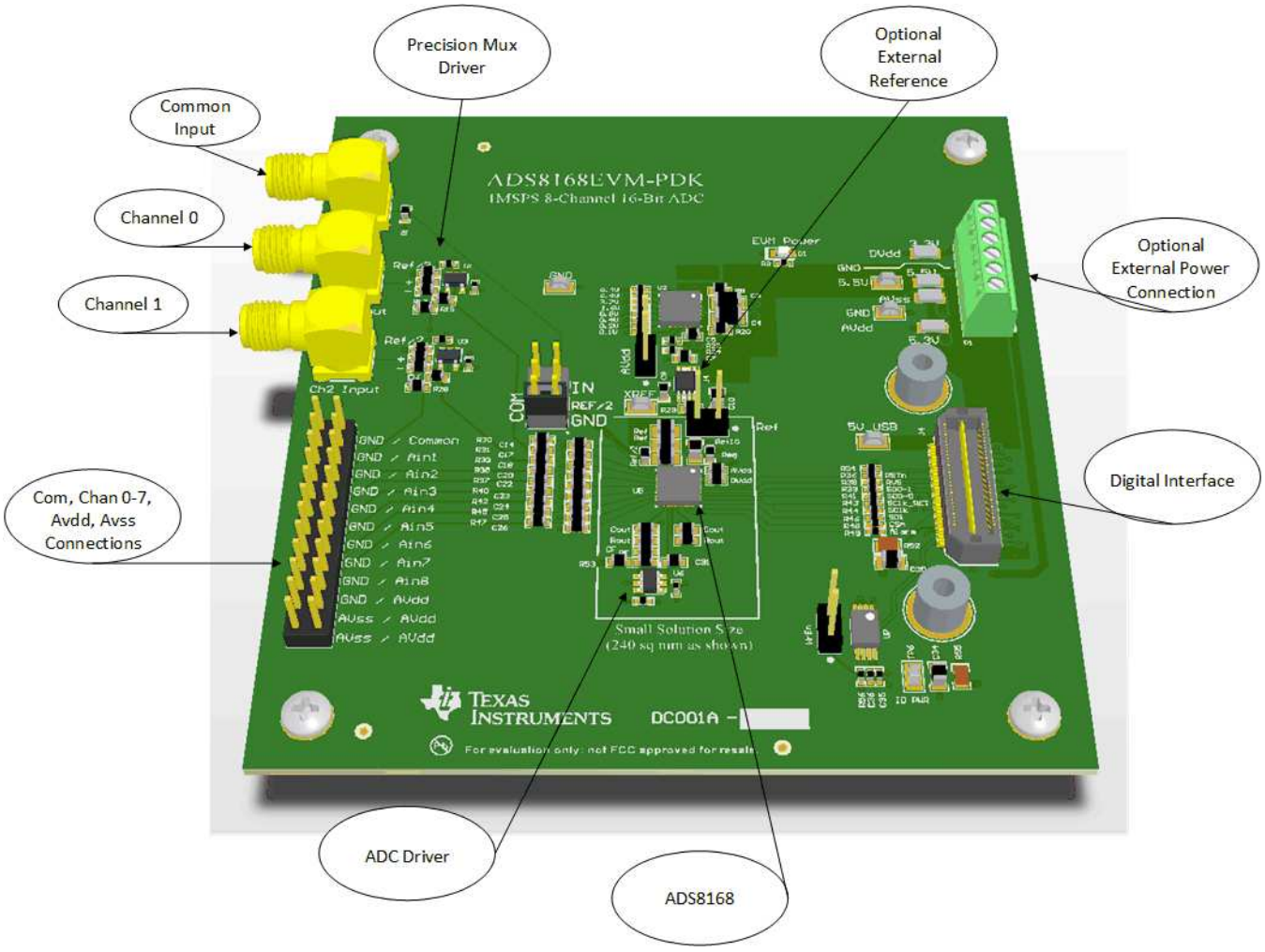
- SMA connections for two channels plus common inputs, pin header connections for all other channels
- Provision for using the onboard precision 5-V voltage reference or the default ADS8168 internal 4.096-V reference. (Selectable by device register setting plus jumpers for the hardware.)

## 1.3 EVM Main Sections (Circuit Blocks)

The ADS8168EVM has the following circuits:

- Input Circuits
  - Channel 1 is populated in buffer configuration, can be driven from SMA connection
  - Channel 2 is unpopulated
  - All channels can be driven by the header pins of P2
  - ADC Driver is in buffer configuration
  - Power generation circuits
  - External reference circuit
  - EEPROM for device identification
  - Connection for external supplies, if desired

**Figure 2. ADS8168EVM Features**



## 2 EVM Analog Interface

The ADS8168EVM is designed for easy interfacing to analog sources. The 12-position, dual-row, pin header connector, J3, provides convenient access to channels Ain1–Ain8 and Ain–COM of the device. In addition, 3 SMA connectors, IN1, IN2, and IN9 provide a high quality connection to channels Ain1, Ain2, and Ain-COM, respectively. For channels 1 and 2, a high-impedance input signal conditioning driver circuit is provided. On all channels, a resistor-capacitor combination helps to provide a stable voltage on the input of the ADS8168 multiplexer inputs.

**Table 1. P2 Header Analog Interface Connections**

| Header Pin Number | Signal | Description |
|---|---|---|
| P2.1, P2.3, P2.5, P2.7, P2.9, P2.11, P2.13, P2.15, P2.17, P2.19 | GND | Analog Ground |
| P2.2 | COM | ADC input common |
| P2.4 | AIN1 | Analog Channel 1 |
| P2.6 | AIN2 | Analog Channel 2 |
| P2.8 | AIN3 | Analog Channel 3 |
| P2.10 | AIN4 | Analog Channel 4 |
| P2.12 | AIN5 | Analog Channel 5 |
| P2.14 | AIN6 | Analog Channel 6 |
| P2.16 | AIN7 | Analog Channel 7 |
| P2.18 | AIN8 | Analog Channel 8 |
| P2.20, P2.22, P2.24 | $AV_{DD}$ | Positive analog power supply |
| P2.21, P2.23 | $AV_{SS}$ | Negative analog power supply (default connection is GND) |

## 2.1 ADS8168 Internal Reference and EVM Onboard Reference

The ADS8168 device incorporates an internal 4.096-V reference. Upon power up, the device uses this configuration. In order to select the external reference, the user must select the external reference mode by writing to the configuration register of the ADS8168. Next, power up the external reference by installing a shunt on JP1, labeled "AVdd"; and connect the reference to the ADS8168 by installing a shunt on JP3, labeled "Ref". Input is now 0 V to 5 V. In this mode, note that the reference is limited by the internal reference buffer of the ADS8168 to $AV_{DD}$ – 0.3 V. A 5-V reference voltage is possible due to the operation of $AV_{DD}$ at 5.3 V.

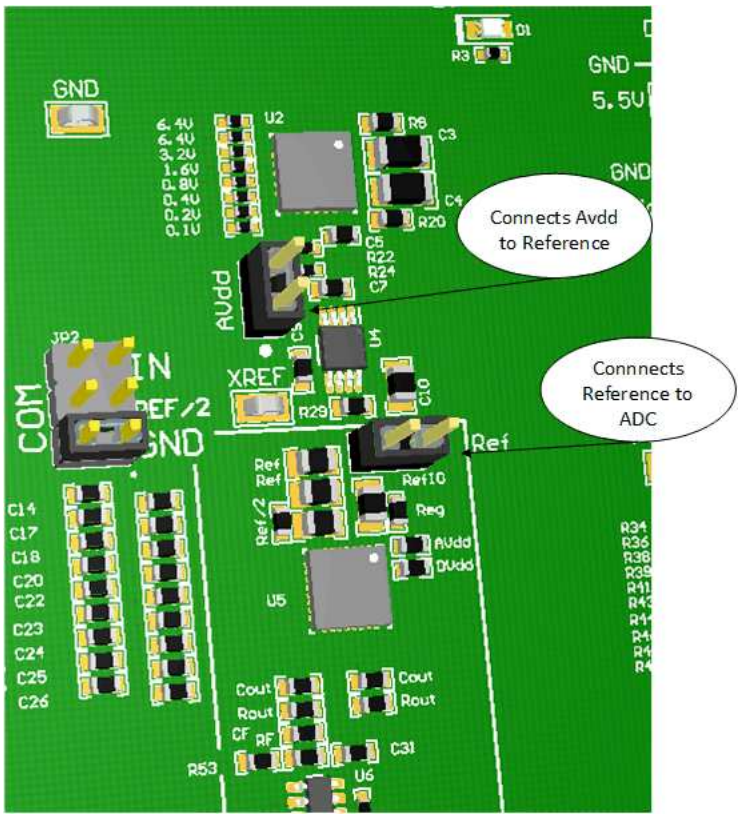



**Figure 3. REF5050 5.0-V External Reference Source**

# 3 Digital Interfaces

The EVM interfaces with the PHI that, in turn, communicates with the computer over USB. There are two devices on the EVM with which the PHI communicates: the ADS8168 ADC (over single- or dual-SDO SPI bus) and the EEPROM (over $I^2C$). The EEPROM comes pre-programmed with the information required to configure and initialize the ADS8168EVM-PDK platform. Once the hardware is initialized, the EEPROM is no longer used.

## 3.1 ADS8168 Digital Interface

The ADS8168EVM-PDK supports SPI and Multi-SPI serial digital interface as detailed in *ADS8168 8-Channel, 16-Bit, 1-MSPS SAR ADC With Easy to Drive Analog Inputs* . The PHI controller is configured to operate at a 3.3-V logic level and is directly connected to the digital I/O lines of the ADC. The digital interface configuration can be selected by navigating to the *ADS8168EVM Interface Configuration Settings* Tab in the GUI. For more information, see Section 6.1.

Connector J4 provides the digital I/O connections between the ADS8168EVM board and the PHI controller.

Table 2 summarizes the pin-outs for connector J4.

**Table 2. Digital I/O Connections for Connector J4**

| Pin Number | Signal | Description |
|---|---|---|
| J4.1 | EVM_REG_5V5 | Regulated 5.5 V |
| J4.2, J4.4 | EVM_RAW_5V | Power directly from host USB port |
| J4.16 | RESET | Resets ADS8168 (active low) |
| J4.18 | SDI | Serial data in |
| J4.22 | nCS | Active-low chip select |
| J4.24 | SCLK | Serial data clock |
| J4.28 | SCLK_RET | Data capture serial data clock |
| J4.30, J4.32, J4.34 | RVS | Multifunction signal. When nCS is low, this signal reflects conversion status. |
| J4.38 | SDO-0 | Serial data out |
| J4.40 | SDO-1 | Serial data out |
| J4.42 | Alarm | Output of digital comparator |
| J4.3, J4.60 | GND | Ground connections |
| J4.50 | EVM_DVdd | Power for interface |
| J4.56 | EVM_ID_SDA | SDA for EEPROM |
| J4.58 | EVM_ID_SCL | SCL for EEPROM |
| J4.59 | ID_POWER | Power supply used only to power the EEPROM (U3) in the EVM board |

## 4 Power Supplies

The ADS8168 ADC analog supply ($AV_{DD}$) is provided by a low-noise linear regulator (TPS7A4700). The regulator uses a 5.5-V supply out of a switching regulator from the PHI controller to generate a quiet and stable 5.3-V supply output. The 3.3-V supply to the digital supply of the ADS8168 is provided directly by an LDO from the PHI controller. The power supply for each active component on the EVM is bypassed with a ceramic capacitor placed close to that component. Additionally, the EVM layout uses thick traces or large copper filled areas, where possible, between bypass capacitors and their loads to minimize inductance along the load current path.

**CAUTION**

In default configuration, the ADS8168EVM is designed to be used in conjunction with the PHI controller, and in this configuration, all required voltages are supplied. Do not apply external power sources to the EVM while in its default configuration.

**CAUTION**

If external power supply sources are connected, ensure that modifications are performed according to Table 3.

**Table 3. Required Modifications for External Power Connection**

| External Supply | Default Voltage | Connection Location | Required Modification |
|---|---|---|---|
| $AV_{DD}$ | 5.3 V | P1.1 | Remove R18, labeled "AVdd" |
| GND | 0 V | P1.2, P1.5 | None |
| $AV_{SS}$ | 0 V | P1.3 | Remove R10, labeled "AVss" |
| 5.5 V | 5.5 V | P1.4 | Remove R5, labeled "5.5V" |
| DVdd | 3.3 V | P1.6 | Remove R2, labeled "DVdd" |

- 5.5 V is only used for developing $AV_{DD}$, via U2. If external $AV_{DD}$ is applied, the 5.5-V voltage node is not necessary. Apply a minimum of $AV_{DD}$ + 0.2 V, and Do not exceed the rated maximum for U2, TPS7A4700.
- $AV_{DD}$ is the positive rail for the input driver amplifiers and the ADC driver amplifiers and for the ADS8168. Use caution not to exceed the maximum rated voltage for these components, taking into account the value of $AV_{SS}$.
- If an external reference is used for the ADS8168, $AV_{DD}$ must be 0.2 V higher than the external reference for proper operation of the internal reference buffer of the ADS8168.
- $AV_{SS}$ is used as the negative rail for the input amplifiers and the ADC driver amplifiers. $AV_{SS}$ can be set to a small negative voltage value in order to allow the amplifiers to drive a signal to a true zero-volt value.
- $AV_{SS}$ should be limited to $AV_{DD}$ – 5.5 V (nominally, 200 mV) to protect the OPA350 circuits onboard.

# 5 ADS8168EVM_PDK Initial Setup

This section explains the initial hardware and software setup procedure that must be completed for the proper operation of the ADS8168EVM-PDK.

## 5.1 Default Jumper Settings

Jumper JP2 selects the voltage level to be applied to the AIN-COM pin on the ADS8168. The default position is between pins 1-2, applying GND to the AIN-COM. Other options are Ref/2 (3-4), or an external connection (5-6). In default configuration, no other jumpers are necessary.

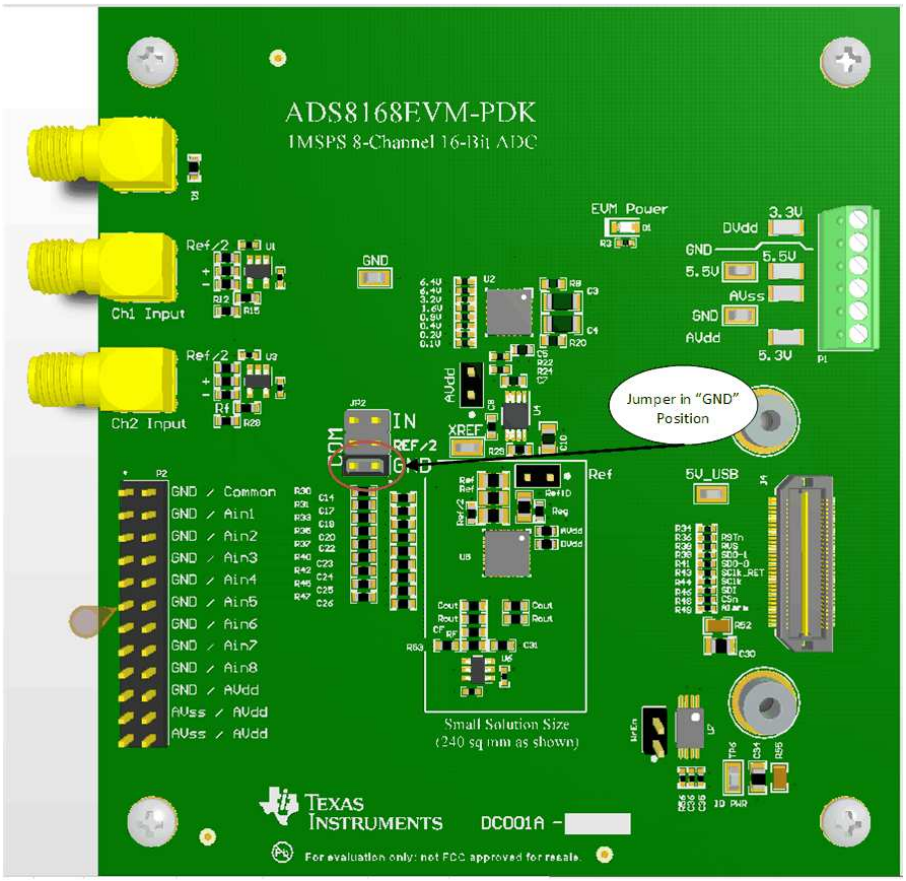



**Figure 4. ADS8168EVM Default Jumper Settings**

**Table 4. Jumper Configuration Details**

| Jumper | Function | Default Position | Description |
|---|---|---|---|
| JP1 | $AV_{DD}$ | Open | Connects $AV_{DD}$ to U4, a REF5050 5-V reference |
| JP2 | COM | GND | Applies voltage to AIN-COM |
| JP3 | Ref | Open | Connects external reference to the ADS8168 REFIO pin |
| JP4 | WrEn | Open | Enables writing EVM identification information to the onboard EEPROM |

**CAUTION**

ADS8168EVM Default JumperConfiguration

## 5.2 EVM Graphical User Interface (GUI) Software Installation

Download the latest version of the EVM GUI installer from the Tools and Software folder of the ADS8168EVM-PDK and run the GUI installer to install the EVM GUI software. The user must have administrator privileges on the PC to be able to install the EVM software. The following steps list the directions to install the software

**CAUTION**

It may be necessary to manually disable any anti-virus software running on the computer before downloading the EVM GUI installer onto the local hard disk. Otherwise, depending on the anti-virus settings, an error message may appear or the *installer.exe* file may be deleted.

Step 1. Download the latest version of the installer from the Tools and Software folder of the ADS8168 and run the GUI installer. Accept the license agreements and follow the on-screen instructions to complete the installation.


**Figure 5. Software Installation Prompts**

Step 2. As a part of the ADS8168 EVM GUI installation, a prompt with a *Device Driver Installation* will appear on the screen. Click *Next* to proceed.

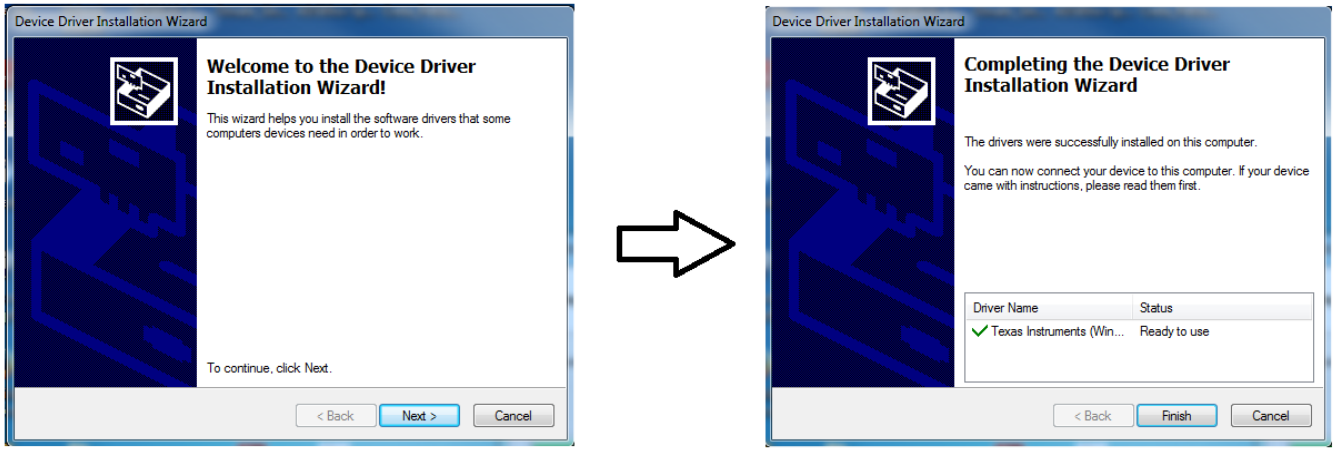



**Figure 6. ADS8168 Device Driver Installation Wizard Prompts**

**NOTE:** A notice may appear on the screen stating that Widows cannot verify the publisher of this driver software. Select *Install this driver software anyway*.

Step 3. The ADS8168EVM-PDK requires LabVIEW™ Run-Time Engine may prompt for the installation of this software, if not already installed.

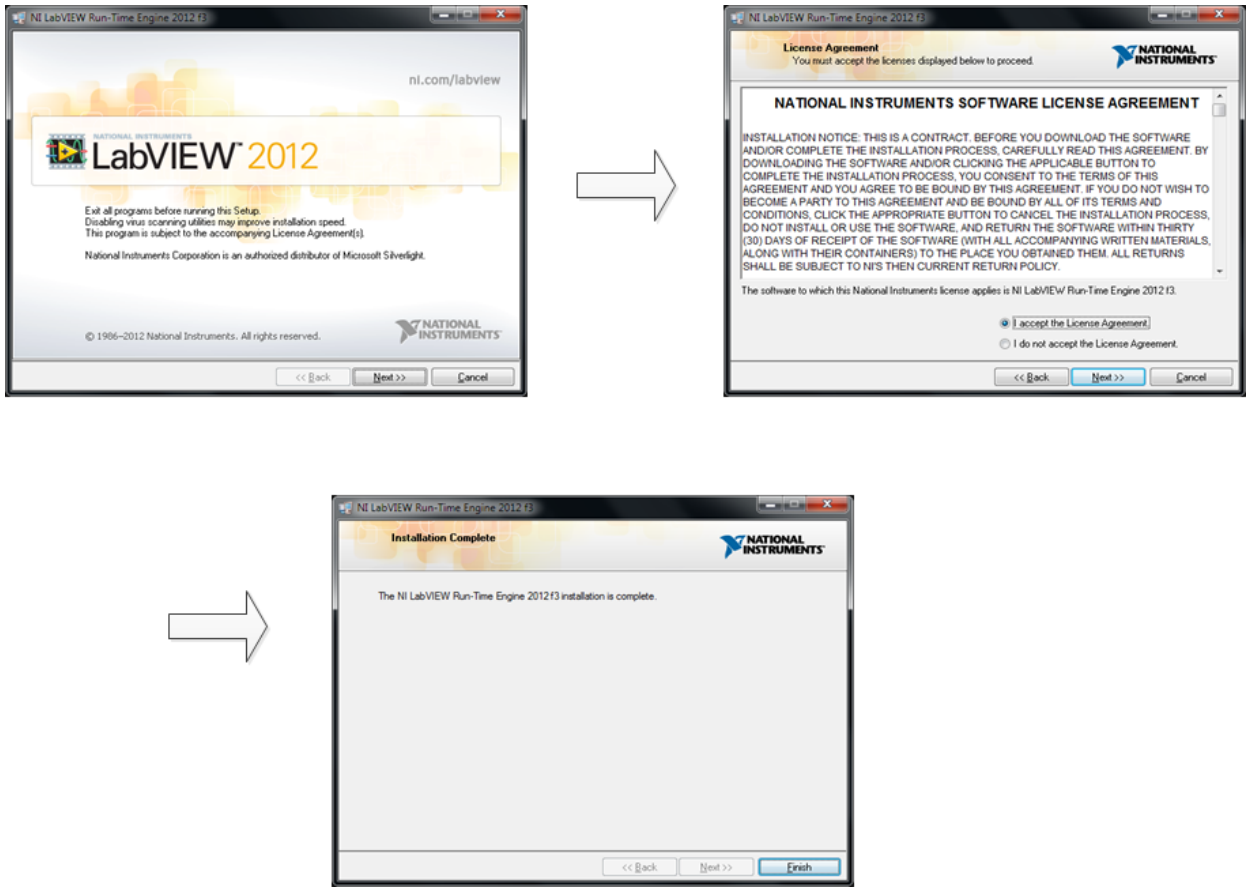



**Figure 7. LabVIEW Run-Time Engine Installation**

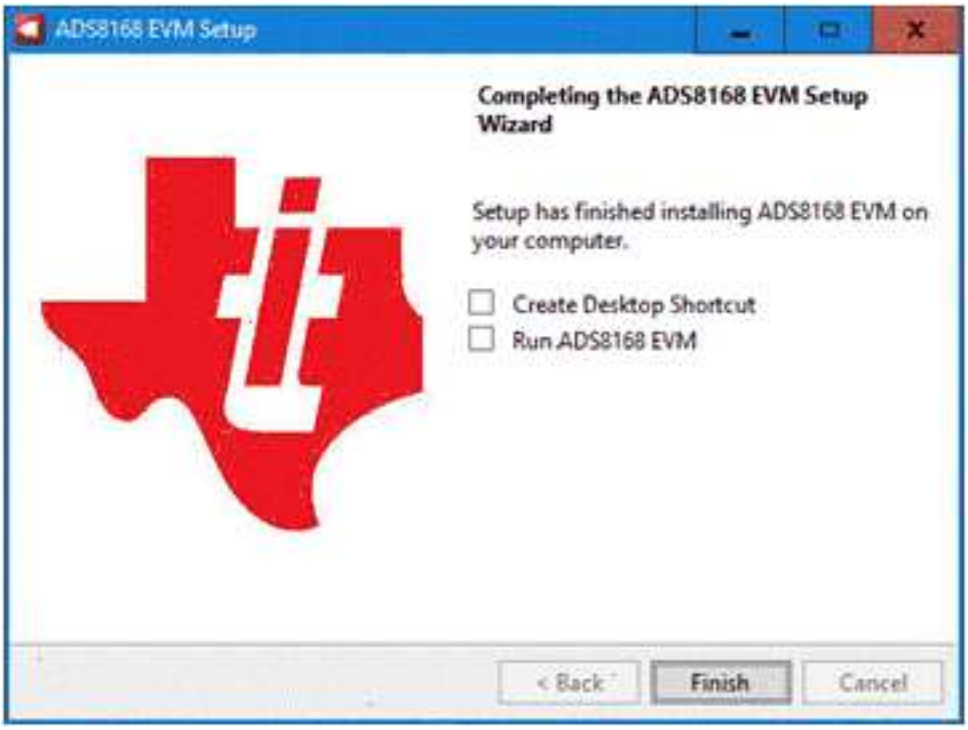



**Figure 8. ADS8168EVM Successful Installation Complete**

Step 4. After these installations, verify that C:\Program Files (x86)\Texas Instruments\ADS8168 EVM is as shown in Figure 9.

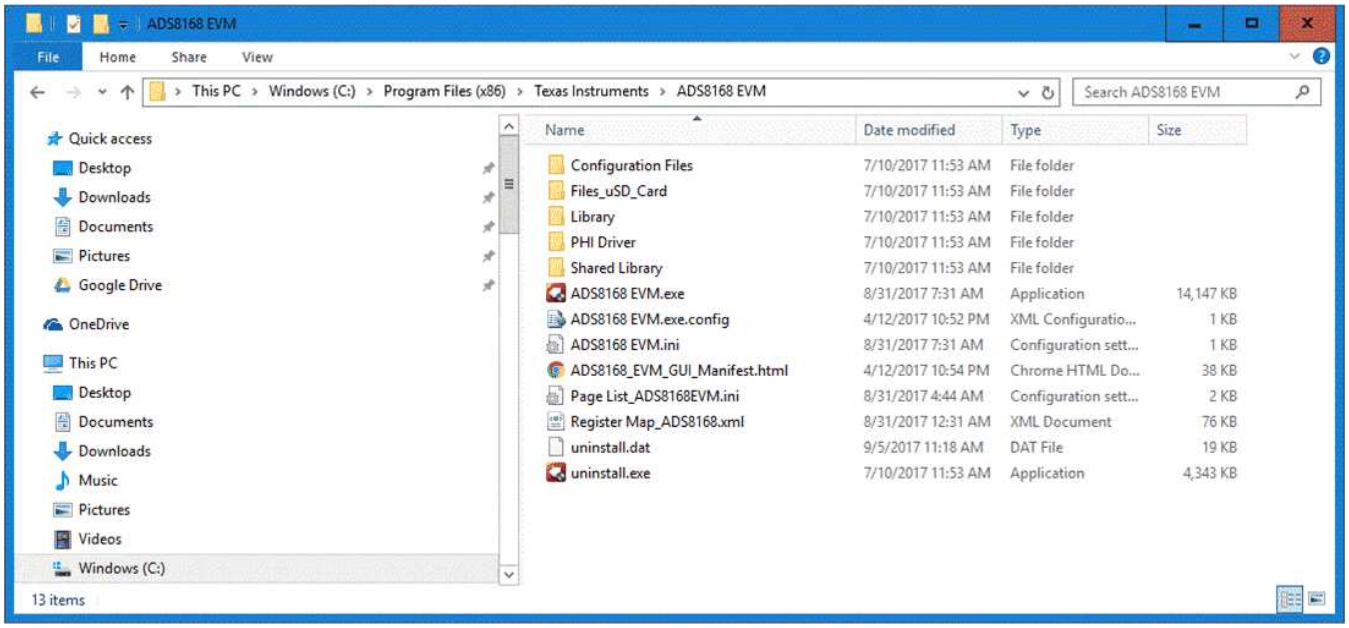



**Figure 9. ADS8168 EVM Folder Post-Installation**

# 6 ADS8168EVM-PDK Operation

The following instructions are a step-by-step guide to connecting the ADS8168 to the computer and evaluating the performance of the ADS8168:

1. Connect the ADS8168EVM to the PHI. Install the two screws as indicated in Figure 10.
2. Use the USB cable provided to connect the PHI to the computer.
    1. LED D5 on the PHI lights up, indicating that the PHI is powered up.
    2. LEDs D1 and D2 on the PHI starts blinking to indicate that the PHI is booted up and communicating with the PC. The resulting LED indicators are shown in Figure 10.

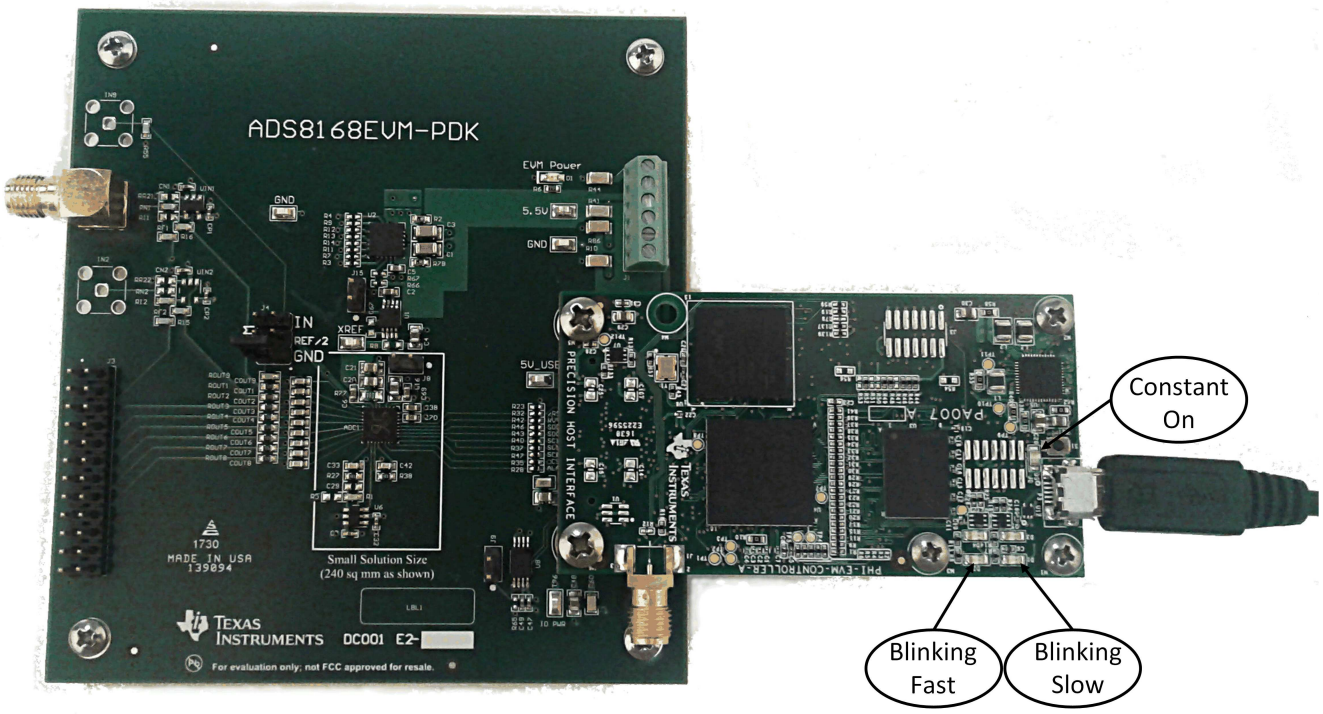



**Figure 10. ADS8168EVM-PDK Hardware Setup and LED Indicators**

3. Double click on the ADS8168 EVM.exe file to launch the EVM GUI, as shown in Figure 11.

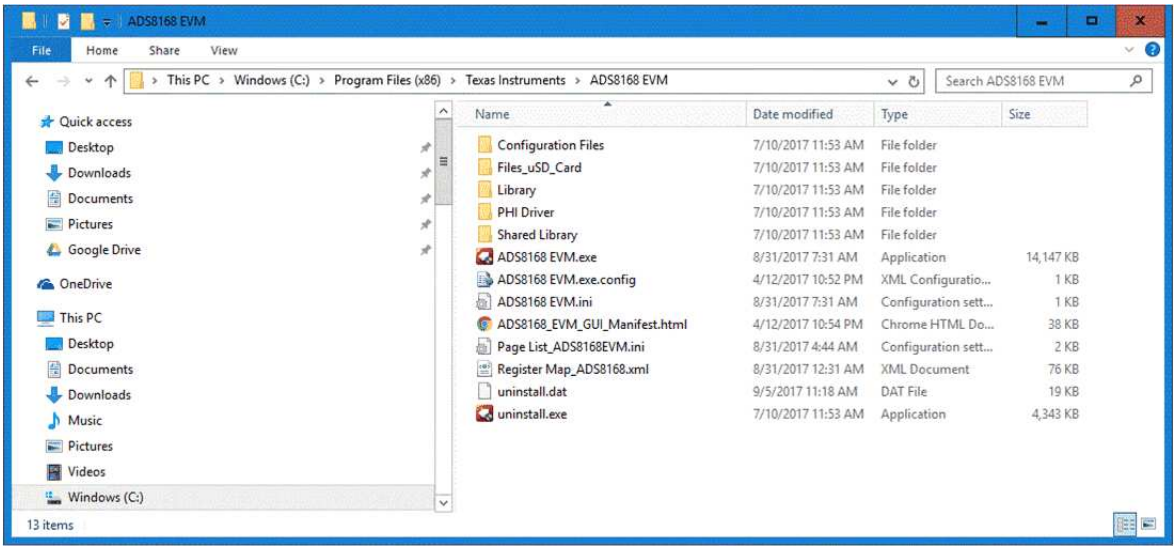



**Figure 11. Launch the ADS8168EVM GUI Software**

## 6.1 EVM GUI Global Settings for ADC Control

Although the EVM GUI does not allow direct access to the voltage levels and timing configuration of the ADC digital interface, the EVM GUI provide users high-level control over the various interface modes and frequencies of the ADS8168, as well as the capture and multiplexer sequencing options. In addition, the EVM GUI provides full low-level control of all register settings.

Figure 12 shows the *Device Configuration* page, through which various functions of the ADS8168 are exercised. These are global settings, and they persist across the different GUI tools or GUI pages listed in the top left plane. The software defaults to operating the ADS8168 in *Manual Mode*, sampling Channel 0 at 1 MSPS. The digital interface defaults to operating the SCLK at 15 MHz.

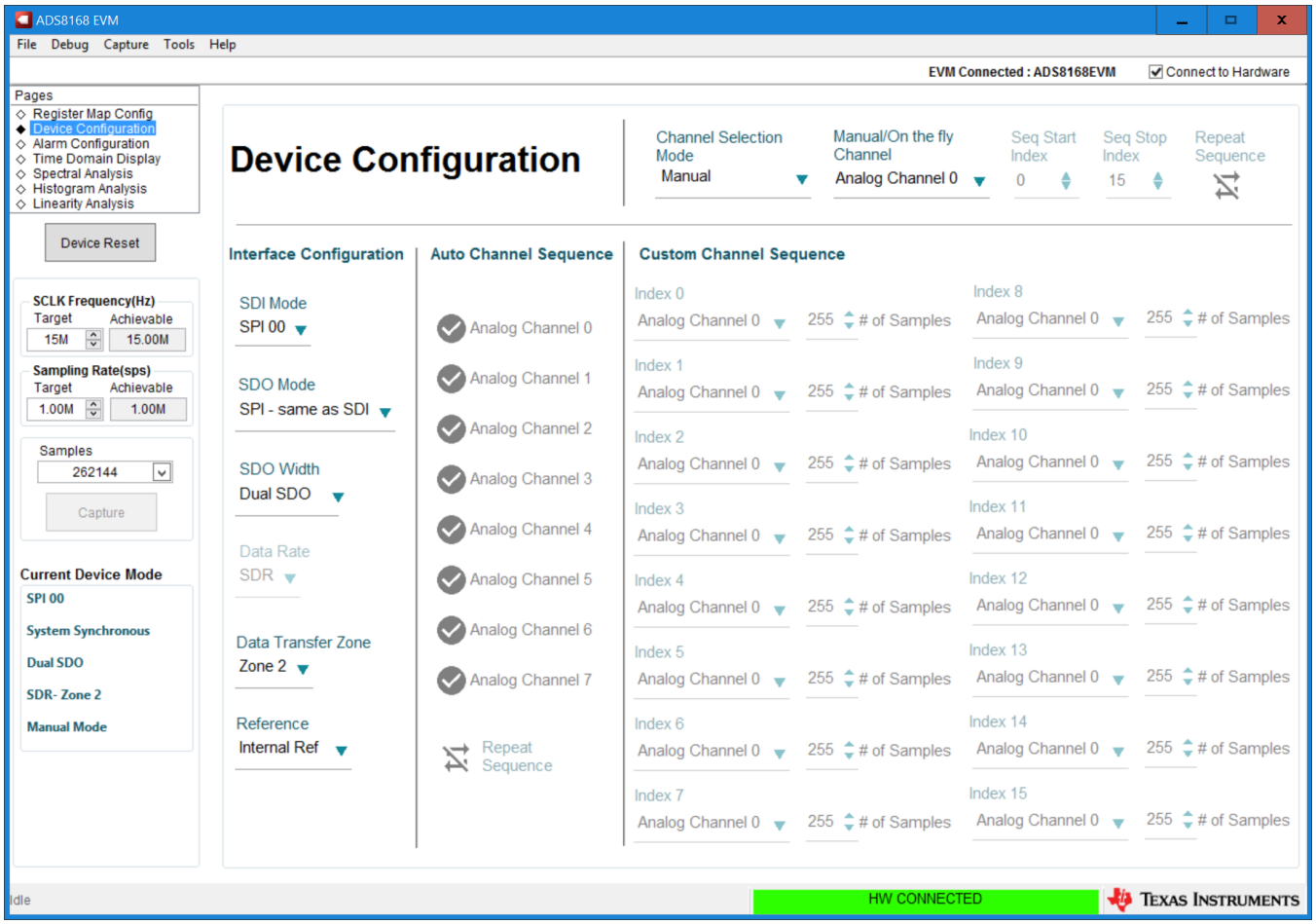



**Figure 12. EVM GUI Global Input Parameters**

Independent of the interface configuration, the user can specify a target SCLK frequency and sampling frequency (in Hz) and the GUI tries to match this frequency as closely as possible by changing the PHI PLL settings. The achievable frequencies can differ from the target value displayed. Achievable frequencies are limited by the various interface modes, and the ADS8168 provide options which allow a very low SCLK. This pane allows the user to try various settings available on the ADS8168 in an iterative fashion until the user converges to the best settings for the corresponding test scenario.

The *Device Reset* button in the GUI functions as a Master RESET to both the ADS8168 EVM and the GUI. When the button is pressed, the ADC RESETs to the default settings shown in Figure 12

## 6.2 Time Domain Display Tool

The time domain display tool allows visualization of the time domain conversion results given a set of analog input signals.

If multiple channels are selected, all data is plotted on the same display; however, the user can selectively display captured data by using the check-box interface on the right.

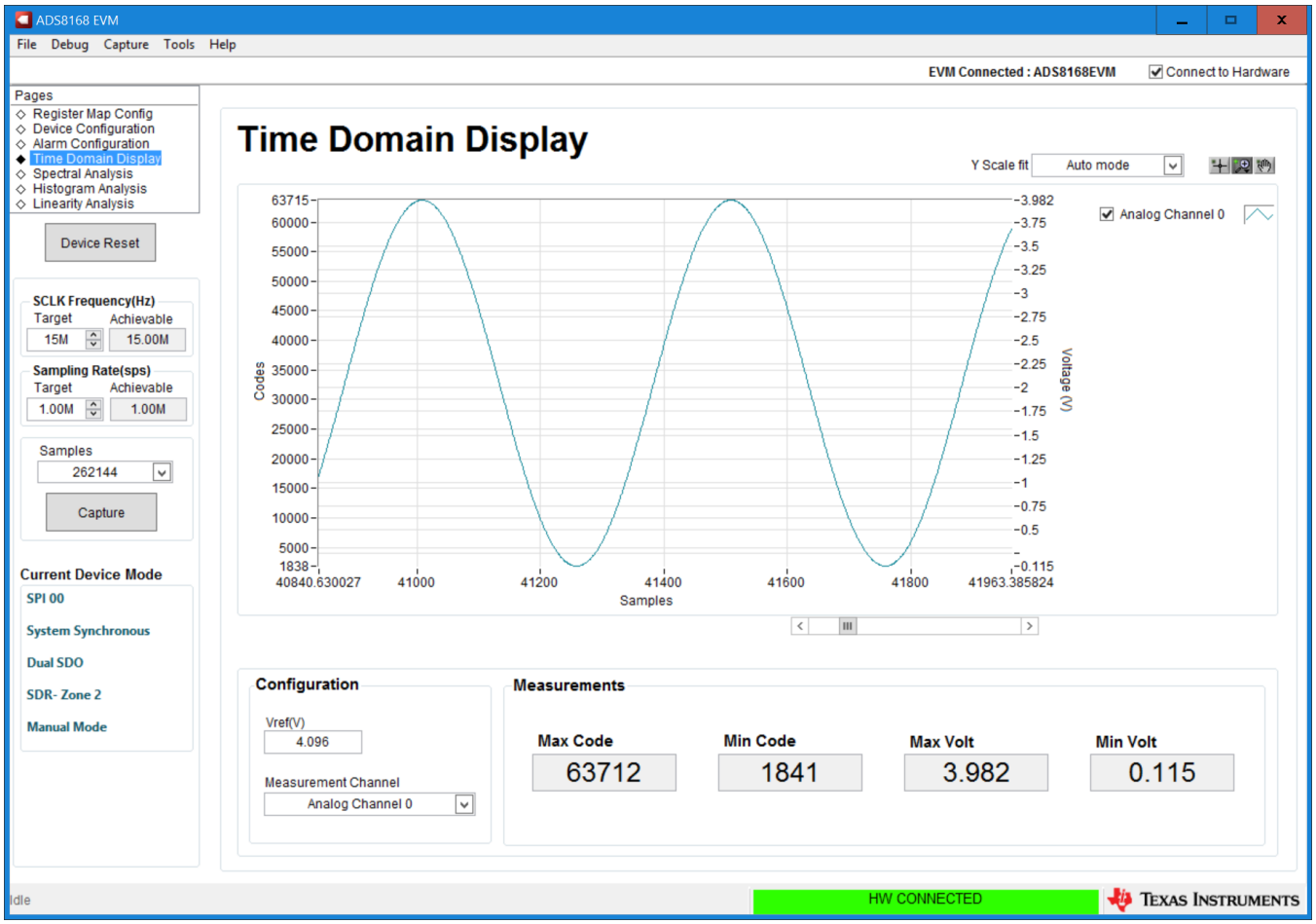



**Figure 13. Time Domain Display**

## 6.3 Spectral Analysis Tool

The spectral analysis tool is intended to evaluate the dynamic performance (SNR, THD, SFDR, SINAD, and ENOB) of ADS8168 SAR ADC through single-tone sinusoidal signal FFT analysis using the 7-term Blackman-Harris window setting.

For dynamic performance evaluation, the external differential source must have better specifications than the ADS8168 itself to ensure that the measured system performance is not limited by the performance of the signal source. Therefore, the external reference source must meet the source requirements mentioned in Table 5.

**Table 5. External Source Requirements for Evaluation of the ADS8168**

| Specification Description | Specification Value |
|---|---|
| Signal frequency | 2 kHz |
| External source type | Single ended |
| External source common-mode | Vref/2, nominally 2.048 V |
| Maximum noise | 14.5 $\mu V_{RMS}$ |
| Minimum SNR | 100 dB |
| Maximum THD | –110 dB |

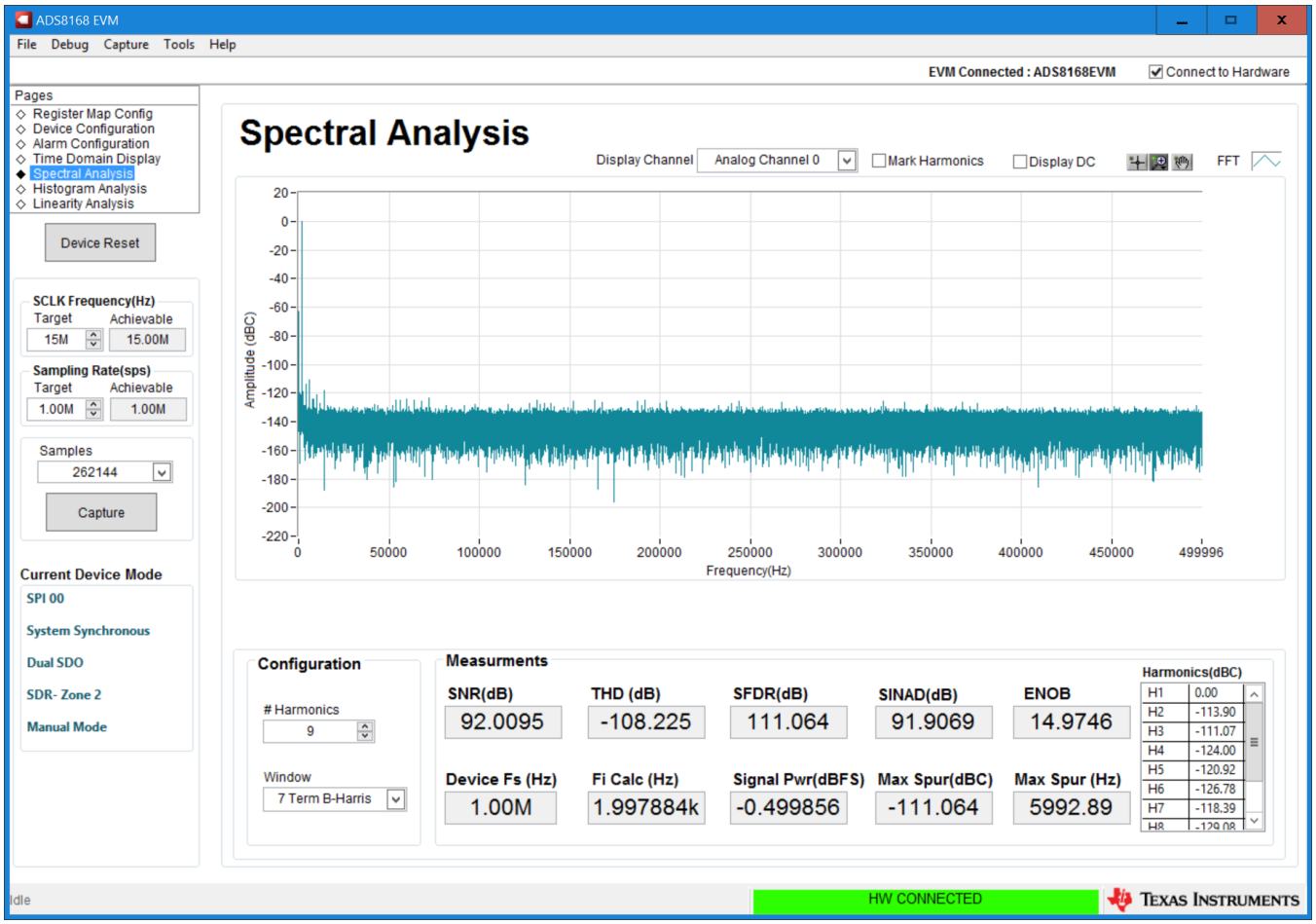



**Figure 14. Spectral Analysis Tool**

Finally, the FFT tool includes windowing options that are required to mitigate the effects of non-coherent sampling (this discussion is beyond the scope of this document). The 7-Term Blackman Harris window is the default option and has sufficient dynamic range to resolve the frequency components of up to a 24-bit ADC. Note that the *None* option corresponds to not using a window (or using a rectangular window) and is not recommended.

## 6.4 Histogram Tool

Noise degrades ADC resolution and the histogram tool can be used to estimate *effective resolution*, which is an indicator of the number of bits of ADC resolution losses resulting from noise generated by the various sources connected to the ADC when measuring a dc signal. The cumulative effect of noise coupling to the ADC output from sources such as the input drive circuits, the reference drive circuit, the ADC power supply, and the ADC itself is reflected in the standard deviation of the ADC output code histogram that is obtained by performing multiple conversions of a dc input applied to a given channel.

The histogram corresponding to a dc input is displayed after clicking the **Capture** button, as shown in Figure 15:

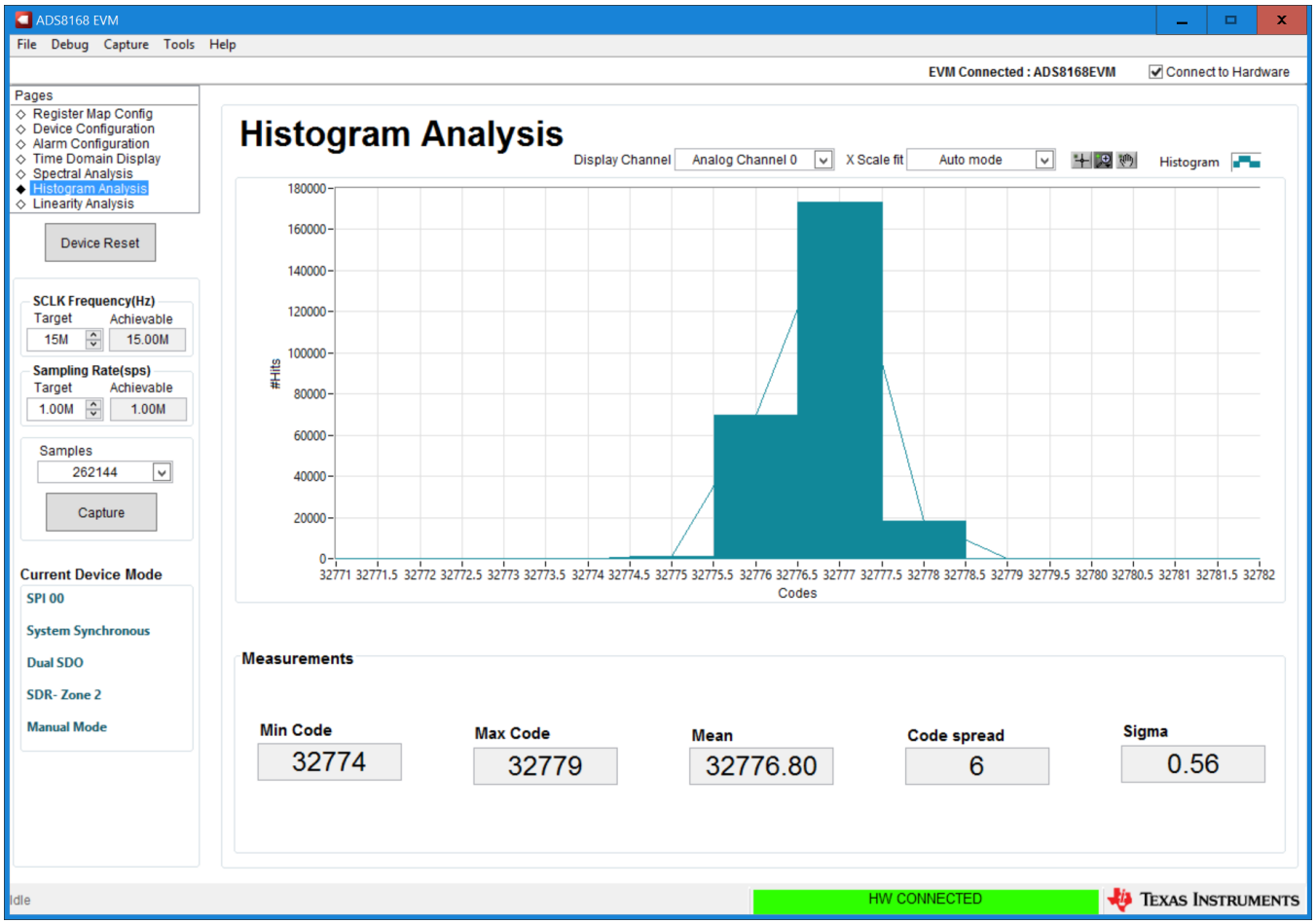



**Figure 15. Histogram Analysis Tool**

## 6.5 Linearity Analysis Tool

The linearity analysis tool measures and generates the performance DNL and INL plots over code for the ADS8168. A 2-kHz sinusoidal input signal is required, which is ideally slightly saturated (100–200 mV outside the full-scale range) with very low distortion. Because the input circuits on the ADS8168 EVM in their default power configuration do not allow a saturated signal on the negative rail, the linearity algorithm attempts to report the performance of the codes of the ADC which could be adequately tested. It should be noted that the results of this test include the nonlinearities of the external signal source, the multiplexer drive amplifier (if used), and the ADC driver amplifier. For this reason, the external source linearity must be better than the ADC linearity. To make sure that the DNL and INL of the ADC are correctly measured, the external source must meet the requirements in Table 6.

**Table 6. External Source Requirements for ADS8168 Evaluation**

| Specification Description | Specification Value |
|---|---|
| Signal frequency | 2 kHz |
| External source type | Single ended, referred to GND |
| External source common mode | Vref/2, nominally 2.048 V |
| Signal amplitude | Vref/2(Vp) + 100 mVp |
| Maximum noise | 14.5 $\mu V_{RMS}$ |
| Maximum SNR | 100 dB |
| Maximum THD | –110 dB |

The number-of-hits setting depends on the external noise source. For a 100-dB SNR external source with approximately 30 µVrms of noise, total number of hits must be 256.

**NOTE:** This analysis can take a couple of minutes to run and the evaluation board must remain undisturbed during the complete duration of the analysis.

Figure 16 shows the linearity analysis tool dialog window.


**Figure 16. Linearity Analysis Tool**

# 7 Bill of Materials, PCB Layout, and Schematics

This section contains the ADS8168 EVM bill of materials, PCB layout, and the EVM schematics.

## 7.1 Bill of Materials

Table 7 lists the ADS8168 EVM BOM

**Table 7. ADS8168EVM-PDK Bill of Materials**

| Part Number | Quantity | Designator | Value | Manufacturer | Description |
|---|---|---|---|---|---|
| PHI-EVM-CONTROLLER (Edge# 6591636 rev. B) | 1 | N/A | | Texas Instruments | USB Controller Board for ADC EVMs (Kit Item) |
| DC001 | 1 | N/A | | Any | Printed Circuit Board |
| GRM155R71C104KA88D | 8 | C1, C2, C6, C8, C32, C33, C35, C36 | 0.1uF | Murata | CAP, CERM, 0.1 uF, 16 V, +/- 10%, X7R, 0402 |
| C3216JB1E476M160AC | 2 | C3, C4 | 47uF | TDK | CAP, CERM, 47 uF, 25 V, +/- 20%, JB, 1206 |
| GRM188R71E105KA12D | 7 | C5, C7, C9, C15, C16, C19, C21 | 1uF | Murata | CAP, CERM, 1 uF, 25 V, +/- 10%, X7R, 0603 |
| GRM21BR71A106KE51L | 6 | C10, C11, C12, C13, C30, C34 | 10uF | Murata | CAP, CERM, 10 uF, 10 V, +/- 10%, X7R, 0805 |
| C0603C561J5GACTU | 9 | C14, C17, C18, C20, C22, C23, C24, C25, C26 | 560pF | Kemet | CAP, CERM, 560 pF, 50 V, +/- 5%, C0G/NP0, 0603 |
| GRM1885C1H122JA01D | 2 | C27, C28 | 1200pF | Murata | CAP, CERM, 1200 pF, 50 V, +/- 5%, C0G/NP0, 0603 |
| 06035A101FAT2A | 1 | C31 | 100pF | AVX | CAP, CERM, 100 pF, 50 V, +/- 1%, C0G/NP0, 0603 |
| 150080VS75000 | 1 | D1 | Bright Green | Wurth Elektronik | LED, Bright Green, SMD |
| PMSSS 440 0025 PH | 4 | H1, H2, H5, H6 | | B&F Fastener Supply | MACHINE SCREW PAN PHILLIPS 4-40 |
| 9774050360R | 2 | H3, H4 | | Wurth Elektronik | ROUND STANDOFF M3 STEEL 5MM |
| 1891 | 4 | H7, H8, H9, H10 | | Keystone | Hex Standoff, #4-40, Aluminum, 1/4" |
| RM3X4MM 2701 | 2 | H11, H13 | | APM HEXSEAL | Machine Screw Pan PHILLIPS M3 |
| 901-143-6RFX | 1 | J2 | | Amphenol RF | JACK, SMA, 50 Ohm, Gold, R/A, TH |
| QTH-030-01-L-D-A | 1 | J4 | | Samtec | Header(Shrouded), 19.7mil, 30x2, Gold, SMT |
| 5-146261-1 | 3 | JP1, JP3, JP4 | | TE Connectivity | Header, 100mil, 2x1, Gold, TH |
| PBC03DAAN | 1 | JP2 | | Sullins Connector Solutions | Header, 100mil, 3x2, Gold, TH |
| 1725698 | 1 | P1 | | Phoenix Contact | Terminal Block, 6x1, 2.54mm, TH |
| TSW-112-07-G-D | 1 | P2 | | Samtec | Header, 100mil, 12x2, Gold, TH |
| MCT06030Z0000ZP500 | 9 | R1, R6, R12, R15, R25, R27, R28, R30, R54 | 0 | Vishay/Beyschlag | RES, 0, 5%, 0.125 W, 0603 |
| 5108 | 4 | R2, R5, R10, R18 | 0 | Keystone | RES, 0, 1%, 0.5 W, 1206 |

**Table 7. ADS8168EVM-PDK Bill of Materials (continued)**

| Part Number | Quantity | Designator | Value | Manufacturer | Description |
|---|---|---|---|---|---|
| CRCW04022K70JNED | 1 | R3 | 2.7k | Vishay-Dale | RES, 2.7 k, 5%, 0.063 W, 0402 |
| ERJ-3RSFR10V | 2 | R8, R20 | 0.1 | Panasonic | RES, 0.1, 1%, 0.1 W, 0603 |
| RC0402JR-070RL | 14 | R13, R17, R19, R21, R24, R36, R38, R39, R41, R43, R44, R46, R48, R49 | 0 | Yageo America | RES, 0, 5%, 0.063 W, 0402 |
| ERJ-3RQFR22V | 1 | R29 | 0.22 | Panasonic | RES, 0.22, 1%, 0.1 W, 0603 |
| RT0603BRD07107RL | 8 | R31, R33, R35, R37, R40, R42, R45, R47 | 107 | Yageo America | RES, 107, 0.1%, 0.1 W, 0603 |
| CRCW08051R00FKEA | 1 | R32 | 1.00 | Vishay-Dale | RES, 1.00, 1%, 0.125 W, 0805 |
| ERJ-2RKF1002X | 2 | R34, R56 | 10.0k | Panasonic | RES, 10.0 k, 1%, 0.1 W, 0402 |
| RT0603BRD0749R9L | 2 | R50, R51 | 49.9 | Yageo America | RES, 49.9, 0.1%, 0.1 W, 0603 |
| 5106 | 2 | R52, R55 | 0 | Keystone | RES, 0, 1%, 0.5 W, 0805 |
| 60900213421 | 1 | SH-J1 | | Wurth Elektronik | Shunt, 2.54mm, Gold, Black |
| 5015 | 6 | TP1, TP2, TP3, TP4, TP5, TP6 | | Keystone | Test Point, Miniature, SMT |
| OPA320AIDBVR | 2 | U1, U6 | | Texas Instruments | Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br) |
| TPS7A4700RGWR | 1 | U2 | | Texas Instruments | 36-V, 1-A, 4.17-uVRMS, RF LDO Voltage Regulator, RGW0020A (VQFN-20) |
| REF5050AIDGKT | 1 | U4 | | Texas Instruments | Low Noise, Very Low Drift, Precision Voltage Reference, -40 to 125 degC, 8-pin VSSOP (DGK), Green (RoHS & no Sb/Br) |
| ADS8168IRHB | 1 | U5 | | Texas Instruments | ADS8168IRHB, RHB0032E (VQFN-32) |
| BR24G32FVT-3AGE2 | 1 | U7 | | Rohm | I2C BUS EEPROM (2-Wire), TSSOP-B8 |
| 06035A2R7CAT2A | 0 | C29 | 2.7pF | AVX | CAP, CERM, 2.7 pF, 50 V, +/- 9%, C0G/NP0, 0603 |
| N/A | 0 | FID1, FID2, FID3, FID4, FID5, FID6 | | N/A | Fiducial mark. There is nothing to buy or mount. |
| 102-1092-BL-00100 | 0 | H12 | | CNC Tech | CABLE USB A MALE-B MICRO MALE 1M (Kit Item) |
| 901-143-6RFX | 0 | J1, J3 | | Amphenol RF | JACK, SMA, 50 Ohm, Gold, R/A, TH |
| MCT06030Z0000ZP500 | 0 | R4, R9, R23, R26, R53 | 0 | Vishay/Beyschlag | RES, 0, 5%, 0.125 W, 0603 |
| RC0402JR-070RL | 0 | R7, R11, R14, R16, R22 | 0 | Yageo America | RES, 0, 5%, 0.063 W, 0402 |
| OPA320AIDBVR | 0 | U3 | | Texas Instruments | Precision, 20 MHz, 0.9 pA Ib, RRIO, CMOS Operational Amplifier, 1.8 to 5.5 V, -40 to 125 degC, 5-pin SOT23 (DBV5), Green (RoHS & no Sb/Br) |

## 7.2 PCB Layout

Figure 17 through Figure 21 illustrate the EVM PCB layout.

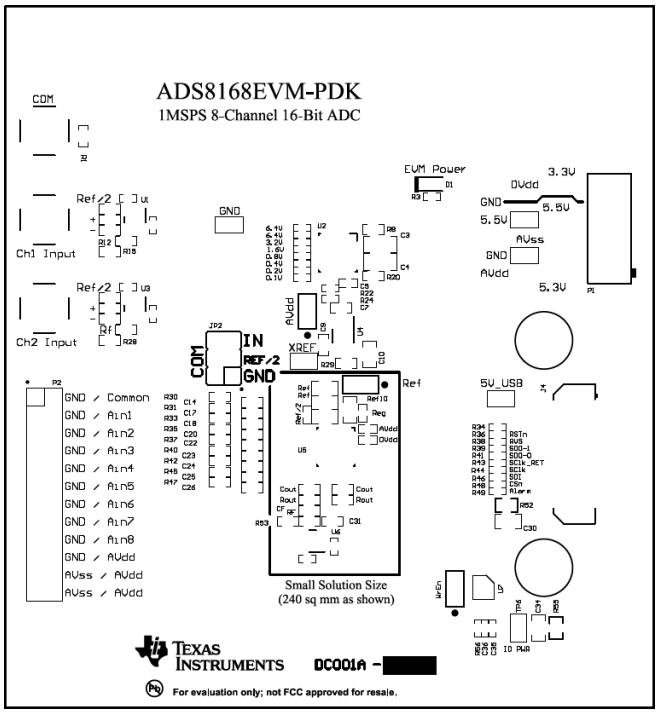



**Figure 17. ADS8168 EVM PCB: Top Overlay**

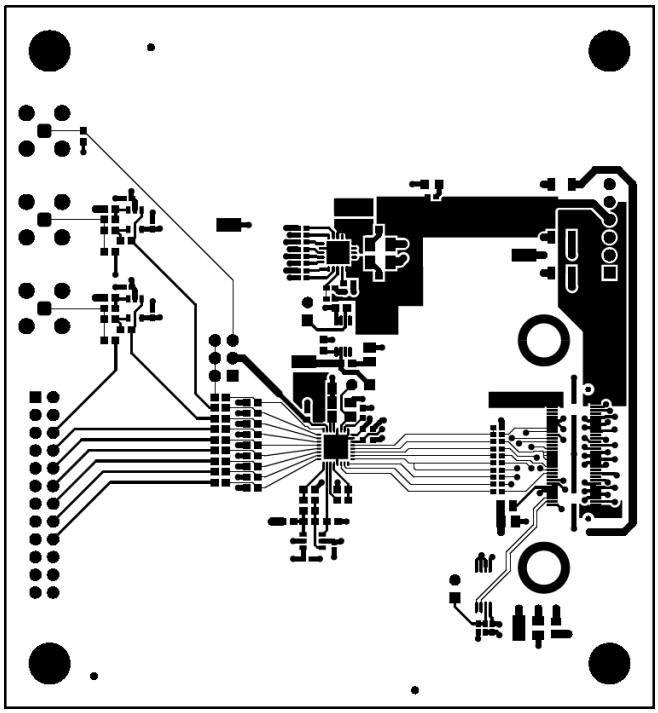


**Figure 18. ADS8168 EVM PCB Layer 1: Top Layer**

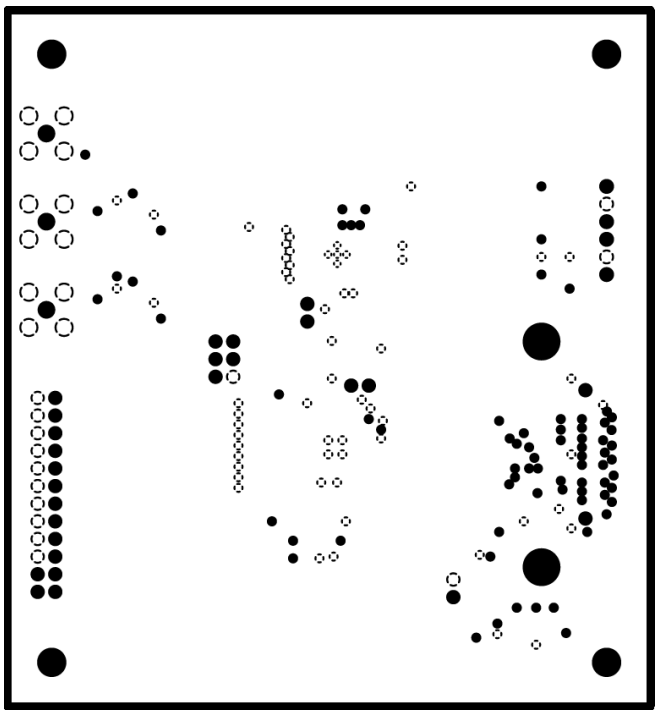


**Figure 19. ADS8168 EVM PCB Layer 2: GND Plane**

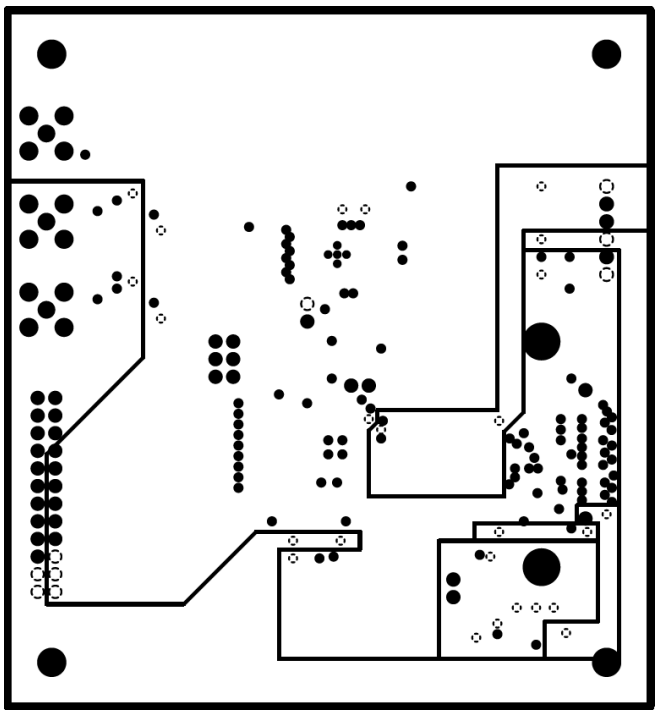


**Figure 20. ADS8168 EVM PCB Layer 3: Power Planes**

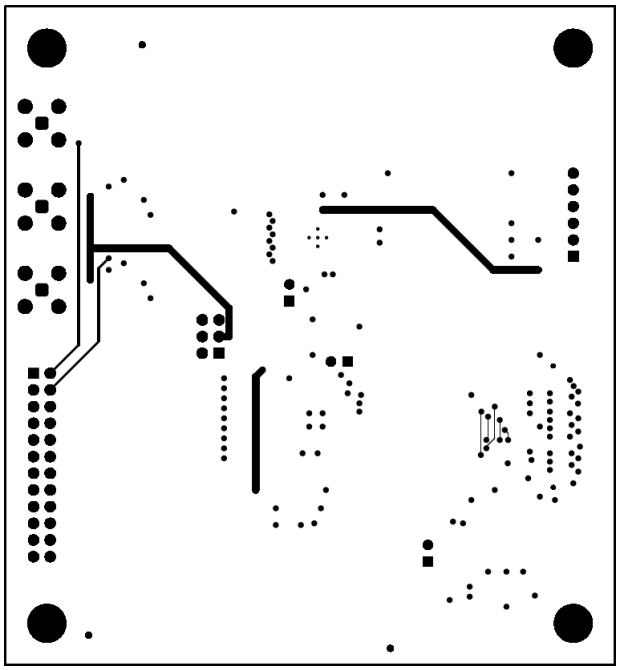


**Figure 21. ADS8168 EVM PCB Layer 4: Bottom Layer**

## 7.3 Schematics

Figure 22 through Figure 24 illustrate the EVM schematics.

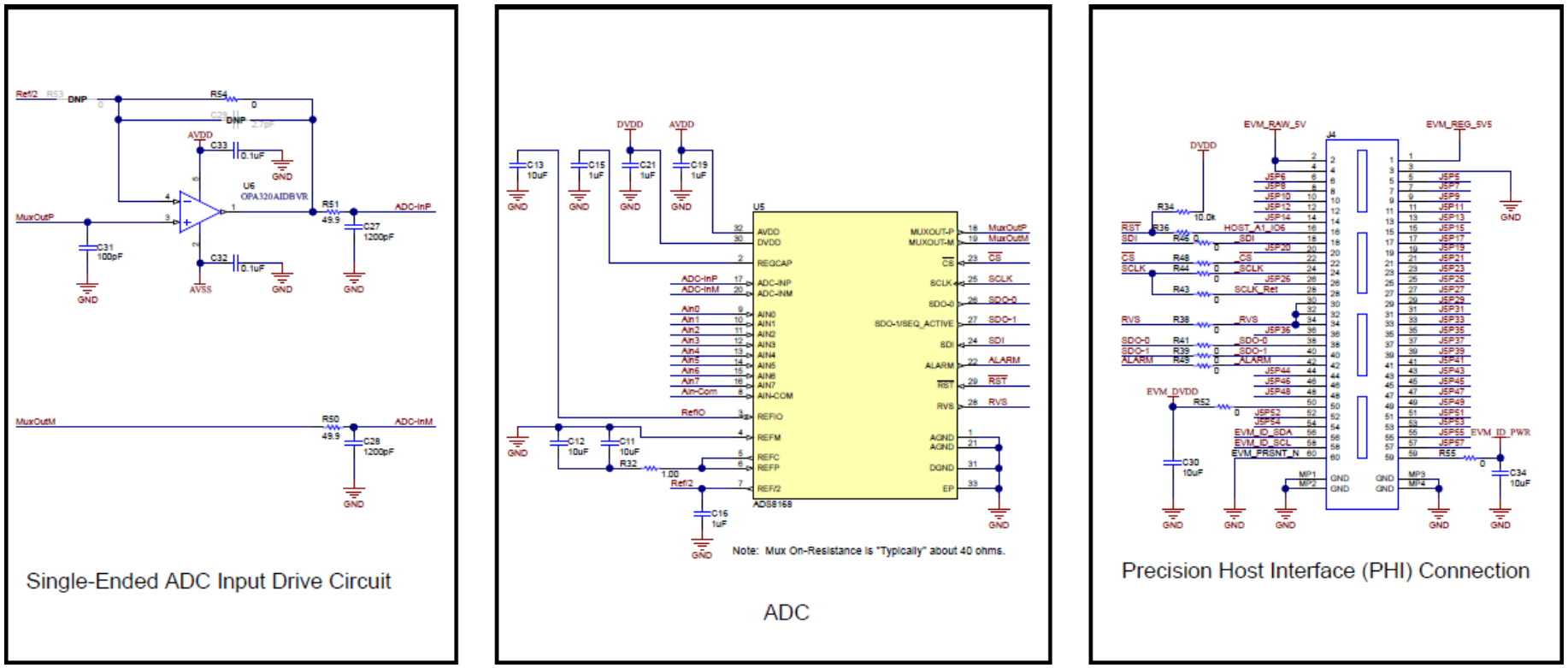



**Figure 22. ADS8588EVM-PDK Schematic**

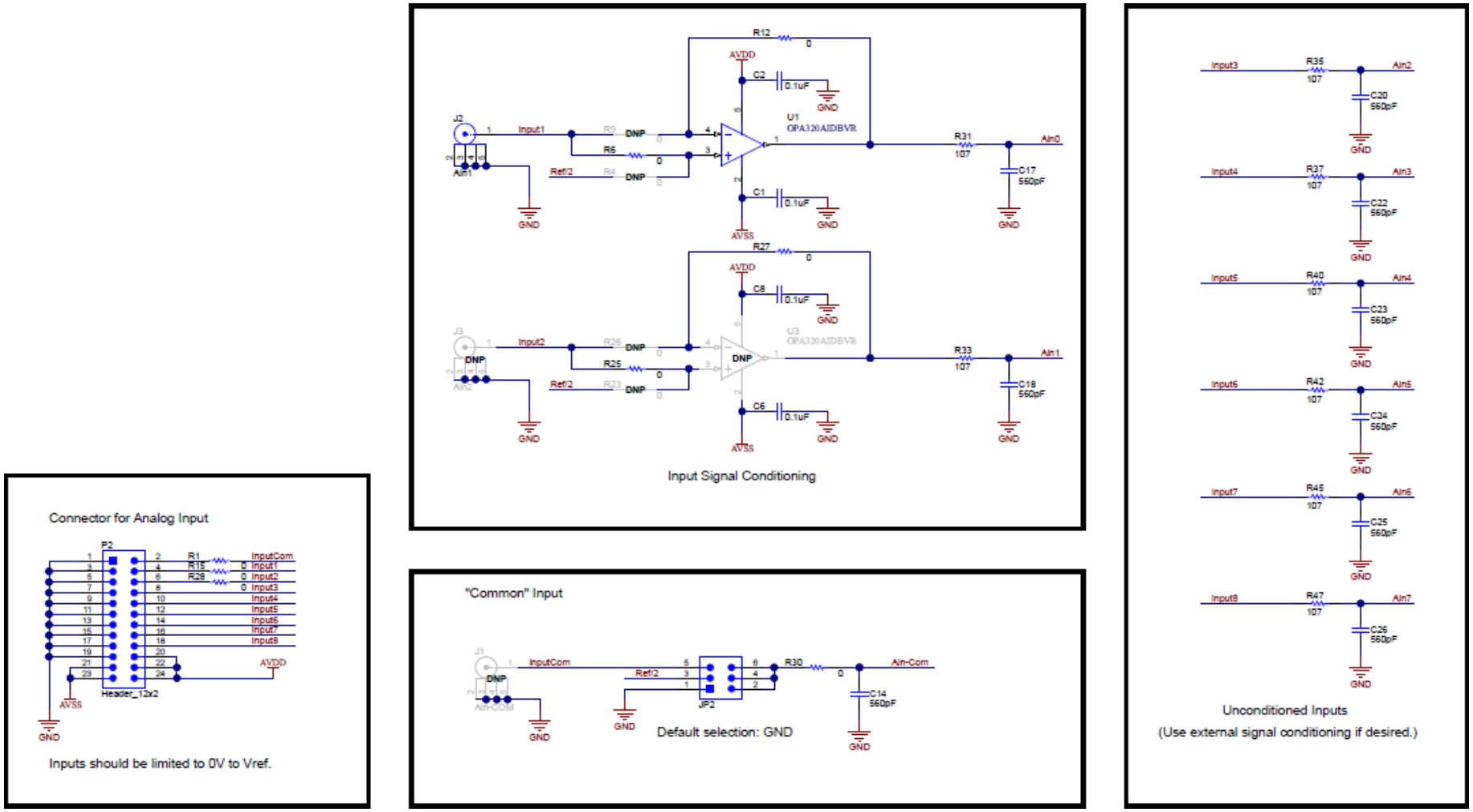



**Figure 23. ADS8588EVM-PDK Schematic**

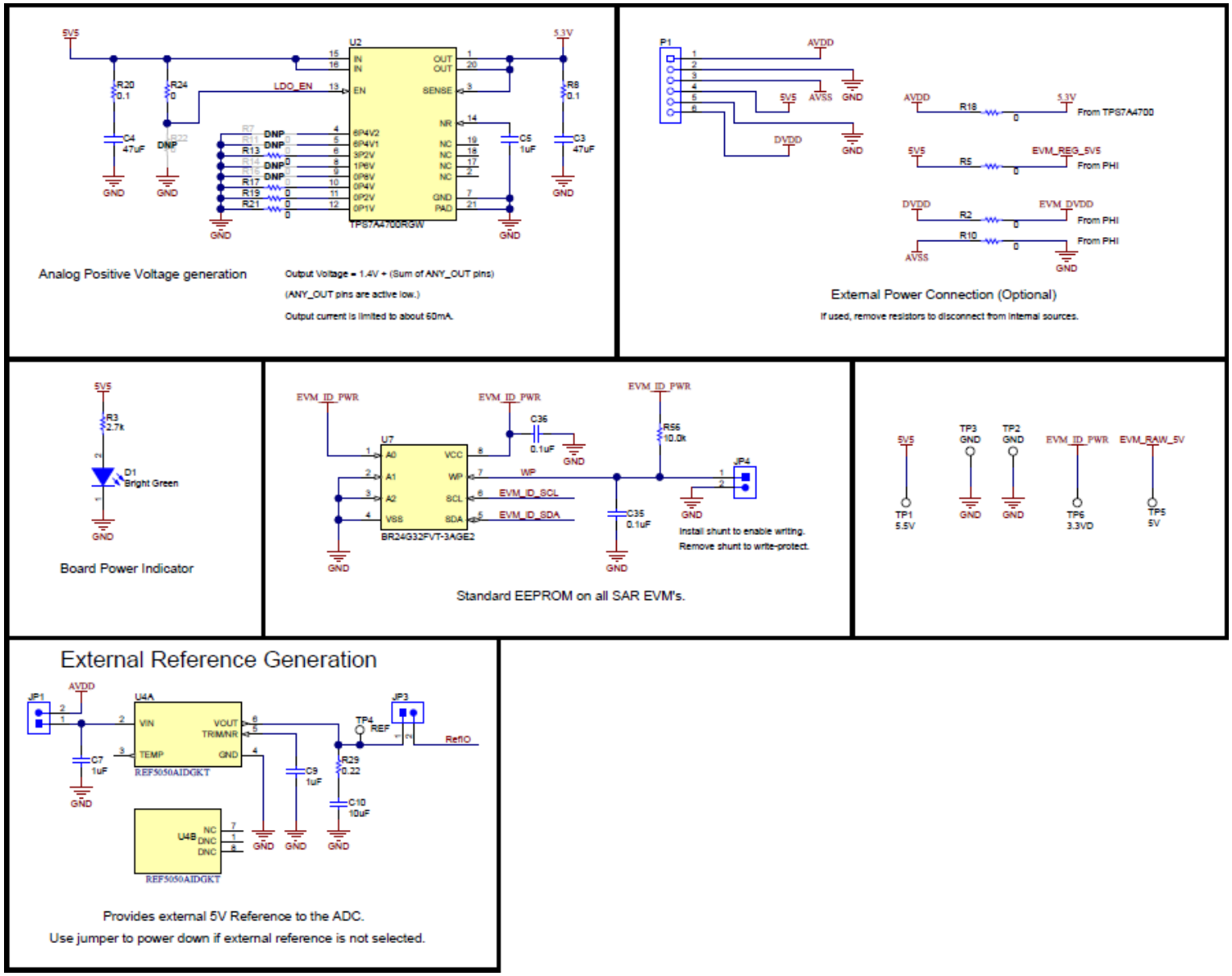



**Figure 24. ADS8588EVM-PDK Schematic**

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   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for a nonconforming EVM if (a) the nonconformity was caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI, (b) the nonconformity resulted from User's design, specifications or instructions for such EVMs or improper system design, or (c) User has not paid on time. Testing and other quality control techniques are used to the extent TI deems necessary. TI does not test all parameters of each EVM. User's claims against TI under this Section 2 are void if User fails to notify TI of any apparent defects in the EVMs within ten (10) business days after delivery, or of any hidden defects with ten (10) business days after the defect has been detected.

   2.3 TI's sole liability shall be at its option to repair or replace EVMs that fail to conform to the warranty set forth above, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      **FCC NOTICE:** This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      **CAUTION**

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      **FCC Interference Statement for Class A EVM devices**

      *NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.*

**FCC Interference Statement for Class B EVM devices**

*NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:*

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210 or RSS-247*

**Concerning EVMs Including Radio Transmitters:**

This device complies with Industry Canada license-exempt RSSs. Operation is subject to the following two conditions:

(1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

**Concernant les EVMs avec appareils radio:**

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

**Concerning EVMs Including Detachable Antennas:**

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

**Concernant les EVMs avec antennes détachables**

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required to follow the instructions set forth by Radio Law of Japan, which includes, but is not limited to, the instructions below with respect to EVMs (which for the avoidance of doubt are stated strictly for convenience and should be verified by User):

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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西新宿三井ビル

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3.4 *European Union*

3.4.1 *For EVMs subject to EU Directive 2014/30/EU (Electromagnetic Compatibility Directive)*:

This is a class A product intended for use in environments other than domestic environments that are connected to a low-voltage power-supply network that supplies buildings used for domestic purposes. In a domestic environment this product may cause radio interference in which case the user may be required to take adequate measures.

4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY MATERIALS PROVIDED WITH THE EVM (INCLUDING, BUT NOT LIMITED TO, REFERENCE DESIGNS AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY EPIDEMIC FAILURE WARRANTY OR IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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8. *Limitations on Damages and Liability:*

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9. *Return Policy.* Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265

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