

JCS2N60FB-VB Datasheet

N-Channel 650V (D-S) Power MOSFET

| PRODUCT SUMMARY | |
|----------------------------|----------------------------|
| V _{DS} (V) | 650 |
| R _{DS(on)} (Ω) | V _{GS} = 10 V 4.0 |
| Q _g (Max.) (nC) | 11 |
| Q _{gs} (nC) | 2.3 |
| Q _{gd} (nC) | 5.2 |
| Configuration | Single |

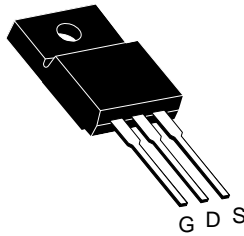
FEATURES

- Low Gate Charge Q_g Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic dV/dt Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Compliant to RoHS directive 2002/95/EC

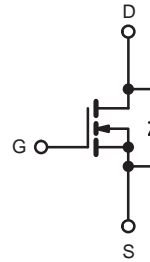


RoHS*
COMPLIANT

TO-220 FULLPAK



Top View




N-Channel MOSFET

| ABSOLUTE MAXIMUM RATINGS T _C = 25 °C, unless otherwise noted | | | |
|---|-----------------------------------|-------------------------|------|
| PARAMETER | SYMBOL | LIMIT | UNIT |
| Drain-Source Voltage | V _{DS} | 650 | V |
| Gate-Source Voltage | V _{GS} | ± 30 | |
| Continuous Drain Current ^e | V _{GS} at 10 V | T _C = 25 °C | A |
| Continuous Drain Current | | T _C = 100 °C | |
| Pulsed Drain Current ^a | I _{DM} | 8 | |
| Linear Derating Factor | | 0.48 | W/°C |
| Single Pulse Avalanche Energy ^b | E _{AS} | 165 | mJ |
| Repetitive Avalanche Current ^a | I _{AR} | 2 | A |
| Repetitive Avalanche Energy ^a | E _{AR} | 6 | mJ |
| Maximum Power Dissipation | P _D | 25 | W |
| Peak Diode Recovery dV/dt ^c | dV/dt | 2.8 | V/ns |
| Operating Junction and Storage Temperature Range | T _J , T _{stg} | - 55 to + 150 | °C |
| Soldering Recommendations (Peak Temperature) ^d | for 10 s | 300 | |
| Mounting Torque | 6-32 or M3 screw | 10 | |
| | | 1.1 | |

Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting T_J = 25 °C, L = 24 mH, R_G = 25 Ω, I_{AS} = 3.2 A (see fig. 12).
- I_{SD} ≤ 3.2 A, dI/dt ≤ 90 A/μs, V_{DD} ≤ V_{DS}, T_J ≤ 150 °C.
- 1.6 mm from case.
- Drain current limited by maximum junction temperature.

| THERMAL RESISTANCE RATINGS | | | | |
|----------------------------------|------------|------|------|------|
| PARAMETER | SYMBOL | TYP. | MAX. | UNIT |
| Maximum Junction-to-Ambient | R_{thJA} | - | 65 | °C/W |
| Maximum Junction-to-Case (Drain) | R_{thJC} | - | 2.1 | |

| SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted | | | | | | | |
|--|-----------------------|---|---|------|------|-----------|---------------|
| PARAMETER | SYMBOL | TEST CONDITIONS | | MIN. | TYP. | MAX. | UNIT |
| Static | | | | | | | |
| Drain-Source Breakdown Voltage | V_{DS} | $V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$ | | 650 | - | - | V |
| V_{DS} Temperature Coefficient | $\Delta V_{DS}/T_J$ | Reference to $25\text{ }^\circ\text{C}$, $I_D = 1\text{ mA}^d$ | | - | 670 | - | mV/°C |
| Gate-Source Threshold Voltage | $V_{GS(th)}$ | $V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$ | | 2.0 | - | 4.0 | V |
| Gate-Source Leakage | I_{GSS} | $V_{GS} = \pm 30\text{ V}$ | | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current | I_{DSS} | $V_{DS} = 650\text{ V}, V_{GS} = 0\text{ V}$ | | - | - | 25 | μA |
| | | $V_{DS} = 520\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$ | | - | - | 250 | |
| Drain-Source On-State Resistance | $R_{DS(on)}$ | $V_{GS} = 10\text{ V}$ | $I_D = 1\text{ A}^b$ | - | 4.0 | - | Ω |
| Forward Transconductance | g_{fs} | $V_{DS} = 50\text{ V}, I_D = 1\text{ A}$ | | 3.9 | - | - | S |
| Dynamic | | | | | | | |
| Input Capacitance | C_{iss} | $V_{GS} = 0\text{ V}, V_{DS} = 25\text{ V}, f = 1.0\text{ MHz}$, see fig. 5 | | - | 1000 | - | pF |
| Output Capacitance | C_{oss} | | | - | 45 | - | |
| Reverse Transfer Capacitance | C_{rss} | | | - | 5 | - | |
| Output Capacitance | C_{oss} | $V_{GS} = 0\text{ V}$ | $V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$ | - | 912 | - | pF |
| | | | $V_{DS} = 520\text{ V}, f = 1.0\text{ MHz}$ | - | 26 | - | |
| Effective Output Capacitance | $C_{oss\text{ eff.}}$ | $V_{DS} = 0\text{ V to } 520\text{ V}^c$ | | - | 42 | - | |
| Total Gate Charge | Q_g | $V_{GS} = 10\text{ V}$ | $I_D = 1.2\text{ A}, V_{DS} = 400\text{ V}$ see fig. 6 and 13 ^b | - | - | 11 | nC |
| Gate-Source Charge | Q_{gs} | | | - | - | 2.3 | |
| Gate-Drain Charge | Q_{gd} | | | - | - | 5.2 | |
| Turn-On Delay Time | $t_{d(on)}$ | $V_{DD} = 325\text{ V}, I_D = 1.2\text{ A}$ $R_G = 9.1\text{ }\Omega, R_D = 62\text{ }\Omega$, see fig. 10 ^b | | - | 14 | - | ns |
| Rise Time | t_r | | | - | 20 | - | |
| Turn-Off Delay Time | $t_{d(off)}$ | | | - | 34 | - | |
| Fall Time | t_f | | | - | 18 | - | |
| Drain-Source Body Diode Characteristics | | | | | | | |
| Continuous Source-Drain Diode Current | I_S | MOSFET symbol showing the integral reverse p - n junction diode  | - | - | 2 | A | |
| Pulsed Diode Forward Current ^a | I_{SM} | | - | - | 8 | | |
| Body Diode Voltage | V_{SD} | $T_J = 25\text{ }^\circ\text{C}, I_S = 3.2\text{ A}, V_{GS} = 0\text{ V}^b$ | | - | - | 1.5 | V |
| Body Diode Reverse Recovery Time | t_{rr} | $T_J = 25\text{ }^\circ\text{C}, I_F = 3.2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}^b$ | | - | 180 | 230 | ns |
| Body Diode Reverse Recovery Charge | Q_{rr} | | | - | 2.1 | 3.2 | μC |
| Forward Turn-On Time | t_{on} | Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D) | | | | | |

Notes

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width $\leq 300\text{ }\mu\text{s}$; duty cycle $\leq 2\%$.
- c. $C_{oss\text{ eff.}}$ is a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80 % V_{DS} .
- d. $t = 60\text{ s}, f = 60\text{ Hz}$.

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Fig. 1 - Typical Output Characteristics



Fig. 3 - Typical Transfer Characteristics



Fig. 2 - Typical Output Characteristics

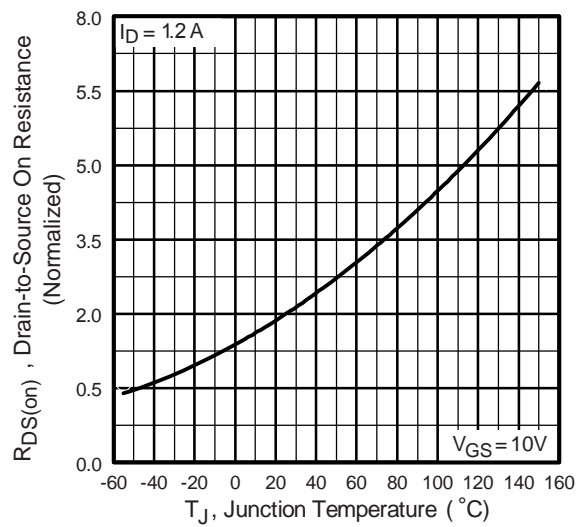


Fig. 4 - Normalized On-Resistance vs. Temperature

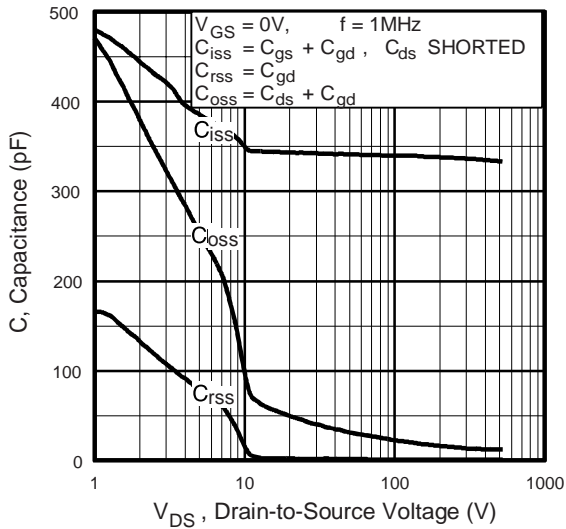


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage



Fig. 7 - Typical Source-Drain Diode Forward Voltage

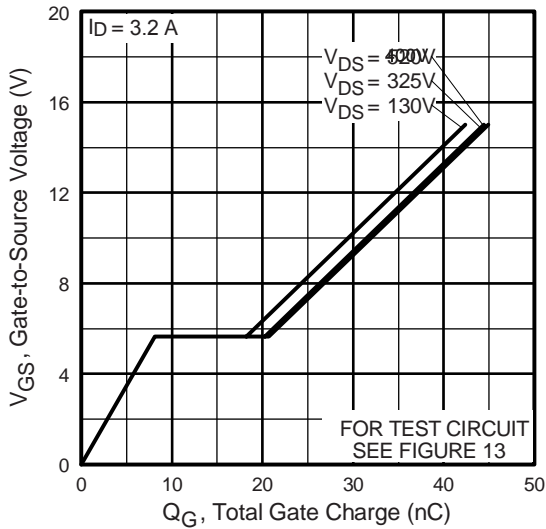


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

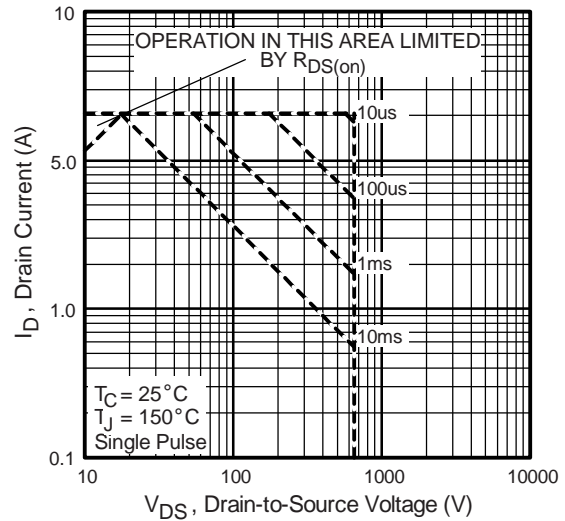


Fig. 8 - Maximum Safe Operating Area

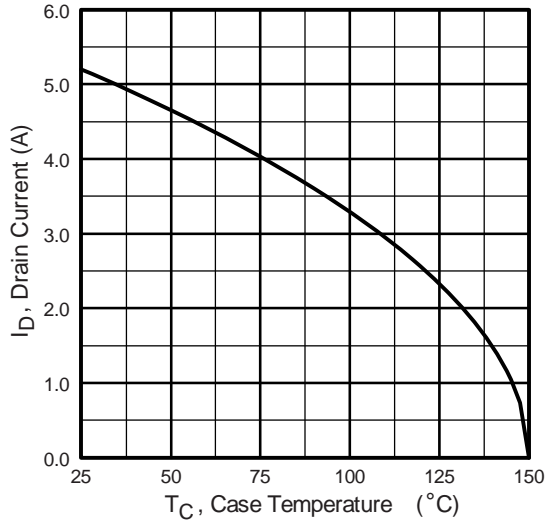


Fig. 9 - Maximum Drain Current vs. Case Temperature

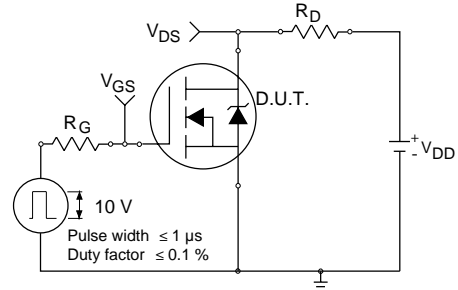


Fig. 10a - Switching Time Test Circuit



Fig. 10b - Switching Time Waveforms

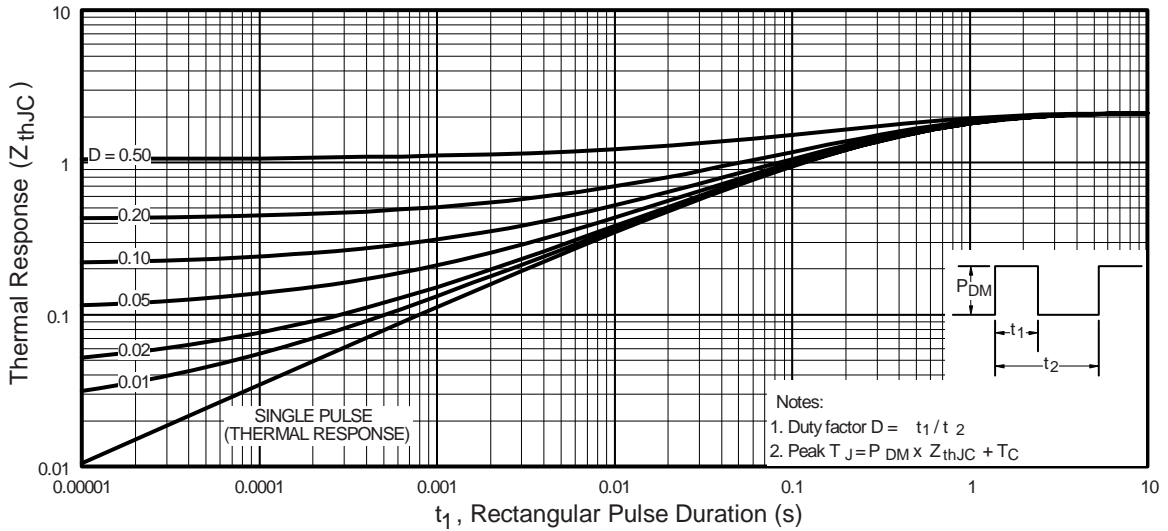


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

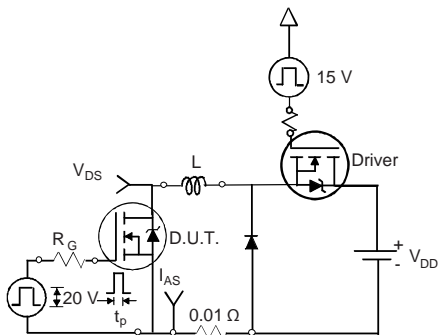


Fig. 12a - Unclamped Inductive Test Circuit

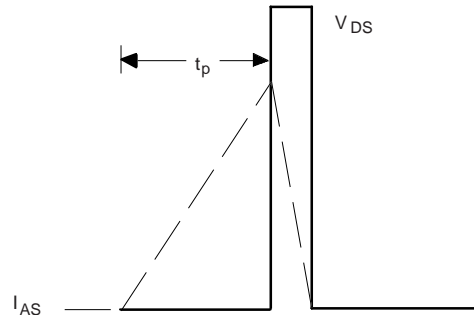


Fig. 12b - Unclamped Inductive Waveforms



Fig. 12c - Maximum Avalanche Energy vs. Drain Current



Fig. 12d - Typical Drain-to Source Voltage vs. Avalanche Current



Fig. 13a - Basic Gate Charge Waveform



Fig. 13b - Gate Charge Test Circuit

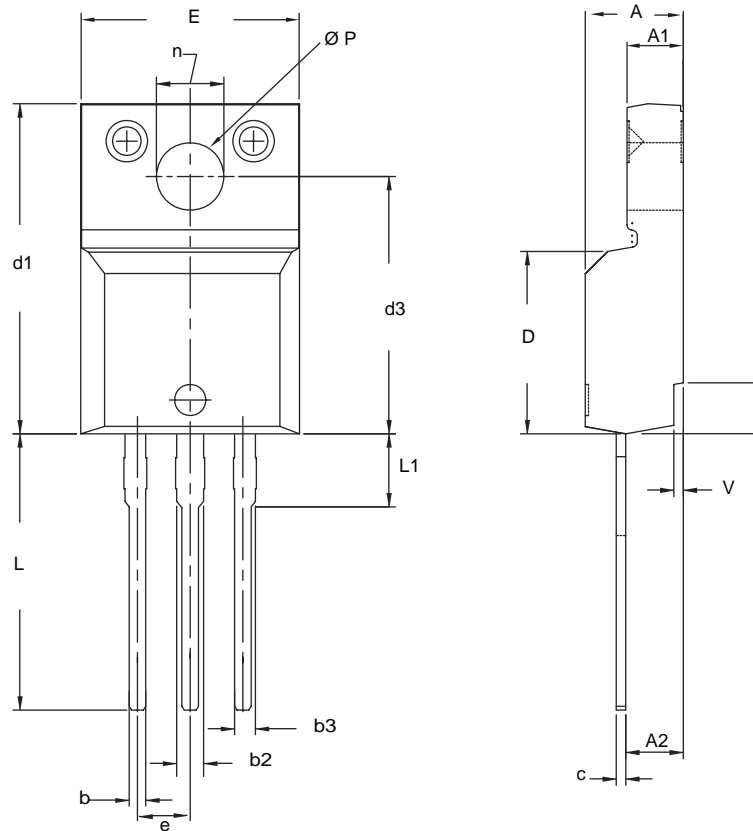
Peak Diode Recovery dV/dt Test Circuit



* $V_{GS} = 5 V$ for logic level devices

Fig. 14 - For N-Channel

TO-220 FULLPAK (HIGH VOLTAGE)



| DIM. | MILLIMETERS | | INCHES | |
|------|-------------|--------|-----------|-------|
| | MIN. | MAX. | MIN. | MAX. |
| A | 4.570 | 4.830 | 0.180 | 0.190 |
| A1 | 2.570 | 2.830 | 0.101 | 0.111 |
| A2 | 2.510 | 2.850 | 0.099 | 0.112 |
| b | 0.622 | 0.890 | 0.024 | 0.035 |
| b2 | 1.229 | 1.400 | 0.048 | 0.055 |
| b3 | 1.229 | 1.400 | 0.048 | 0.055 |
| c | 0.440 | 0.629 | 0.017 | 0.025 |
| D | 8.650 | 9.800 | 0.341 | 0.386 |
| d1 | 15.88 | 16.120 | 0.622 | 0.635 |
| d3 | 12.300 | 12.920 | 0.484 | 0.509 |
| E | 10.360 | 10.630 | 0.408 | 0.419 |
| e | 2.54 BSC | | 0.100 BSC | |
| L | 13.200 | 13.730 | 0.520 | 0.541 |
| L1 | 3.100 | 3.500 | 0.122 | 0.138 |
| n | 6.050 | 6.150 | 0.238 | 0.242 |
| Ø P | 3.050 | 3.450 | 0.120 | 0.136 |
| u | 2.400 | 2.500 | 0.094 | 0.098 |
| v | 0.400 | 0.500 | 0.016 | 0.020 |

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DWG: 5972

Notes

1. To be used only for process drawing.
2. These dimensions apply to all TO-220, FULLPAK leadframe versions 3 leads.
3. All critical dimensions should C meet $C_{pk} > 1.33$.
4. All dimensions include burrs and plating thickness.
5. No chipping or package damage.

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