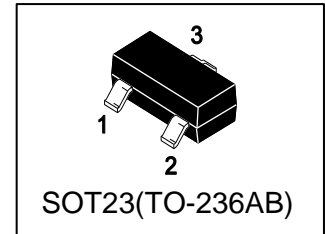


# LN2312LT1G

## 20V N-Channel Enhancement-Mode MOSFET

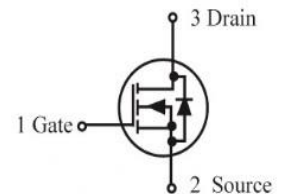
### 1. FEATURES

- VDS= 20V
- RDS(ON), VGS@4.5V, IDS@5A ≤ 41mΩ
- RDS(ON), VGS@2.5V, IDS@4.5A ≤ 47mΩ
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



### 2. APPLICATIONS

- High density cell design for ultra low on-resistance
- Advanced trench process technology



### 3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LN2312LT1G	N12	3000/Tape&Reel
LN2312LT3G	N12	10000/Tape&Reel

### 4. MAXIMUM RATINGS(Ta = 25°C)

Parameter	Symbol	Limits	Unit
Drain–Source Voltage	VDSS	20	V
Gate–to–Source Voltage – Continuous	VGS	±8	V
Drain Current			A
– Continuous TA = 25°C	ID	4.9	
– Pulsed(Note 1)	IDM	15	

### 5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Maximum Power Dissipation	PD	0.75	W
Thermal Resistance, Junction–to–Ambient(Note 2)	RθJA	140	°C/W
Junction and Storage temperature	TJ,Tstg	-55~+150	°C

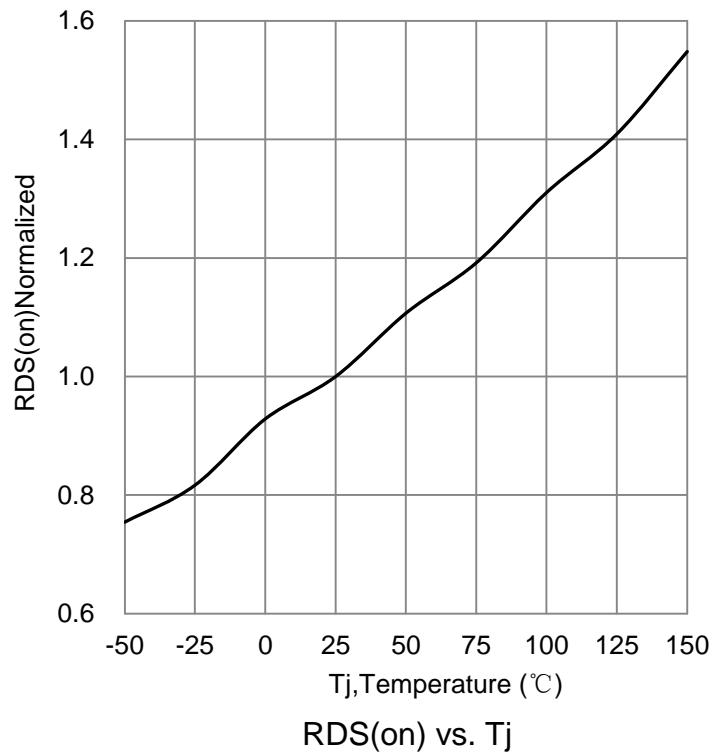
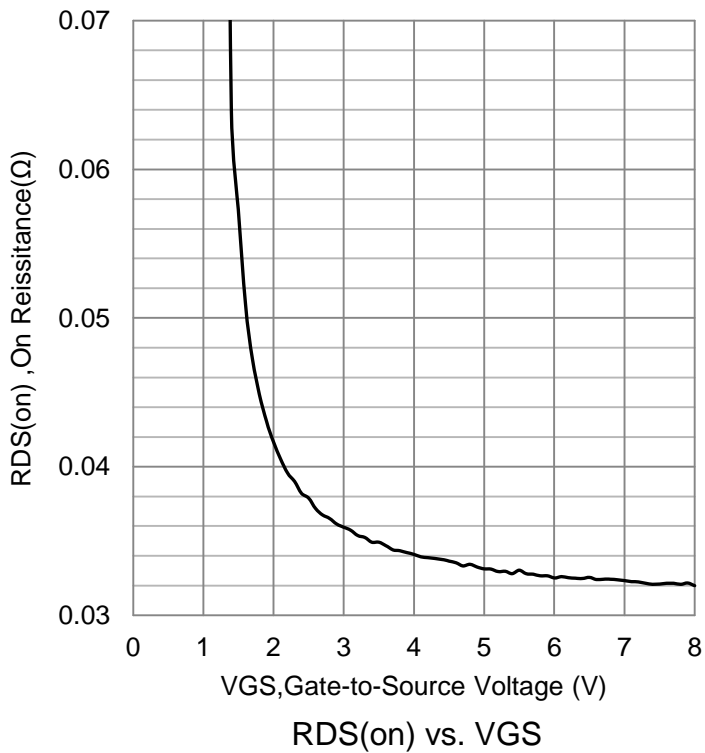
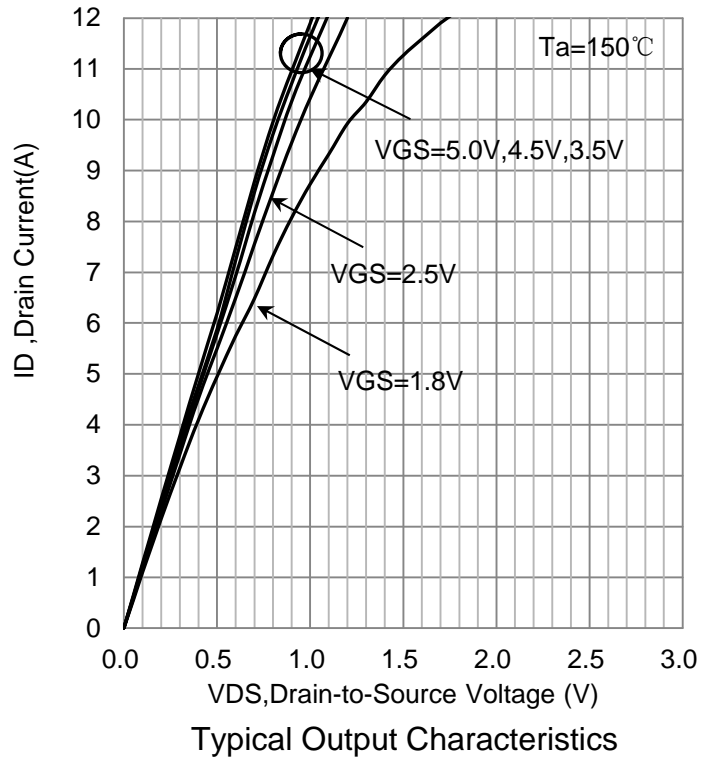
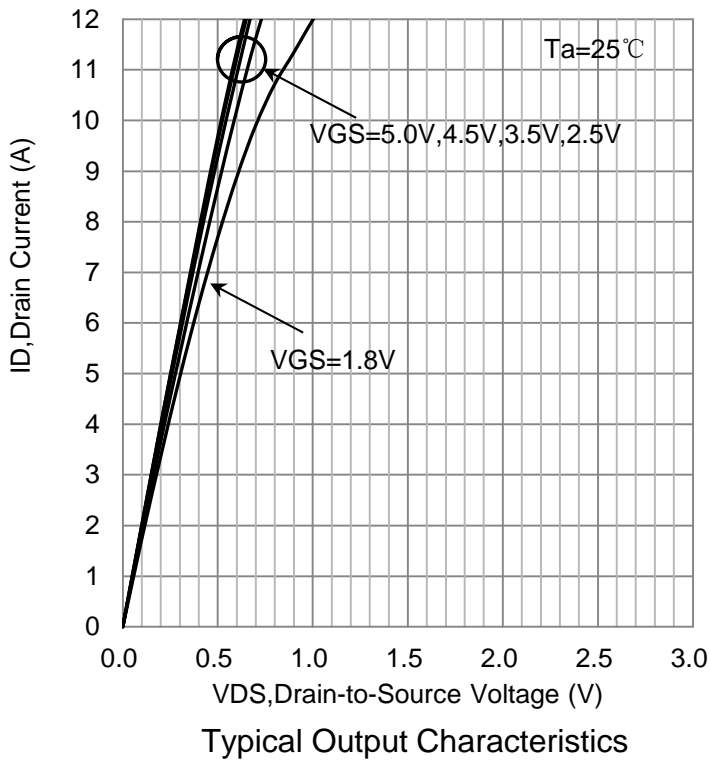
1. Repetitive Rating: Pulse width limited by the Maximum junction temperature.
2. 1-in<sup>2</sup> 2oz Cu PCB board.

**6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)**

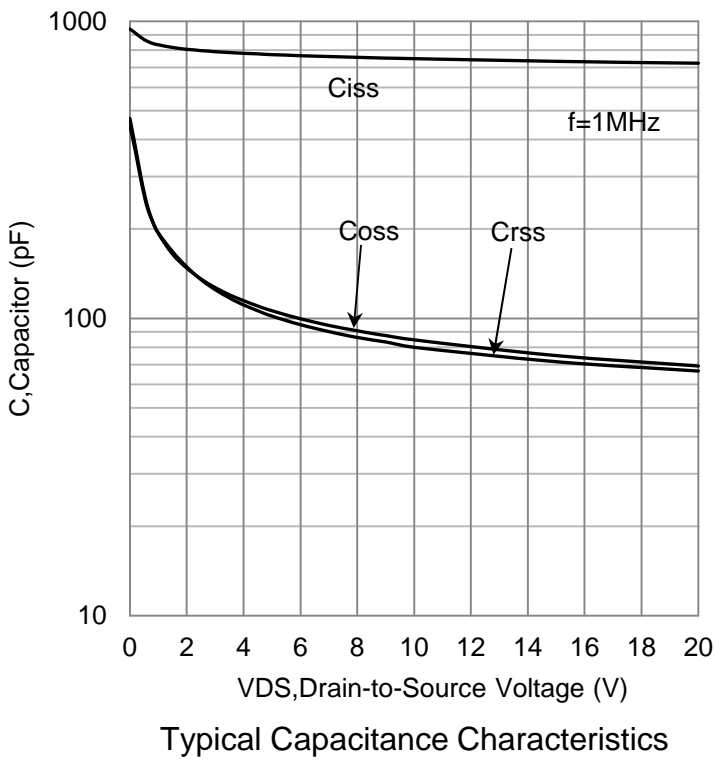
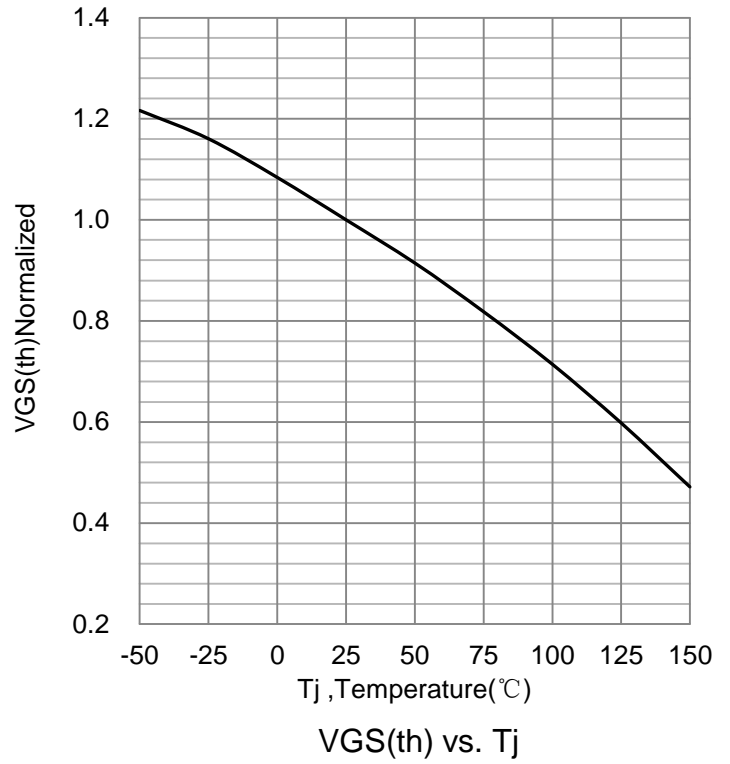
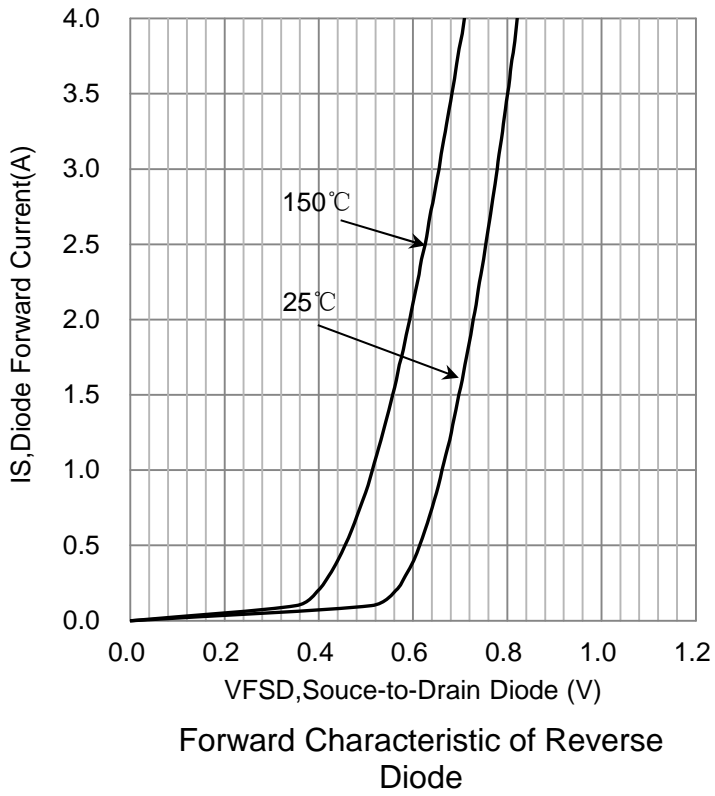
Characteristic	Symbol	Min.	Typ.	Max.	Unit
<b>STATIC</b>					
Drain–Source Breakdown Voltage (VGS = 0, ID = 250μA)	V(BR)DSS	20	-	-	V
Gate Threshold Voltage (VDS = VGS, ID = 250μA)	VGS(th)	0.4	0.6	1.0	V
Zero Gate Voltage Drain Current (VDS=20V, VGS=0V)	IDSS	-	-	1	μA
Gate–Body Leakage Current, Forward (VDS = 0 V, VGS = 8 V)	IGSSF	-	-	100	nA
Gate–Body Leakage Current, Reverse (VDS = 0 V, VGS = -8 V)	IGSSR	-	-	-100	nA
Static Drain–Source On–State Resistance (VGS = 1.8 V, ID = 4 A) (VGS = 2.5 V, ID = 4.5 A) (VGS = 4.5 V, ID = 5 A)	RDS(on)	-	31 24 21	57 47 41	mΩ
Diode Forward Voltage (VGS = 0 V, ISD = 1.7 A)	VSD	-	-	1.2	V
<b>DYNAMIC</b>					
Input capacitance	(VDS =8V, VGS =0V, f=1MHz)	Ciss	-	500	-
Output Capacitance		Coss	-	300	-
Reverse Transfer Capacitance		Crss	-	140	-
Turn-On Delay Time	(VDD =10V, ID =1A, VGEN=4.5V, RG = 6Ω)	td(on)	-	5.5	-
Rise Time		tr	-	10	-
Turn-Off Delay Time		td(off)	-	33	-
Fall Time		tf	-	15	-
Total Gate Charge	(VDS = 10 V, VGS = 4.5 V, ID = 5 A)	Qg	-	5.9	-
Gate to Source Charge		Qgs	-	0.9	-
Gate to Drain Charge		Qgd	-	1.3	-

3.Pulse test; pulse width≤300μs, duty cycle≤2%.

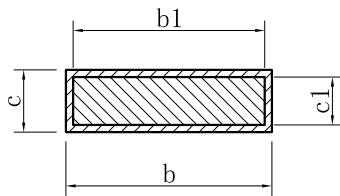
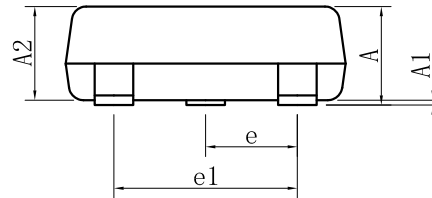
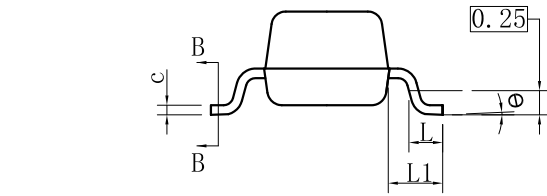
### 7. ELECTRICAL CHARACTERISTICS CURVES



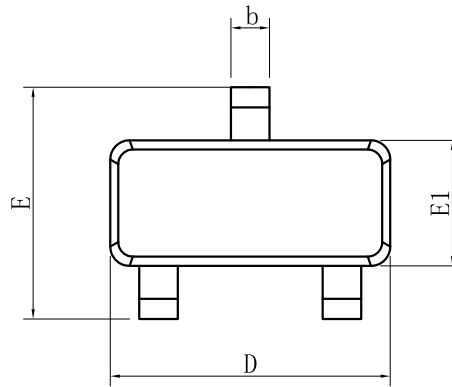
**7. ELECTRICAL CHARACTERISTICS CURVES (Con.)**



### 8. OUTLINE AND DIMENSIONS



SECTION B-B

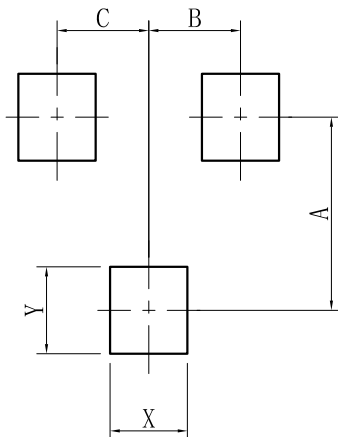


SOT23			
DIM	MIN	NOR	MAX
A	0.89	-	1.12
A1	0.01	-	0.10
A2	0.88	0.95	1.02
b	0.30	-	0.50
b1	0.30	0.40	0.45
c	0.08	-	0.20
c1	0.08	0.10	0.16
D	2.80	2.90	3.04
E	2.10	-	2.64
E1	1.20	1.30	1.40
e	0.95BSC		
e1	1.90BSC		
L	0.40	0.46	0.60
L1	0.54REF		
θ	0°	-	8°
All Dimensions in mm			

#### GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um

### 9. SOLDERING FOOTPRINT



SOT23	
DIM	(mm)
X	0.80
Y	0.90
A	2.00
B	0.95
C	0.95

## **DISCLAIMER**

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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