WD1502F

Http//:www.sh-willsemi.com

28V, 2A, Step-Down DC/DC Converter

Descriptions

WD1502 is a high efficiency, synchronous step down DC-DC converter. It can deliver up to 2A of continuous output current with operating at an input range of 4.5V-28V. The internal synchronous power switches provide high efficiency without the use of an external Schottky diode. WD1502 operates at 650 kHz fixed switching frequency with Pulse-Width-Modulation (PWM) and enters Pulse-Skipping-Modulation (PSM) operation at light load current to maintain high efficiency and low output ripple over the entire load current range.

The WD1502 has short-circuit protection, thermal protection, and input under voltage lockout.

The WD1502 is available in TSOT-23-6L package. Standard products is Pb-Free and Halogen-Free.

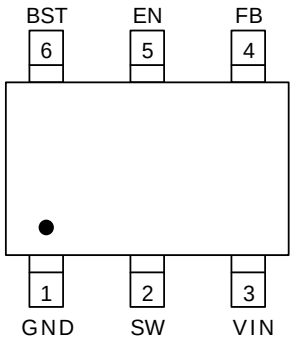
Features

- Wide 4.5V~28V Operating Input Range
- Typical 650 kHz Switching Frequency
- 2A continuous output current
- Low 2-μA Shutdown, 60-μA Quiescent Current
- Internal 5mS Soft-Start
- Peak Efficiency > 94%
- 150mΩ Internal Power HS MOSFET Switch
- 75mΩ Internal Synchronous LS MOSFET Switch
- Cycle-by-Cycle Over Current Protection

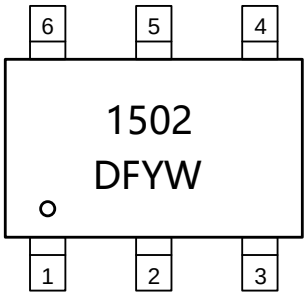
Applications

- 12V, 24V Distributed Power-Bus Supply
- Industrial Applications
- White Goods
- Consumer Application

TSOT-23-6L



Pin configuration (Top view)



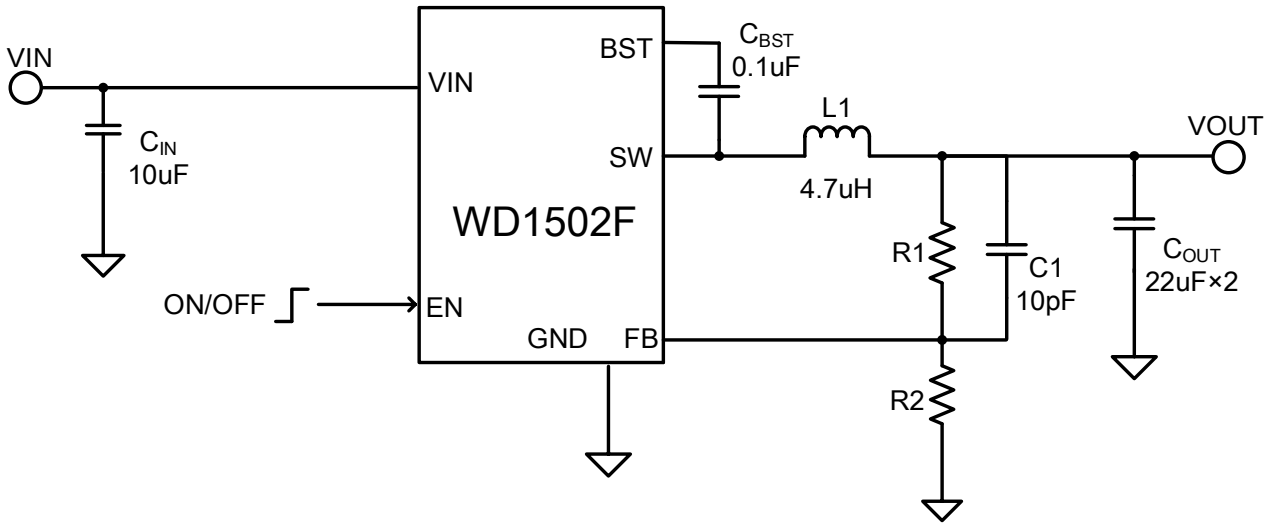
1502 = Device code
DF = Special code
Y = Year code
W = Week code

Marking

Order information

Device	Package	Shipping
WD1502F-6/TR	TSOT-23-6L	3000/Reel&Tape

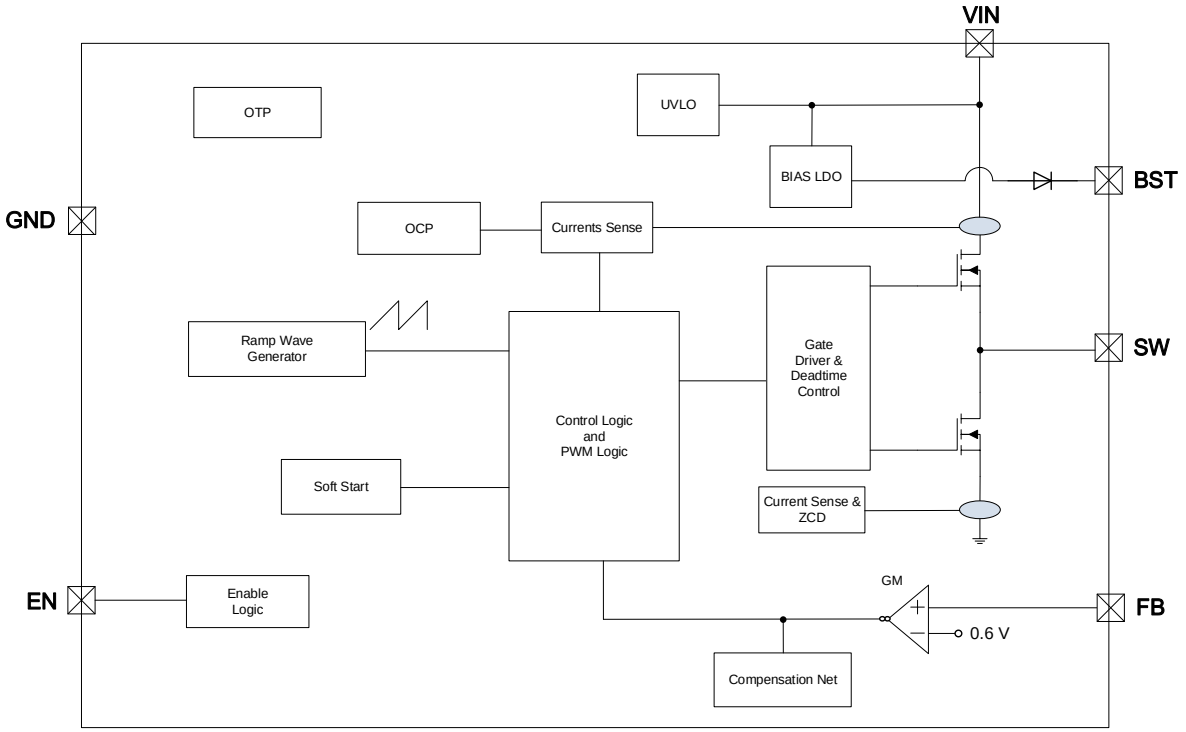
Typical Applications



Pin Descriptions

Symbol	Pin Number	Descriptions
GND	1	Ground pin. Ground reference for power circuit as well as controller circuit.
SW	2	Switch Node. Connect this pin to the switching end of the inductor.
VIN	3	Power Supply Input. Connecting a ceramic bypass capacitor between VIN and GND.
FB	4	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage.
EN	5	On/Off Control Input. Device would be enabled if float this pin.
BST	6	Bootstrap pin. A 100nF capacitor is connected between SW and BST pin to supply high side driver.

Block Diagram



Absolute Maximum Ratings

Parameter	Symbol	Value	Unit
VIN pin voltage range	V_{IN}	-0.3～+36	V
EN pin voltage range	-	-0.3～7	V
SW pin voltage range (DC)	V_{SW}	-0.3～$V_{IN(Max)}$	V
BST pin voltage range(DC)	-	(V_{SW} – 0.3) ~ (V_{SW} + 7)	V
All Other Pins Voltage	-	-0.3~ 7	V
Power Dissipation – TSOT23-6L (Note 1)	P_D	0.5	W
Thermal Characteristics (Note 1)	$R_{\theta JA}$	250	°C/W
	$R_{\theta JC}$	110	°C/W
Maximum Junction Temperature	T_J	150	°C
Lead temperature(Soldering, 10s)	T_L	260	°C
Operating ambient temperature	Topr	-40 ~ 85	°C
Storage temperature	Tstg	-65 ~ 150	°C
ESD Classification	HBM	5000	V
	CDM	2000	V

These are stress ratings only. Stresses exceeding the range specified under “Absolute Maximum Ratings” may cause substantial damage to the device. Functional operation of this device at other conditions beyond those listed in the specification is not implied and prolonged exposure to extreme conditions may affect device reliability.

Note 1: Surface mounted on FR-4 Board using 1 square inch pad size, dual side, 1oz copper

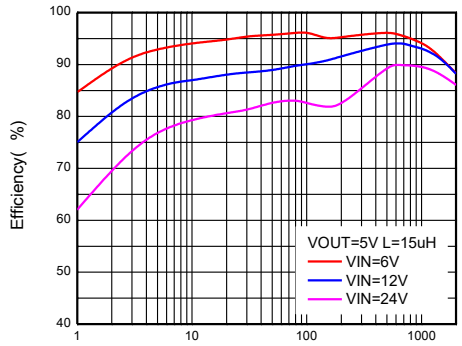
Electronics Characteristics

(Ta=25℃, V_{IN}=12V, V_{EN}=2V, unless otherwise noted)

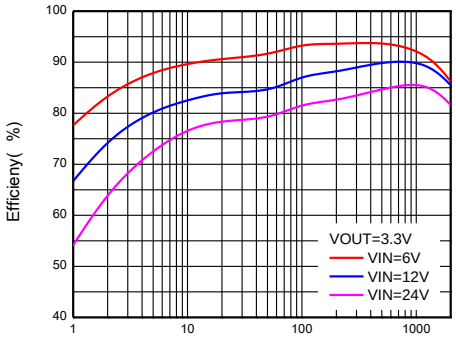
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	V_{IN}		4.5		28	V
V_{IN} Under Voltage Lockout Threshold	V_{UVLO}	Rising		4	4.3	V
		Falling	3.3	3.6		
Standby Supply Current	I_Q	V_{FB} = 105%, I_{OUT} = 0A		60		uA
Shutdown Supply Current	I_{SHDN}	V_{EN} = 0V, Vin=12V		2	5	uA
Feedback reference Voltage	V_{FB}		0.588	0.6	0.612	V
Inductor Peak Current Limit	$I_{LIM-Peak}$	V_{IN} = 12V, V_{OUT} = 5V	3	4	4.9	A
Inductor Valley Current Limit	$I_{LIM-Valley}$		2.4	2.8	3.2	A
Switching Frequency	f_{OSC}	CCM		650		kHz
$R_{DS(ON)}$ of HS	R_{HS}	I_{SW} = −100mA		150		mΩ
$R_{DS(ON)}$ of LS	R_{LS}	I_{SW} = 100mA		75		mΩ
Feedback Leakage Current	I_{FB}	VFB=0.65V			±30	nA
SW Leakage Current	I_{LSW}	V_{IN} = 12V, V_{SW} = 0V or 12V			±1	uA
EN Rising Threshold	V_{ENH}			1.27	1.3	V
EN Falling Threshold	V_{ENL}		1.05	1.19		V
EN Leakage Current	I_{EN}	V_{IN} = 12V, V_{EN} = 1		0.7		uA
		V_{IN} = 12V, V_{EN} = 1.5 V		1.5		
Min On Time	T_{ON-MIN}			110		nS
Soft Start Time	SS			5		mS
Over Temperature Protection	T_{OTP}			155		°C
OTP Hysteresis	T_{OTP_HYS}			30		°C

Typical Characteristics

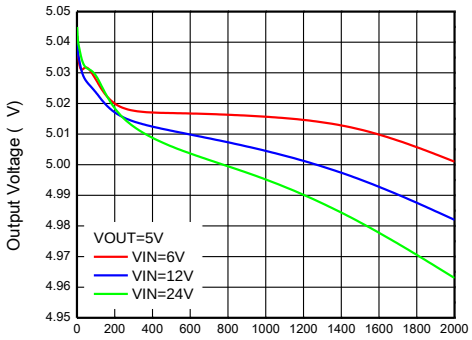
(Ta=25°C, V_{IN}=12V, V_{EN}=2V, V_{OUT}=5V, L1=4.7uH, C_{IN}=10uF, C_{OUT}=22μF×2, C1=10pF, unless otherwise noted)



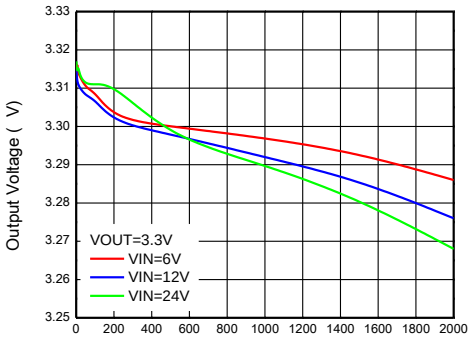
Efficiency vs.Load Current



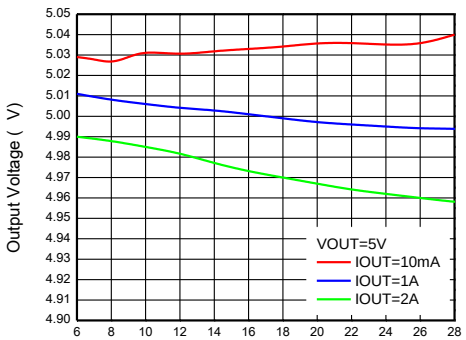
Efficieny vs.Load Current



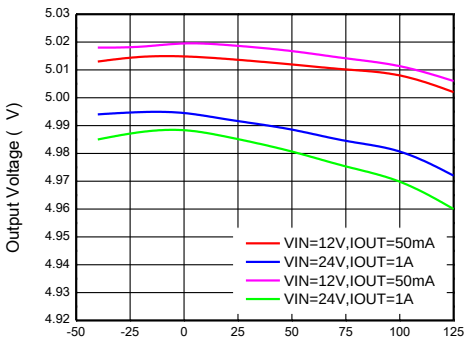
Output Voltage vs.Output Current



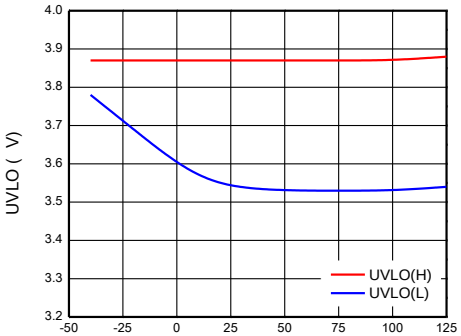
Output Voltage vs.Output Current



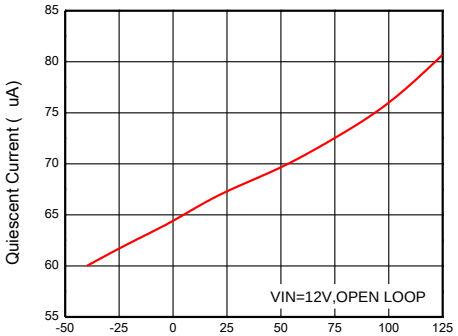
Output Voltage vs.Input Voltage



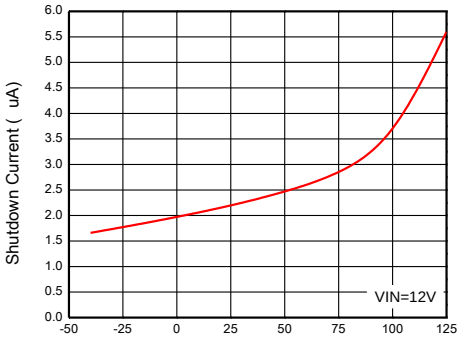
Output Voltage vs.Temperature



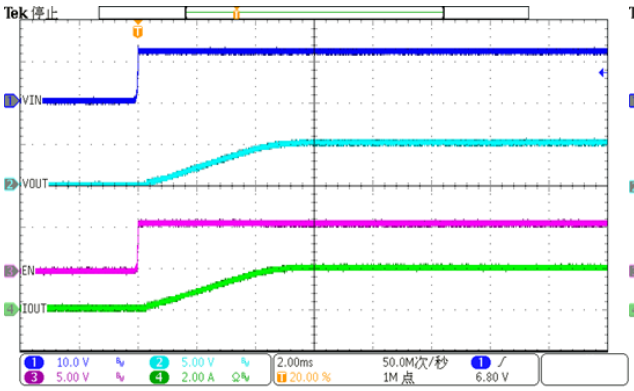
UVLO vs.Temperature



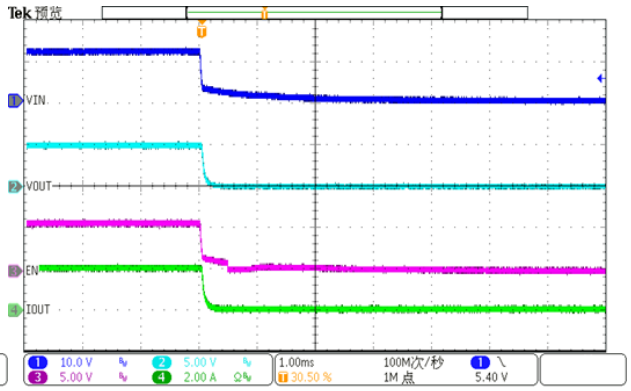
Quiescent Current vs.Temperature



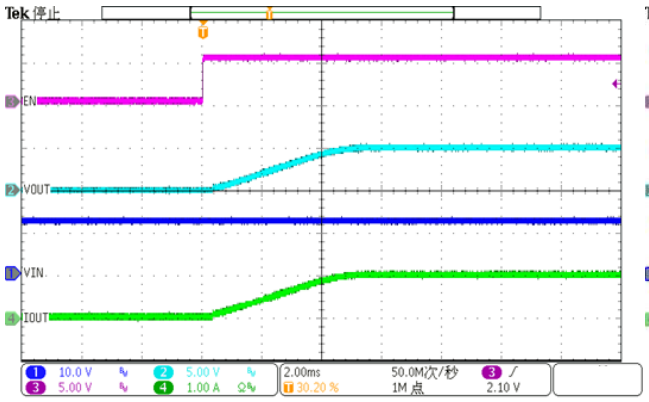
Quiescent Current vs.Temperature



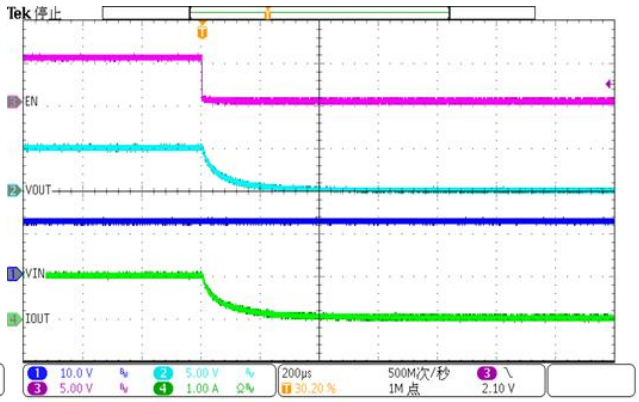
Start Up From V_{IN}; V_{IN}=12V, V_{EN}=5V, V_{OUT}=5V, I_{OUT}=2A



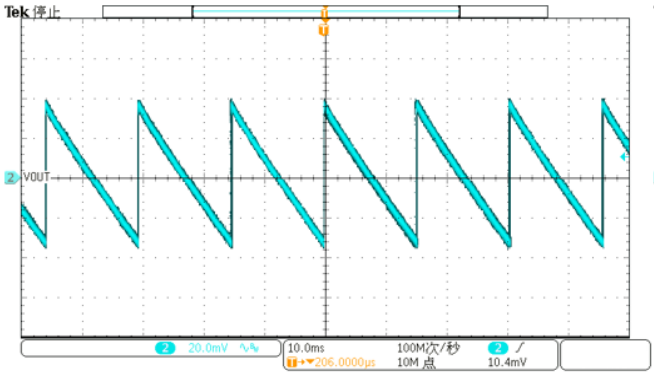
Shut Down From V_{IN}; V_{IN}=12V, V_{EN}=5V, V_{OUT}=5V, I_{OUT}=2A



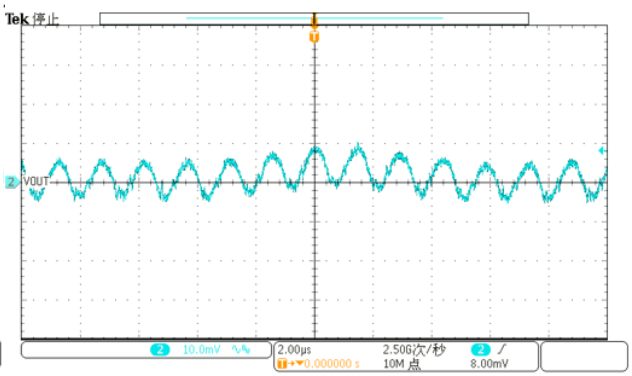
Start Up From EN; V_{IN}=12V, V_{EN}=5V, V_{OUT}=5V, I_{OUT}=2A



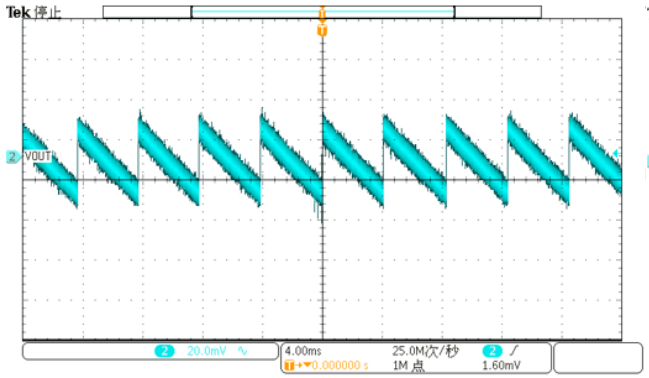
Shut Down From EN; V_{IN}=12V, V_{EN}=5V, V_{OUT}=5V, I_{OUT}=2A



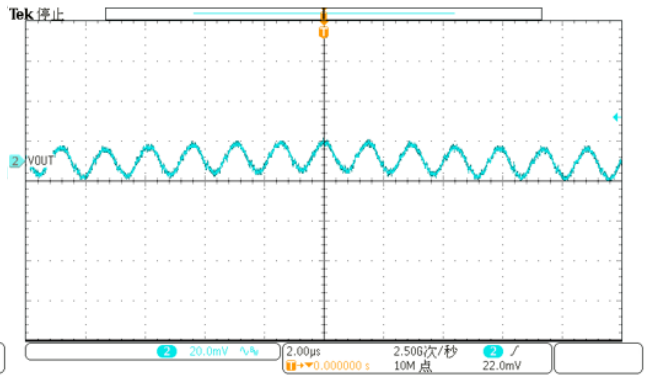
Ripple; V_{IN}=12V,V_{EN}=5V,V_{OUT}=3.3V,I_{OUT}=0mA



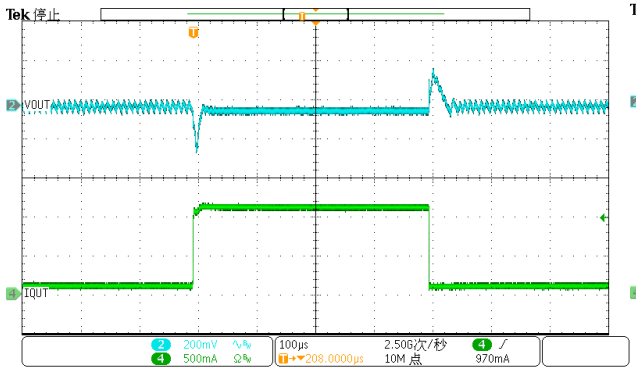
Ripple; V_{IN}=12V,V_{EN}=5V,V_{OUT}=3.3V,I_{OUT}=2000mA



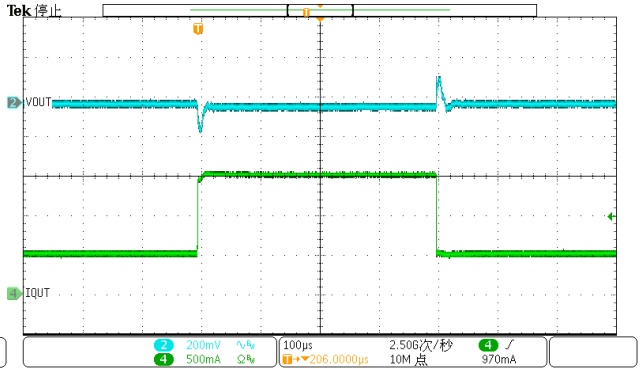
Ripple; V_{IN}=12V,V_{EN}=5V,V_{OUT}=5V,I_{OUT}=0mA



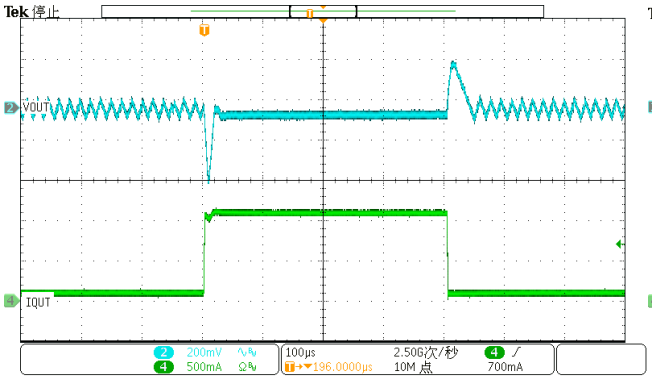
Ripple; V_{IN}=12V,V_{EN}=5V,V_{OUT}=5V,I_{OUT}=2000mA



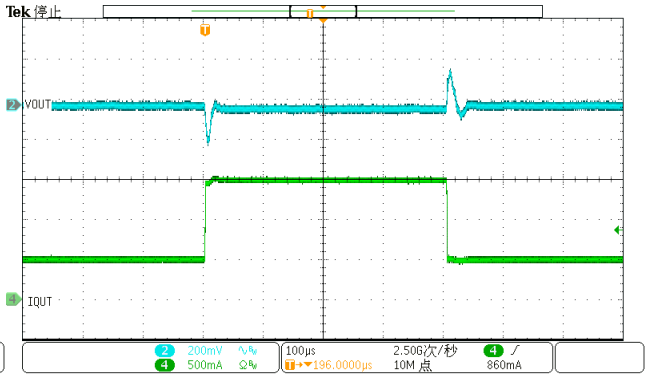
Load Transient: V_{IN}=12V,V_{EN}=5V,V_{OUT}=3.3V,I_{OUT}=0.1A-1A



Load Transient: V_{IN}=12V,V_{EN}=5V,V_{OUT}=3.3V,I_{OUT}=0.5A-1.5A



Load Transient; V_{IN}=12V,V_{EN}=5V,V_{OUT}=5V,I_{OUT}=0.1A-1A



Load Transient; V_{IN}=28V,V_{EN}=5V,V_{OUT}=5V,I_{OUT}=0.5A-1.5A

Operation Informations

Control Mode

The WD1502 is a 28V, 2A step-down converter operates with typically 650 kHz fixed-frequency at moderate to heavy load condition. Both upper and lower synchronous N-channel MOSFET switches are integrated internally. The converter uses a peak-current-mode control scheme with optimized internal compensation network to achieve good line and load transient response. At the beginning of each clock cycle initiated by the clock signal, the main switch is turned on. The current flows from the input capacitor via the main switch through the inductor to the output capacitor and load. During this phase, the current ramps up until the PWM comparator trips and the control logic turn off the switch. After a dead time, which prevents shoot-through current, the synchronous switch is turned on and the inductor current ramps down. The current flows from the inductor and the output capacitor to the load. It returns back to the inductor through the synchronous switch.

The next cycle is initiated by the clock signal again turning off the synchronous switch and turning on the main switch.

WD1502 automatically enters Pulse-Skipping-Modulation (PSM) operation at light load condition to maintain the high efficiency.

Enable

The WD1502 has an enable input pin EN. A high level (above 1.3 V) on this pin enables the device if VIN is above UVLO. A low level on this pin disables the device and makes the device in shutdown mode. In shutdown mode, the reference, control circuit, main switch, and synchronous switch turn off and the output becomes high impedance.The EN pin has a small internal pull-up which allows the device to be enabled by default when this pin is floating. A Zener diode (typical break down voltage 6.9 V) is integrated internally to clamp the EN input voltage, so that connects EN to VIN directly via a high resistance resistor (typical >=100k to limit the quiescent current) to enable the device is allowed to simplify the design.

Over-Current and Short-Circuit Protection

The device is protected from over current by a cycle-by-cycle current limitation on both high-side MOSFET and low-side MOSFET.

When high side FET turns on, the peak switch current ramps up until the PWM comparator trips and the control logic turn off the high side FET and turn on the low-side MOSFET after deadtime, the conduction current is monitored by the internal circuitry. At the end of every clock cycle, the low-side MOSFET sourcing current is compared to the internally set low-side sourcing current-limit. If the low-side sourcing current-limit is exceeded, the high-side MOSFET does not turn on and the low-side MOSFET stays on for the next cycle. The high-side MOSFET turns on again when the low-side current is below the low-side sourcing current-limit at the start of a cycle which is the inductor current valley value.

When the output is shorted to ground, the device goes into shutdown mode. In this mode, the high-side and low-side MOSFET are turned off.

Over Temperature Protection (OTP)

As soon as the junction temperature (T_J) exceeds 155°C (Typ.), the device goes into thermal shutdown. In this mode, both high-side and low-side MOSFET are turned off. If the junction temperature drops below 125°C (Typ.), the system automatically recovers and a normal power−up sequence follows.

Application Informations

External component selection for the application circuit depends on the load current requirements. Certain tradeoffs between different performance parameters can also be made.

Output Voltage Setting

The output voltage can be calculated as:

$$V_{OUT} = V_{FB} \times \left(1 + \frac{R1}{R2}\right)$$

Where

V_{OUT} = output voltage

V_{FB} = feedback reference voltage

R_1 = resistance between OUT and FB

R_2 = resistance between FB and GND

The external resistive divider is connected to the output. An external feed forward capacitor C1, is required for optimum load transient response. The value of C1 should be in the range between 10pF and 22pF.

Route the FB line away from noise sources, such as the V_{IN} and the SW line.

Inductor Selection

The high switching frequency of WD1502 allows the use of a physically small inductor. The inductor ripple current is determined by

$$\Delta I_L = \frac{V_{OUT}}{f \times L}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

The inductor peak-to-peak current ripple is typically set to be 30% to 50% of the maximum dc load current. Using this guideline and solving for L,

$$L = \frac{V_{OUT}}{f \times 40\% \times I_{LOAD(MAX)}}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

It is important to ensure that the inductor is capable of handling the maximum peak inductor current, I_{LPK}, determined by

$$I_{LPK} = I_{LOAD(MAX)} + \frac{\Delta I_L}{2}$$

Where

V_{OUT} = output voltage

V_{IN} = input voltage

L = the inductance value.

f = the switching frequency.

$\triangle I_L$ = the peak-to-peak inductor ripple current

I_{LPK} = the maximum peak inductor current

Input Capacitor Selection

Capacitor ESR is a major contributor to input ripple in high-frequency DC-DC converters. Ordinary aluminum electrolytic capacitors have high ESR and should be avoided. Low-ESR tantalum or polymer capacitors are better and provide a compact solution for space constrained surface mount designs. Ceramic capacitors have the lowest overall ESR. Connect a low ESR ceramic capacitor to the input. Select this capacitor to meet the input ripple requirements and voltage rating rather than capacitance value. Use the following equation to calculate the maximum RMS input current:

$$I_{RMS} = \frac{I_{OUT}}{V_{IN}}\sqrt{V_{OUT} \times (V_{IN} - V_{OUT})}$$

Where

V_{OUT} = output voltage

V_{IN} = input voltage

I_{OUT} = output current

I_{LPK} = the maximum peak inductor current

I_{RMS} =the maximum RMS input current

Output Capacitor Selection

Ceramic capacitors are recommended at the output due to the lowest ESR and ESL performance. At moderate or heavy load condition, the device operates in PWM mode, and the RMS ripple current is calculated as:

$$I_{RMSCout} = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \frac{1}{2 \times \sqrt{3}}$$

Where

V_{OUT} = output voltage

V_{IN} = input voltage

L = the inductance value.

f = the switching frequency.

$\triangle I_L$ = the peak-to-peak inductor ripple current

$I_{RMSCOUT}$ = the RMS ripple current is calculated

At this condition, the overall output voltage ripple is the sum of the voltage spike caused by the output capacitor ESR plus the voltage ripple caused by charging and discharging the output capacitor:

$$\Delta V = V_{OUT} \times \frac{1 - \frac{V_{OUT}}{V_{IN}}}{L \times f} \times \left(\frac{1}{8 \times C_{OUT} \times f} + R_{ESR} \right)$$

Where

V_{OUT} = output voltage

V_{IN} = input voltage

L = the inductance value

f = the switching frequency

R_{ESR} = the ESR of the output capacitor

C_{OUT} = the output capacitor

ΔV = the output voltage ripple

At very light load condition, the converter operates in pulse skipping mode (PSM), and the output voltage ripple is dependent on the capacitor and inductor values. Larger output capacitor and inductor values minimize the voltage ripple and tighten dc output accuracy in PSM operation.

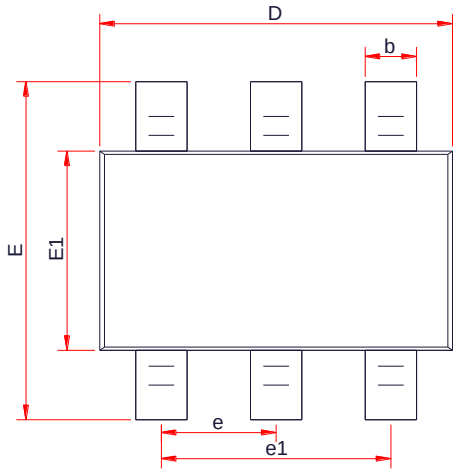
Layout Considerations

A good circuit board layout aids in extracting the most performance from the WD1502. Poor circuit layout degrades the output ripple and the electromagnetic interference (EMI) or electromagnetic compatibility (EMC) performance. The evaluation board layout is optimized for the WD1502. Use this layout as a good reference. If this layout needs changing, use the following guidelines:

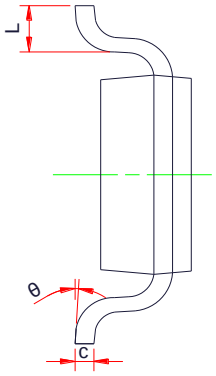
1. Locate C_{IN} as close to the V_{IN} pin as possible, and input loop area should be as small as possible.
2. Keep high current traces (from C_{IN}, VIN, SW, through L to C_{OUT}, and back to GND pin) as short and as wide as possible.
3. Place the feedback resistors as close as possible to the FB pin to prevent noise pickup.
4. Avoid routing FB trace near high current or voltage switching area such as SW node. Add ground shield for this loop if possible.

PACKAGE OUTLINE DIMENSIONS

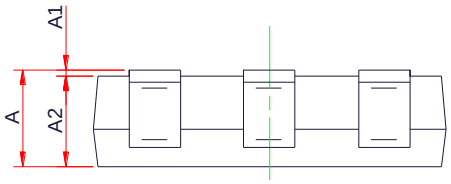
TSOT-23-6L



TOP VIEW



SIDE VIEW

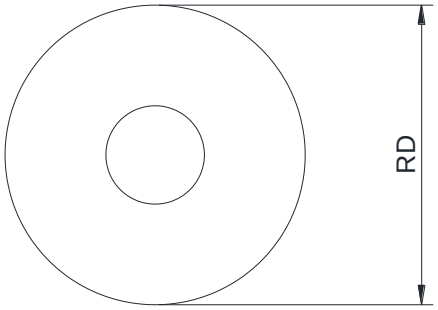


SIDE VIEW

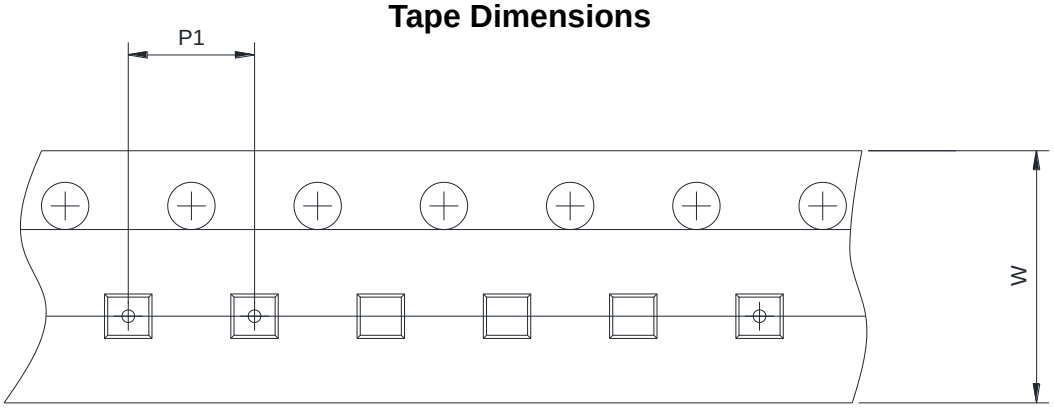
Symbol	Dimensions in Millimeters		
	Min.	Typ.	Max.
A	-	-	0.90
A1	0.00	-	0.10
A2	0.70	0.75	0.80
b	0.35	-	0.50
c	0.08	-	0.20
D	2.82	2.92	3.02
E	2.65	2.80	2.95
E1	1.60	1.65	1.70
e	0.95 BSC		
e1	1.90 BSC		
L	0.30	0.45	0.60
θ	0 °	-	8 °

TAPE AND REEL INFORMATION

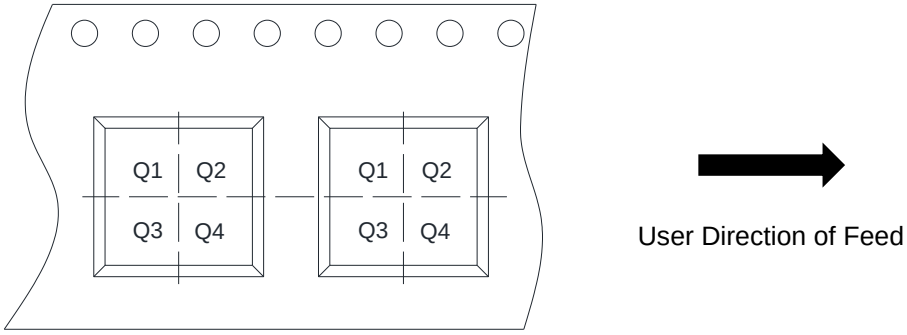
Reel Dimensions



Tape Dimensions



Quadrant Assignments For PIN1 Orientation In Tape



RD	Reel Dimension	☑ 7inch ☐ 13inch
W	Overall width of the carrier tape	☑ 8mm ☐ 12mm ☐ 16mm
P1	Pitch between successive cavity centers	☐ 2mm ☑ 4mm ☐ 8mm
Pin1	Pin1 Quadrant	☐ Q1 ☐ Q2 ☑ Q3 ☐ Q4