DATASHEET: ZM5202

FULLY INTEGRATED Z-WAVE® WIRELESS MODULE

The Silicon Labs ZM5202 module is a low-cost fully integrated Z-Wave module in a small 12.5mm x 13.6mm x 1.9mm form factor. It is an ideal solution for home control applications such as access control, appliance control, AV control, building automation, energy management, lighting, security, and sensor networks in the "Internet of Things".

It contains all the required passive components, including the crystal and a SAW filter to provide a complete Z-Wave system. The ZM5202 module remains pad and pin compatible with the ZM3102 and the ZM4102 Z-Wave modules.

The ZM5202 module is based on an 8-bit 8051 CPU core, which is optimized to handle the data and link management requirements of a Z-Wave node. The patented Z-Wave protocol supports automatic retransmissions, collision avoidance mechanisms, frame acknowledgements, frame CRCs, frequency agility, and full mesh routing to ensure a highly reliable and robust wireless communication solution.

An integrated baseband controller, sub-1 GHz radio transceiver, a comprehensive set of hardware peripherals, 16kB of SRAM, and 128kB of Flash memory is available for OEM applications and the Z-Wave protocol stack.

Features

- Pad and pin compatible with the ZM3102 and ZM4102
- ITU G.9959 compliant

Module

- Optimized 8051 CPU Core
- 128kB Flash
- 16kB SRAM
- UART with speed up to 230.4kbps
- SPI with speed up to 8MHz
- 2 Interrupt Inputs
- 4-channel 12/8-bit rail-to-rail ADC with VDD/internal/external voltage reference
- PWM Output
- 10 General Purpose IOs
- Hardware AES-128 security engine
- 1000 step dimmer (TRIAC/FET)
- Power-On-Reset/Brown-out Detection
- Supply voltage range from 2.3V to 3.6V for optional battery operation
- TX mode current typ. 36mA@0dBm
- RX mode current typ. 32mA
- Normal mode current typ. 15mA
- Sleep mode current typ. 1µA
- Wake-up timer current typ. 700nA
- Less than 1ms cold start-up time

Radio Transceiver

- Receiver sensitivity with SAW filter down to -103dBm @ 9.6kbps
- Transmit power with SAW filter up to +4dBm
- Z-Wave 9.6/40/100kbps data rates
- Supports all Z-Wave sub-1 GHz frequency bands (865.2 MHz to 926.3 MHz)
- Supports multi-channel frequency agility and listen before talk
- Regulatory Compliance
  ACMA: AS/NZS 4268
  CE: EN 300 220/489
  FCC: CFR 47 Part 15
  IC: RSS-GEN/210
  MIC: ARIB STD-T108

1 CONTENT

2 OVERVIEW

The ZM5202 module is a fully integrated module containing all the hardware and firmware required to add Z-Wave functionality to OEM products. The ZM5202 module contains the SD3502 chip along with all the required passives for supply decoupling, matching, crystal and a SAW filter as illustrated in Figure 2.1. The module only requires a stable DC supply and an antenna matched to 50Ω for operation.

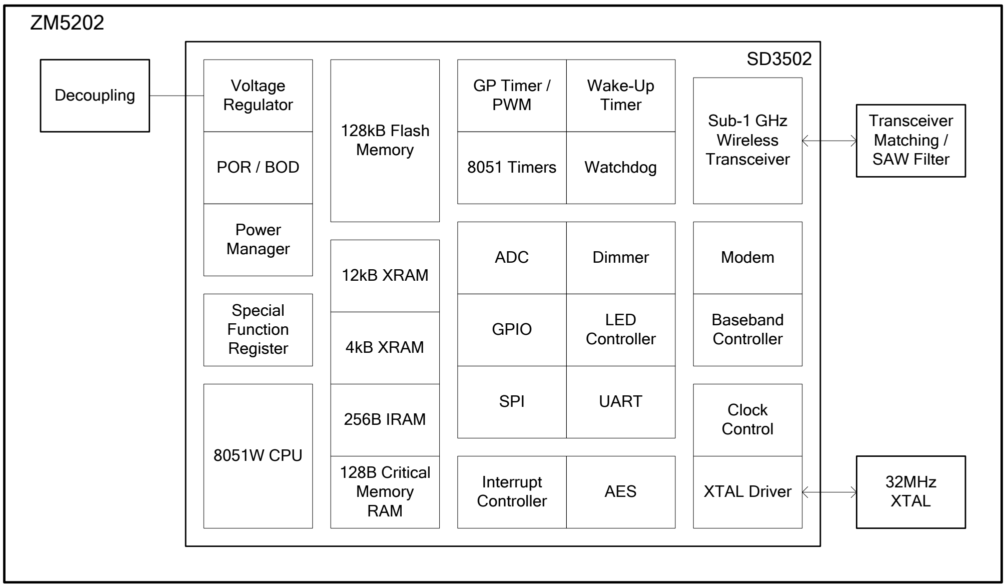


Figure 2.1: Functional block diagram

The module is verified to pass regulatory requirements and qualified to meet Z-Wave specifications. The crystal and the SAW filter are key elements that provide frequency stability of the RF output signal, and excellent RF immunity to interfering signals in the receiver path. The ZM5202 module is fully backwards compatible with the ZM4102 and ZM3102 modules in terms of the available GPIOs, hardware peripherals, and footprint. Unlike the ZM4102, it does not require a higher voltage during programming.

2.1 CPU

The CPU is binary compatible with the industry standard 803x/805x CPU and is operated at 32MHz. Its cycle performance is improved by six times relative to the standard 8051 implementation.

The CPU can be placed in 4 main modes as described in Table 2.1.

Table 2.1: CPU modes

Mode	Description
ACTIVE	• Code is executed • Peripherals are available • All I/O's are resistively pulled high • Use a short (up to 4ms) reset-low pulse to enter the reset of active state
SLEEP	• Wake-up timer available • Critical memory retention available • I/O's states according to user configuration • Use API call to enter from ACTIVE mode
PROGRAMMING DURING SUSTAINED RESET	• Used to program the internal FLASH via SPI1 • Code is not executed • All I/O's are resistively pulled high • Programming requires external control of the reset pin plus the SPI port
EXTERNAL NVM PROGRAMMING	• Used to program an external NVM (FLASH/EPROM) (optionally) wired to the SPI port • Code is not executed • All I/O's are resistively pulled high • External NVM programming requires external control of the RESET pin (plus the NVM-SPI port)

2.2 PERIPHERALS

2.2.1 ADVANCED ENCRYPTION STANDARD SECURITY PROCESSOR

The Z-Wave protocol specifies the use of Advanced Encryption Standard (AES) 128-bit block encryption for secure applications. The built-in Security Processor is a hardware accelerator that encrypts and decrypts data at a rate of 1 byte per 1.5µs. It encodes the frame payload and the message authentication code to ensure privacy and authenticity of messages. The processor supports Output FeedBack (OFB), Cipher-Block Chaining (CBC), and Electronic CodeBook (ECB) modes to target variable length messages. Payload data is streamed in OFB mode, and authentication data is processed in CBC mode as required by the Z-Wave protocol. The processor implements two efficient access methods: Direct Memory Access (DMA) and streaming through Special Function Register (SFR) ports. The processor functionality is exposed via the Z-Wave API for application use.

2.2.2 ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital Converter (ADC) is capable of sampling one of the five available input voltage sources and returns an 8 or 12-bit unsigned representation of the selected input scaled relative to the selected reference voltage, as described by the formula below.

$$ADC_{OUT} = \frac{V_{IN}}{V_{REF+} - V_{REF-}}, \qquad V_{REF-} \leq V_{IN} \leq V_{REF+}$$

The ADC is capable of operating rail to rail, while the following input configurations apply (V_{BG} = built-in Band-gap 1.25V, V_{DD} = supply voltage, V_{IN} = pin 10 and pin 13 to pin 15):

Table 2.2: ADC voltage source configuration options

Source	Description	Pin
V_{IN}	The sampling input voltage	Pin 10, pin 13, pin 14, pin15, V_{BG}
V_{REF+}	The positive node of the reference voltage	Pin 14, V_{BG}, V_{DD}
V_{REF-}	The negative node of the reference voltage	Pin 13, GND

If the sampling input voltage crosses a predefined lower or upper voltage threshold, an interrupt is triggered. Setting V_{IN} = V_{BG} and V_{RFE+} = V_{DD} implements a battery monitor. All inputs (V_{IN}, V_{REF+}, V_{REF-}) must be driven by low impedance (R_{source}) voltage sources, to suppress offsets caused by GPIO input leakage of up to 10µA.

$$R_{source} \leq \frac{V_{REF+} - V_{REF-}}{2 * |I_{INADC}| * 2^{No.\ of\ bits}}, where\ I_{INADC} = \pm 10\mu A$$

If the output impedance of the signal source is larger than R_{source}, an external buffer must be used.

2.2.3 BROWN-OUT DETECTOR / POWER-ON-RESET

When a cold start-up occurs, an internal Power-On-Reset (POR) circuit ensures that code execution does not begin unless the supply voltage is sufficient. After which, an internal Brown-Out Detector (BOD) circuit guarantees that faulty code execution does not occur by entering the reset state, if the supply voltage drops below the minimum operating level. These guarantees apply equally in both the active and sleep modes.

2.2.4 CRYSTAL DRIVER AND SYSTEM CLOCK

The system clock and RF frequencies are derived from the module mounted 32MHz crystal (XTAL), which internal system performance is factory trimmed to guarantee initial RF frequency precision. The temperature and 5 years aging margin for the internal 32MHz XTAL is 15 ppm.

2.2.5 DIMMER

The Dimmer allows you to build *leading edge* or *trailing edge* dimmers to cover dimming applications with electronic transformers, halogen or incandescent lamps, wire-wound transformers, etc. The classic leading edge method requires an external TRIAC while the more versatile and electronic transformer friendly trailing edge method requires external Field Effect Transistors (FET) or Insulated-Gate Bipolar Transistors (IGBT). The Dimmer regulates the power-on duration with a precision of 1000 steps in each 50 Hz or 60 Hz half-period. Once the Dimmer has been initialized, it will run at the requested power setting without any assistance from the MCU.

2.2.5.1 LEADING EDGE MODE

This is the classic TRIAC mode. Based on the dim-level requested, the Dimmer determines *when* and *how* the power is switched on. To ensure reliable handling in presence of inductive loads, multiple trigger pulses are automatically appended when needed.

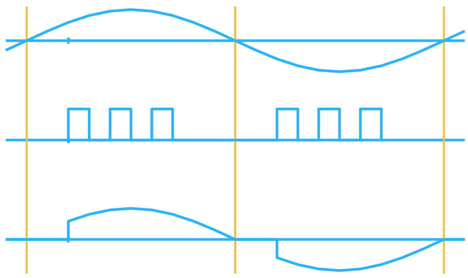


Figure 2.2: Leading edge mode (TRIAC)

2.2.5.2 TRAILING EDGE MODE

When FET/IGBT Mode is enabled, the Dimmer allows power to grow softly after each voltage zero crossing event. The Dimmer controls the turn-off time (or angle) by switching off the FET/IGBT.

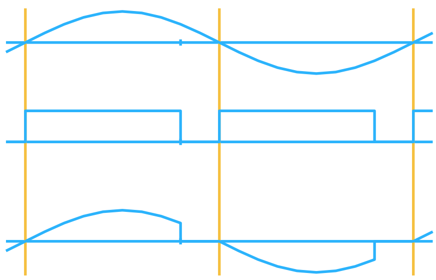


Figure 2.3: Trailing edge mode (FET/IGBT)

2.2.5.3 ZERO CROSSING SYNCHRONIZATION

The Dimmer detects and synchronizes to the AC voltage via a zero-crossing acquisition signal provided by the dimming application. This signal must be connected to pin 14 and GPIO input level compliant. Multiple single and dual event-per-cycle formats are supported. Fixed phase delays are accepted and easily compensated for through the Z-Wave API.

2.2.6 GENERAL PURPOSE INPUT/OUTPUT

There are 10 General Purpose Input/Output (GPIO) pins. These pins can be configured individually as Schmitt triggered inputs with/without internal pull-up or open-drain/push-pull outputs. The GPIO pins can be overridden by peripheral functions and each pin is able to drive loads with a minimum of 8mA.

2.2.7 GENERAL PURPOSE TIMER / PULSE WIDTH MODULATOR

A 16-bit General Purpose (GP) auto-reload timer could be provided with either an accurate 4MHz clock or an approximate 32kHz clock. It can be configured to auto-reload a predefined value and may be polled or programmed to generate an interrupt when the register wraps around. It also serves as a Pulse Width Modulated (PWM) signal generator on pin 4. A simple low frequency Digital-to-Analog Converter (DAC) could be designed using a few external passive components.

2.2.8 INTERRUPT CONTROLLER

Fifteen interrupt sources are supported, including external interrupt sources on the pin 3 and pin 4. The interrupts are shared between the user application and the Z-Wave protocol. Priorities for the interrupts are pre-assigned by the Z-Wave protocol implementation. Therefore, constraints for the user application apply.

Table 2.3: Interrupt vector table

Vector	Interrupt Name	Priority	Resources served
00	INT0	01	External interrupt 0 via pin 4
02	INT1	03	External interrupt 1 either via pin 3, or pin 3 and pin 4
04	UART0	05	UART0 end of RX or TX
05	Multi	06	AES, SPI, and many more reserved resources
06	Dimmer	07	External interrupt via ZEROX pin 14. Supported by the Dimmer API
07	General Purpose Timer	08	General Purpose Timer overflow
08	ADC	09	Battery monitor, ADC low and high monitor
09	RF	10	RF DMA
14	NMI	00	Non Maskable Interrupt for debugger and more

2.2.9 LIGHT-EMITTING DIODE CONTOLLER

The Light-Emitting Diode (LED) controller provides a single channel PWM generator on pin 5, that can be used to control the current drawn through an LED.

Table 2.4: Properties of the LED controller

Property	Description
Pulse width resolution	16-bit
Frequency	488 Hz
No. of channels	1
Placement of the pulse within a single period	Normal mode (Pulses of all channels are synchronized to the beginning of a period) Skewed mode (In each consecutive channel, pulses are shifted 25% of the period relative to the previous channel)
Drive strength	8mA

2.2.10 RESET CONTROLLER

After a reset event, the MCU is reinitialized in less than 1ms. This delay is mostly due to the charge time of the internal and external supply capacitances, and bringing the XTAL clock into a stable oscillation. Multiple events may cause a reset. Therefore, the actual cause is latched by hardware and may be retrieved via software when the system resumes operation. Some reset methods deliberately leave the state of GPIO pins unchanged, while other GPIO pins are set to high impedance with an internal pull-up.

Table 2.5: Supported reset methods

Reset Cause	Description	GPIO state	Maskable
BOR	Reset request generated by Brown-Out-Reset hardware	High impedance with pull-up	No
INT1	Reset request generated when a signal is received on pin INT1, when the chip is in power down mode	Unchanged	Yes
POR	Reset request generated by Power-On-Reset hardware	High impedance with pull-up	No
RESET_N	Reset request generated by the RESET_N pin being de-asserted	High impedance with pull-up	No
Software	Reset request generated in software.	Unchanged	Yes
WATCHDOG	Reset request generated by the WATCHDOG Timer timing out	High impedance with pull-up	Yes
WUT	Reset request generated by the Wake-Up-Timer timing out	Unchanged	Yes

2.2.11 SERIAL PERIPHERAL INTERFACE

SPI1 Serial Peripheral Interface enables synchronous data transfers between devices.

Table 2.6: SPI1 signal modes

SPI1 Signal	SPI1 Function, master
MOSI	Data output
MISO	Data input
SCK	Clock output

During data transmission, SCK acts as a clock, while 8 bits of data are exchanged between the two devices within 8 cycles of SCK.

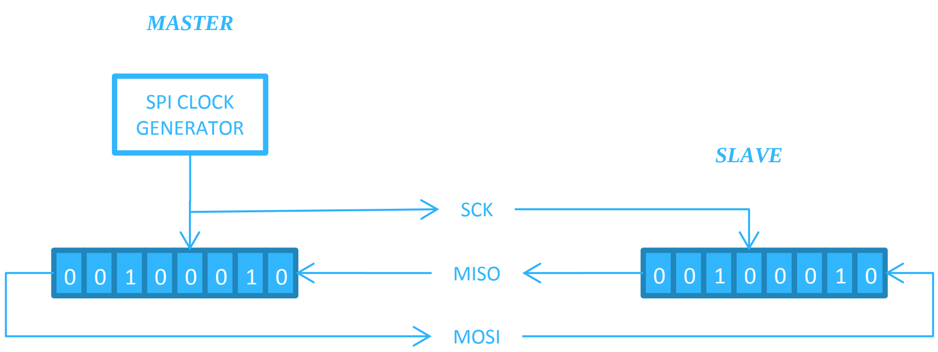


Figure 2.4: Flow of data between SPI master and slave

The module acts as a SPI master when controlling an external Non-Volatile Memory (NVM). The slave select (or chip select) of the external NVM could be driven by an available GPIO. SPI1 slave mode is reserved for In-System Programming (ISP). Therefore, SPI1 can only be used as a master.

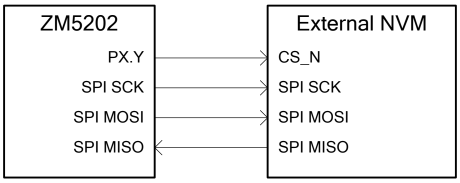


Figure 2.5: Typical interface to slave device

2.2.12 TIMERS

Timer 0 and Timer 1 are 16-bit counters that can be clocked from a fixed internal source or an external source. Except for the use of external gating signals, the complete set of classic 8051 T0/T1 features is available.

Table 2.7: Timer sources

Timer	Fixed Internal Source	External Source
Timer 0	16 MHz	Pin 10
Timer 1	16 MHz	Pin 15

2.2.13 UNIVERSAL ASYNCHRONOUS RECEIVER / TRANSMITTER

The Universal Asynchronous Receiver / Transmitter (UART) is a hardware block operating independently of the 8051 CPU. It offers full-duplex data exchange, up to 230.4kbps, with an external host microcontroller requiring an industry standard NRZ asynchronous serial data format. The UART0 interface is available over pin 10 and pin15. A data byte is shifted as a start bit, 8 data bits (lsb first), and a stop bit, respectively, with no parity and hardware handshaking. Figure 2.6 shows the waveform of a single serial byte. The UART is compliant with RS-232 when an external level converter is used.

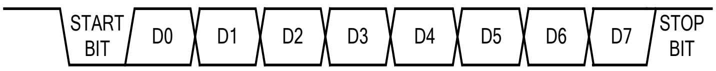


Figure 2.6: UART waveform

2.2.14 WAKE-UP TIMER

The Wake-Up Timer (WUT) plays an important role in maximizing battery life of applications like Frequently Listening Routing Slave (FLiRS) Z-Wave nodes. It is available to customer applications via the Z-Wave API, and can be configured to wake a sleeping node after 1 to 256 seconds. The programming resolution equals 8-bit fractions of 2 seconds, alternatively 8-bit fractions of 256 seconds. The WUT is automatically calibrated to the system clock when it is operational, maintaining an accuracy of <2%.

2.2.15 WATCHDOG

The watchdog helps prevents the CPU from entering a deadlock state. A timer that is enabled by default achieves this by triggering a reset event in case it overflows. The timer overflows in 1 second, therefore it is essential that the software clear the timer periodically. The watchdog is disabled when the chip is in power down mode, and automatically restarts with a cleared timer when waking up to the active mode.

2.2.16 WIRELESS TRANSCEIVER

The wireless transceiver is a sub-1 GHz ISM narrowband FSK radio, a modem, and a baseband controller. This architecture provides an all-digital direct synthesis transmitter and a low IF digital receiver. The Z-Wave protocol currently utilizes 2-key FSK/GFSK modulation schemes at 9.6/40/100 kbps data rates throughout a span of carrier frequencies from 865.2 to 926.3MHz.

The output power of the transmitter is configurable in the range -26dBm to +4dBm (V_{DD} = 2.3V to 3.6V, T_A = -10°C to +85°C). An external front-end could be used to further increase the link budget if necessary.

2.3 MEMORY MAP

Figure 2.7 shows an illustration of the byte wise addressable memories that are shared between the user application and the Z-Wave protocol stack. Additional ROM and NVR areas are used for boot code, calibration data, production data, and lock bytes.

Table 2.8: Description of memory blocks

ID	Memory	Address Method	Exposed during Programming	Description
M1-M4	128kB Flash	Program Memory	Yes	Flash memory, mapped in 3 banks of 32kB slices over a 32kB common block, one read access per 2 clock cycles.
M5-M6	16kB RAM	XRAM	Yes	SRAM's split into 4kB and 12kB contiguous blocks
M7	256B RAM	IRAM	No	Bit addressable SRAM
M8	128B RAM	XRAM	No	Critical SRAM for data persistency during sleep mode
M9	256B NVM	(API)	No	Cached high endurance non-volatile data registers
M10	256B NVR	(API)	Yes	Flash area reserved for the Z-Wave protocol, calibration data, production data, and lock bytes

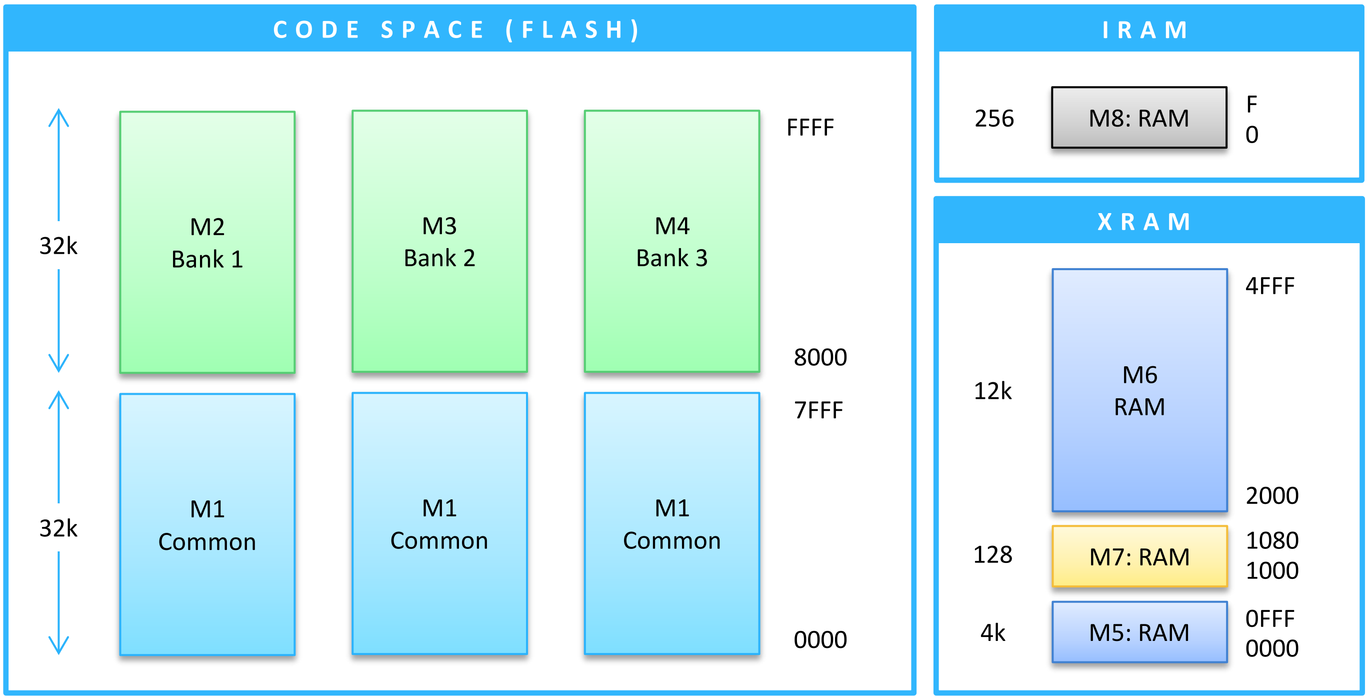


Figure 2.7: Non-API addressable memory blocks

2.4 MODULE PROGRAMMING

The code space and the NVR of the flash can be programmed and/or read through the SPI1 interface. [1]

2.4.1 ENTERING IN-SYSTEM PROGRAMMING MODE

The module can be placed into the In-System Programming (ISP) mode by asserting the active low RESET_N signal for 5.2ms. The programming unit of the module then waits for the “Interface Enable” serial command before activating the ISP mode over the SPI1.

2.5 POWER SUPPLY REGULATOR

While the supply to the digital I/O circuits is unregulated, on-chip low-dropout regulators derive all the 1.5 V and 2.5 V internal supplies required by the Micro-Controller Unit (MCU) core logic, non-volatile data registers, flash, and the analogue circuitry.

3 TYPICAL APPLICATION

An illustration of an application example using the ZM5202 module implementation follows. It is strongly recommended that the power supply is decoupled sufficiently, and a pull-up resistor placed on the RESET_N signal if the host GPIO is unable to drive it.

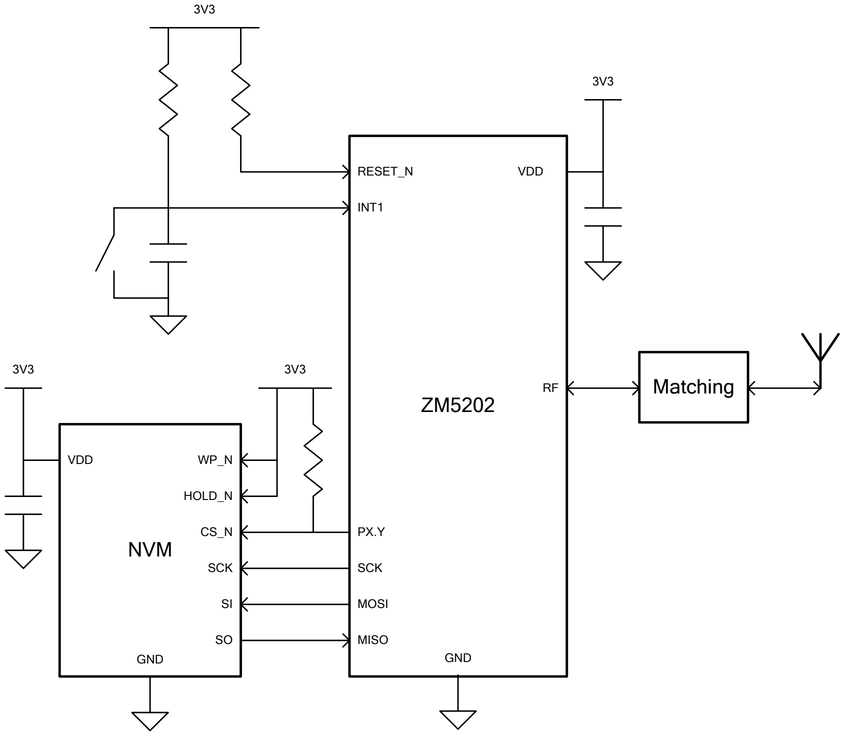


Figure 3.1: Example of a standalone application with an external antenna

4 PIN CONFIGURATION

The layout of the pins on the ZM5202 module is shown in Figure 4.1.

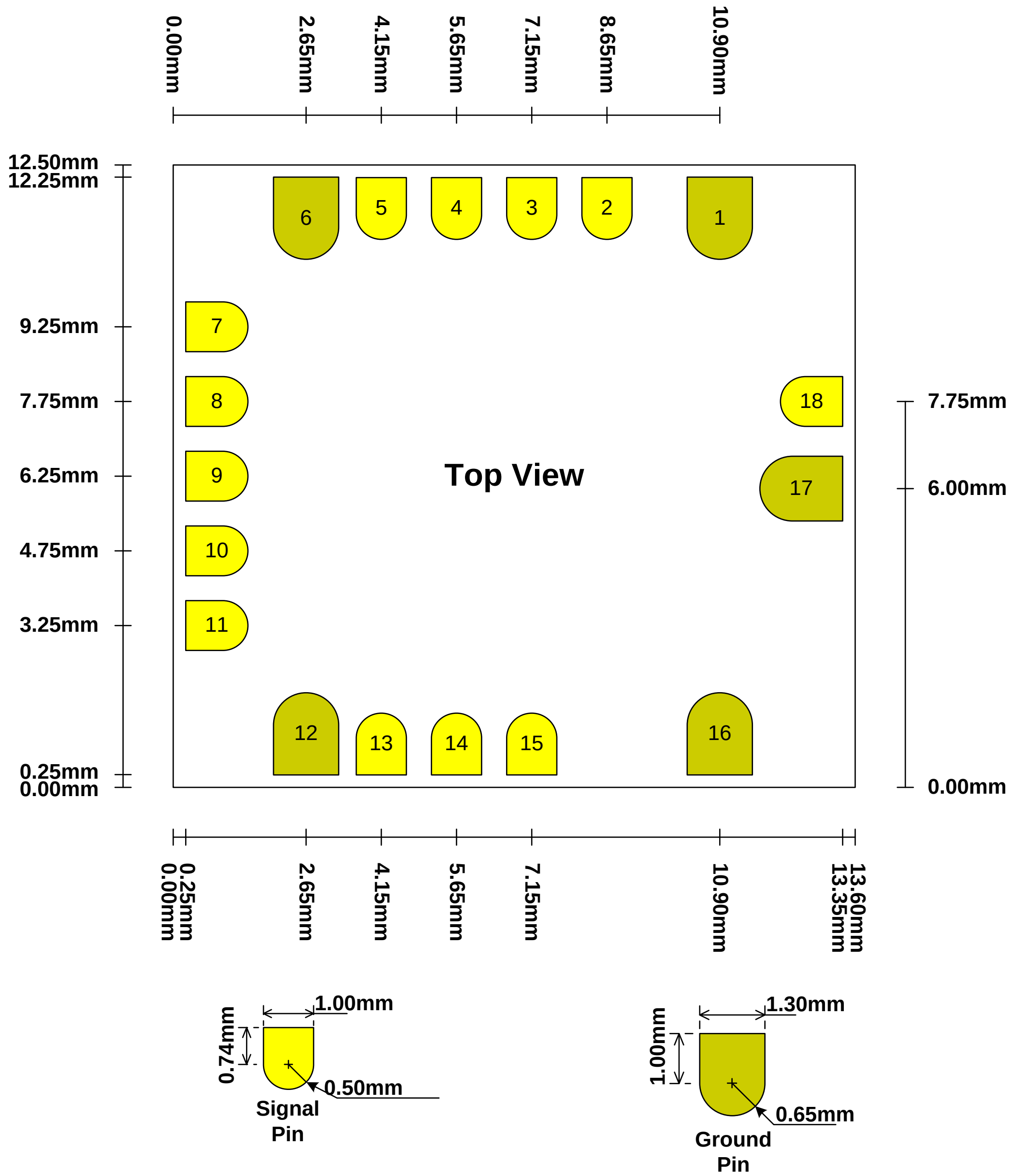


Figure 4.1: Pin layout (top view)

4.1 PIN FUNCTIONALITY

Table 4.1: Power and ground signals

Pin Name	Pin Location	Type[1]	Function
V_{DD}	11	S	Module power supply.
GND	1, 6, 12, 16, 17	S	Ground. Must be connected to the ground plane.

Table 4.2: Module control signal

Pin Name	Pin Location	Type	Function
RESET_N	2	I	Active low signal that places the module in a reset/programmable state.

Table 4.3: SPI1 interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
SPI1 SCK	8	O	SPI1 Clock input with internal pull-up.	SPI1 Clock. Output in master mode.
SPI1 MISO	7	I	Serial data transmit when in SPI1 ISP mode, high impedance otherwise with internal pull-up.	Master-In-Slave-Out serial data. Input in master mode.
SPI1 MOSI	9	O	Waits for the ”Interface Enable” serial command after 5.2ms. Enters SPI1 ISP mode after command is received from the host.	Master-Out-Slave-In serial data. Output in master mode.

Table 4.4: UART0 interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
UART0 RX	10	I	High impedance with internal pull-up.	Receive data from host serial port.
UART0 TX	15	O	High impedance with internal pull-up.	Transmit data to host serial port.

Table 4.5: ADC interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
ADC0	10	I	High impedance with internal pull-up.	Analog-to-Digital converter input.
ADC1	15	I	High impedance with internal pull-up.	Analog-to-Digital converter input.
ADC2	13	I	High impedance with internal pull-up.	Analog-to-Digital converter input or lower reference voltage.
ADC3	14	I	High impedance with internal pull-up.	Analog-to-Digital converter input or higher reference voltage.

[1] I = Input, O = Output, D+ = Differential Plus, D- = Differential Minus, S = Supply

Table 4.6: External interrupt interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
INT0	4	I	High impedance with internal pull-up.	External interrupt 0 input. High priority.
INT1	3, 4	I	High impedance with internal pull-up.	External interrupt 1 input. Low priority.

Table 4.7: PWM signal

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
PWM	4	O	High impedance with internal pull-up.	Pulse width modulator output.

Table 4.8: LED controller interface signal

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
PWM LED0	5	O	High impedance with internal pull-up.	LED controller output.

Table 4.9: Dimmer interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
TRIAC	13	O	High impedance with internal pull-up.	Dimmer output. Firing pulse to TRIAC/FET/IGBT.
ZEROX	14	I	High impedance with internal pull-up.	Zero-cross detection input.

Table 4.10: Timer interface signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
T0 EXT CLK	10	I	High impedance with internal pull-up.	Timer 0 external clock input.
T1 EXT CLK	15	I	High impedance with internal pull-up.	Timer 1 external clock input.

Table 4.11: RF interface signal

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
RF[2]	18	I/O	High impedance with internal pull-up.	RF input and output.

[2] Caution: pin is sensitive to electro-static discharge

Table 4.12: GPIO signals

Pin Name	Pin Location	Type	Function in Reset State	Function in Active State
P0.4	5	I/O	High impedance with internal pull-up.	General purpose input and output.
P1.0	4	I/O	High impedance with internal pull-up.	General purpose input and output.
P1.1	3	I/O	High impedance with internal pull-up.	General purpose input and output.
P2.2	9	I/O	Waits for the ”Interface Enable” serial command after 5.2ms. Enters SPI1 ISP mode after command is received from the host.	General purpose input and output.
P2.3	7	I/O	Serial data transmit when in SPI1 ISP mode, high impedance with internal pull-up otherwise.	General purpose input and output.
P2.4	8	I/O	Programmer clock input with internal pull-up.	General purpose input and output.
P3.4	10	I/O	High impedance with internal pull-up.	General purpose input and output.
P3.5	15	I/O	High impedance with internal pull-up.	General purpose input and output.
P3.6	13	I/O	High impedance with internal pull-up.	General purpose input and output.
P3.7	14	I/O	High impedance with internal pull-up.	General purpose input and output.

5 ELECTRICAL CHARACTERISTICS

This section describes the electrical parameters of the ZM5202 module.

5.1 TEST CONDITIONS

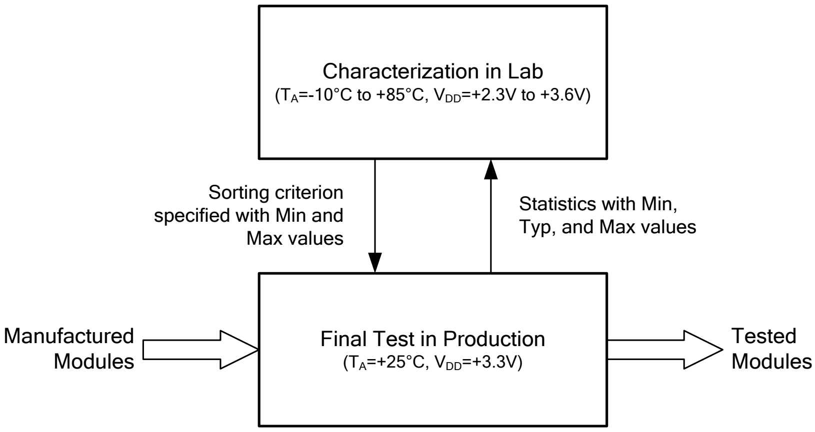


Figure 5.1: Testing flow

The following conditions apply for characterization in the lab, unless otherwise noted.

1. Ambient temperature T_A = -10°C to +85°C
2. Supply voltage V_{DD} = +2.3V to +3.6V
3. All tests are carried out on the ZDB5202 Z-Wave Development Board. [2]
4. Conducted transmission power is measured with the SAW filter for 868.4, 908.4, 919.8, and 921.4MHz at 50Ω
5. Conducted receiver sensitivity is measured with the SAW filter for 868.4, 908.4, 919.8, and 921.4MHz at 50Ω

The following conditions apply for the final test in production, unless otherwise noted.

1. Ambient temperature T_A = +25°C
2. Supply voltage V_{DD} = +3.3V
3. Conducted transmission power is measured with the SAW filter for 868.4, 908.4, 919.8, and 921.4MHz at 50Ω
4. Conducted receiver sensitivity is measured with the SAW filter for 868.4, 908.4, 919.8, and 921.4MHz at 50Ω

5.1.1 TYPICAL VALUES

Unless otherwise specified, typical data refer to the mean of a data set measured at an ambient temperature of T_A=25°C and supply voltage of V_{DD}=+3.3V.

5.1.2 MINIMUM AND MAXIMUM VALUES

Unless otherwise specified the minimum and maximum values are guaranteed in the worst conditions of ambient temperature, supply voltage and frequencies by a final test in production on 100% of the devices at an ambient temperature of T_A=25°C and supply voltage of V_{DD}=+3.3V.

For data based on measurements, the minimum and maximum values represent the mean value plus or minus three times the standard deviation (μ±3σ).

5.2 ABSOLUTE MAXIMUM RATINGS

The absolute ratings specify the limits beyond which the module may not be functional. Exposure to absolute maximum conditions for extended periods may cause permanent damage to the module.

Table 5.1: Voltage characteristics

Symbol	Description	Min	Max	Unit
V_{DD-GND}	Main supply voltage	-0.3	+3.6	V
V_{IN-GND}	Voltage applied on any I/O pin	-0.3	+3.6	V
I_{IN}	Current limit when over driving the input (V_{IN-GND} > V_{DD-GND})	-	+20.0	mA
P_{RF-IN}	Radio receiver input power	-	+10.0	dBm
ESD_{HBM}	JEDEC JESD22-A114F Human Body Model	-	+2000.0	V
ESD_{MM}	JEDEC JESD22-A115C Machine Model	-	+200.0	V
ESD_{CDM}	JEDEC JESD22-C101E Field-Induced Charged-Device Model	-	+500.0	V

Table 5.2: Current characteristics

Symbol	Description	Min	Max	Unit
I_{VDD}	Current into V_{DD} power supply pin	-	+120	mA
I_{GND}	Sum of the current out of all GND ground pins	-120	-	mA

Table 5.3: Thermal characteristics

Symbol	Description	Min	Max	Unit
T_J	Junction temperature	-55	+125	°C

5.3 GENERAL OPERATING RATINGS

The operating ratings indicate the conditions where the module is guaranteed to be functional.

Table 5.4: Recommended operating conditions

Symbol	Description	Min	Typ	Max	Unit
V_{DD}	Standard operating supply voltage	+2.3	+3.3	+3.6	V
f_{SYS}	Internal clock frequency	-	32.0	-	MHz
T_A	Ambient operating temperature	-10.0	+25.0	+85.0	°C

5.4 CURRENT CONSUMPTION

Measured at an ambient temperature of TA=-10°C to +85°C and a supply voltage of VDD=+2.3V to +3.6V.

Table 5.5: Current consumption in active modes

Symbol	Description	Min	Typ	Max	Unit
I_{DD_ACTIVE}	MCU running at 32MHz	-	14.9	15.9	mA
I_{DD_RX}	MCU and radio receiver active	-	32.4	35.1	mA
$I_{DD\_TX\_-26}$	MCU and radio transmitter active, -26dBm	-	27.5	-	mA
$I_{DD\_TX\_4}$	MCU and radio transmitter active, +4dBm	-	42.1	-	mA

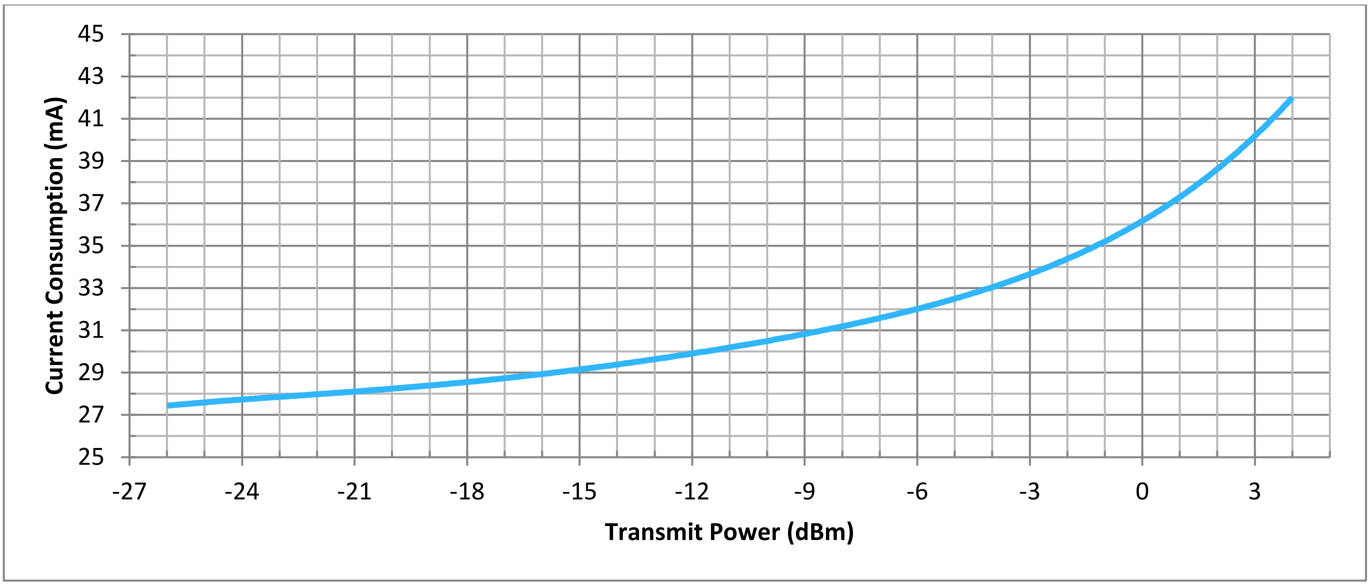


Figure 5.2: Typical current consumption vs. transmit power

Table 5.6: Current consumption in power saving modes

Symbol	Description	Min	Typ	Max	Unit
I_{DD_SLEEP}	Module in sleep state	-	1.0	-	µA
I_{DD_WUT}	Module in sleep state with wake-up timer active	-	2.0	-	µA
$I_{DD\_WUT\_RAM}$	Module in sleep state with wake-up timer and 128 bytes of critical RAM active	-	2.1	-	µA

Table 5.7: Current consumption during programming

Symbol	Description	Min	Typ	Max	Unit
$I_{DD\_PGM\_SPI}$	Programming via SPI1	-	15	-	mA

5.5 SYSTEM TIMING

Measured at an ambient temperature of T_A=-10°C to +85°C and a supply voltage of V_{DD}=+2.3V to +3.6V.

Table 5.8: Transition between operating modes

Symbol	Description	Min	Typ	Max	Unit
t_{ACTIVE_SLEEP}	Transition time from the active state to the sleep state	-	-	125	ns
t_{SLEEP_ACTIVE}	Transition time from the sleep state to the active state ready to execute code	-	-	160	µs

Table 5.9: System start-up time

Symbol	Description	Min	Typ	Max	Unit
V_{POR}	Power-on-Reset (POR) threshold on rising supply voltage at which the reset signal is deasserted	-	-	+2.3	V
t_{RESET_ACTIVE}	Transition time from the reset state to the active state ready to execute code with a power rise time not exceeding 10µs	-	-	1.0	ms

Table 5.10: Wake-up timer accuracy

Symbol	Description	Min	Typ	Max	Unit
t_{WUT_OFFSET}	Wake-up timer offset, Y-axis intercept of time vs. setting curve	-	-	40	ms
t_{WUT_SCALE}	Wake-up timer absolute error	-	-	2	%

Table 5.11: Reset timing requirements

Symbol	Description	Min	Typ	Max	Unit
t_{RST_PULSE}	Duration to assert RESET_N to guarantee a full system reset	20	-	-	ns

Table 5.12: Programming time

Symbol	Description	Min	Typ	Max	Unit
t_{ERASE_FULL}	Time taken to erase the entire flash memory	-	-	44.1	ms
t_{PGM_FULL}	Time taken to program the entire flash memory over SPI1 at 4MHz including a full erase	-	-	1.4	s

5.6 NON-VOLATILE MEMORY

Qualified for an ambient temperature of T_A=+25°C and a supply voltage of V_{DD}=+3.3V. The on-chip memory is based on SuperFlash® technology.

Table 5.13: On-chip flash

Symbol	Description	Min	Typ	Max	Unit
END_{FLASH}	Endurance, erase cycles before failure	10000	-	-	cycles
$RET_{FLASH-LT}$	Data retention	100	-	-	years
$RET_{FLASH-HT}$	Data retention *(Qualified for a junction temperature of T_J=-10°C to +85°C)*	10	-	-	years

Table 5.14: On-chip M9 high endurance NVM

Symbol	Description	Min	Typ	Max	Unit
END_{NVM}	Endurance, erase cycles before failure	100000	-	-	cycles
RET_{NVM-LT}	Data retention	100	-	-	years
RET_{NVM-HT}	Data retention *(Qualified for a junction temperature of T_J=-10°C to +85°C)*	10	-	-	years

5.7 ANALOG-TO-DIGITAL CONVERTER

Measured at an ambient temperature of T_A=-10°C to +85°C and a supply voltage of V_{DD}=+2.3V to +3.6V.

Table 5.15: 12 bit ADC characteristics

Symbol	Description	Min	Max	Unit
V_{BG}	Internal reference voltage	+1.20	+1.30	V
V_{REF+}	Upper reference input voltage	V_{DD} - 0.90	V_{DD}	V
V_{REF-}	Lower reference input voltage	0.00	+1.20	V
I_{ADCIN}	Input current *($0 \le V_{IN} \le V_{DD}$)*	-10.00	+10.00	µA
DNL_{ADC}	Differential non-linearity	-1.00	+1.00	LSB
ACC_{8b}	Accuracy when sampling 20ksps with 8 bit resolution	-2.00	+2.00	LSB
ACC_{12b}	Accuracy when sampling 10ksps with 12 bit resolution	-5.00	+5.00	LSB
f_{S-8b}	8 bit sampling rate	-	0.02	Msps
f_{S-12b}	12 bit sampling rate	-	0.01	Msps

5.8 GENERAL PURPOSE INPUT OUTPUT

Measured at an ambient temperature of T_A=-10°C to +85°C.

Table 5.16: Digital input characteristics, supply voltage of V_{DD}=+2.3V to +3.0V

Symbol	Description	Min	Max	Unit
V_{IH}	Logical 1 input voltage high level	+1.85	-	V
V_{IL}	Logical 0 input voltage low level	-	+0.75	V
V_{IF}	Falling input trigger threshold	+0.75	+1.05	V
V_{IR}	Rising edge trigger threshold	+1.35	+1.85	V
V_{HYS}	Schmitt trigger voltage hysteresis	+0.55	+0.85	V
I_{IH}	Logical 1 input high level current leakage	-	+7.00	µA
I_{IL-NPU}	Logical 0 input low level current leakage *(no internal pull-up resistor)*	-7.00	-	µA
I_{IL-PU}	Logical 0 input low level current leakage *(with internal pull-up resistor)*	+35.00	+90.00	µA
PU_{IN}	Internal pull-up resistance *(T_A=+25°C)*	20.00	30.00	kΩ
C_{IN}	Pin input capacitance	-	15.00	pF

Table 5.17: Digital output characteristics, supply voltage of V_{DD}=+2.3V to +3.0V

Symbol	Description	Min	Max	Unit
V_{OH}	Logical 1 output voltage high level	+1.9	-	V
V_{OL}	Logical 0 output voltage low level	-	+0.4	V
I_{OH-LP}	Logical 1 output high level current sourcing	-	+6.0	mA
I_{OL-LP}	Logical 0 output low level current sinking	-6.0	-	mA
I_{OH-HP}	Logical 1 output high level current sourcing *(pin 10 and pin 13 to pin 15)*	-	+12.0	mA
I_{OL-HP}	Logical 0 output low level current sinking *(pin 10 and pin 13 to pin 15)*	-12.0	-	mA

Table 5.18: Digital input characteristics, supply voltage of V_{DD}=+3.0V to +3.6V

Symbol	Description	Min	Max	Unit
V_{IH}	Logical 1 input voltage high level	+2.10	-	V
V_{IL}	Logical 0 input voltage low level	-	+0.90	V
V_{IF}	Falling input trigger threshold	+0.90	+1.30	V
V_{IR}	Rising edge trigger threshold	+1.60	+2.10	V
V_{HYS}	Schmitt trigger voltage hysteresis	+0.65	+0.95	V
I_{IH}	Logical 1 input high level current leakage	-	+10.00	µA
I_{IL-NPU}	Logical 0 input low level current leakage *(no internal pull-up resistor)*	-10.00	-	µA
I_{IL-PU}	Logical 0 input low level current leakage *(with internal pull-up resistor)*	+40.00	+120.00	µA
PU_{IN}	Internal pull-up resistance *(T_A=+25°C)*	15.00	20.00	kΩ
C_{IN}	Pin input capacitance	-	15.00	pF

Table 5.19: Digital output characteristics, supply voltage of V_{DD}=+3.0V to +3.6V

Symbol	Description	Min	Max	Unit
V_{OH}	Logical 1 output voltage high level	+2.4	-	V
V_{OL}	Logical 0 output voltage low level	-	+0.4	V
I_{OH-LP}	Logical 1 output high level current sourcing	-	+8.0	mA
I_{OL-LP}	Logical 0 output low level current sinking	-8.0	-	mA
I_{OH-HP}	Logical 1 output high level current sourcing *(pin 10 and pin 13 to pin 15)*	-	+16.0	mA
I_{OL-HP}	Logical 0 output low level current sinking *(pin 10 and pin 13 to pin 15)*	-16.0	-	mA

5.9 RF CHARACTERISTICS

5.9.1 TRANSMITTER

Measured at an ambient temperature of T_A=-10°C to +85°C and a supply voltage of V_{DD}=+2.3V to +3.6V. The transmission power is adjusted by setting the value of the RFPOW register.

Table 5.20: Transmitter performance

Symbol	Description	Min	Typ	Max	Unit
P_{63}	RF output power delivered to the antenna, RFPOW=63	+2.9	+4.0	-	dBm
P_{01}	RF output power delivered to the antenna, RFPOW=01	-29.0	-26.1	-	dBm
P_{H2-63}	2nd harmonic, RFPOW=63	-	-57.3	-	dBc
P_{H2-48}	2nd harmonic, RFPOW=48	-	-60.2	-	dBc
P_{H2-32}	2nd harmonic, RFPOW=32	-	-61.9	-	dBc
P_{H2-20}	2nd harmonic, RFPOW=20	-	-59.6	-	dBc
P_{H2-8}	2nd harmonic, RFPOW=8	-	-51.3	-	dBc
P_{H3-63}	3rd harmonic, RFPOW=63	-	-45.4	-	dBc
P_{H3-48}	3rd harmonic, RFPOW=48	-	-45.8	-	dBc
P_{H3-32}	3rd harmonic, RFPOW=32	-	-45.6	-	dBc
P_{H3-20}	3rd harmonic, RFPOW=20	-	-47.6	-	dBc
P_{H3-8}	3rd harmonic, RFPOW=8	-	-46.6	-	dBc
PN_{30kHz}	Phase noise at 30kHz	-	-88.1	-	dBc/Hz
PN_{100kHz}	Phase noise at 100kHz	-	-95.2	-	dBc/Hz
PN_{1MHz}	Phase noise at 1MHz	-	-107.3	-	dBc/Hz
PN_{10MHz}	Phase noise at 10MHz	-	-113.1	-	dBc/Hz
PN_{20MHz}	Phase noise at 100MHz	-	-113.8	-	dBc/Hz
$BW_{9.6}$	Channel bandwidth, 9.6kbps	-	90.0	-	kHz
BW_{40}	Channel bandwidth, 40kbps	-	90.0	-	kHz
BW_{100}	Channel bandwidth, 100kbps	-	110.0	-	kHz

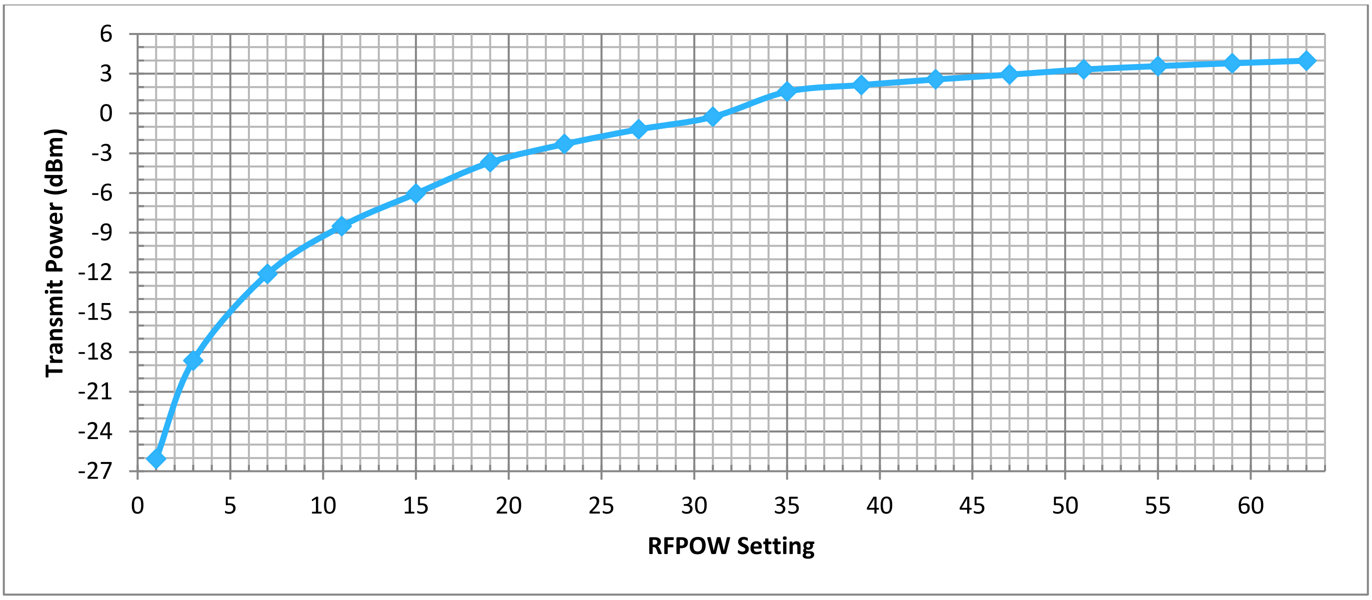


Figure 5.3: Typical transmit power vs. RFPOW setting

The transmitter is calibrated from factory. Refer to [3] for more information.

5.9.2 RECEIVER

Measured over an ambient temperature of T_A=+25°C and a supply voltage of V_{DD}=+2.3V to +3.6V.

Table 5.21: Receiver sensitivity

Symbol	Description	Min	Typ	Max	Unit
$P_{9.6}$	Sensitivity at 9.6kbps, FER < 1%	-	-102.7	-101.0	dBm
P_{40}	Sensitivity at 40kbps, FER < 1%	-	-99.0	-97.2	dBm
P_{100}	Sensitivity at 100kbps, FER < 1%	-	-93.0	-91.8	dBm

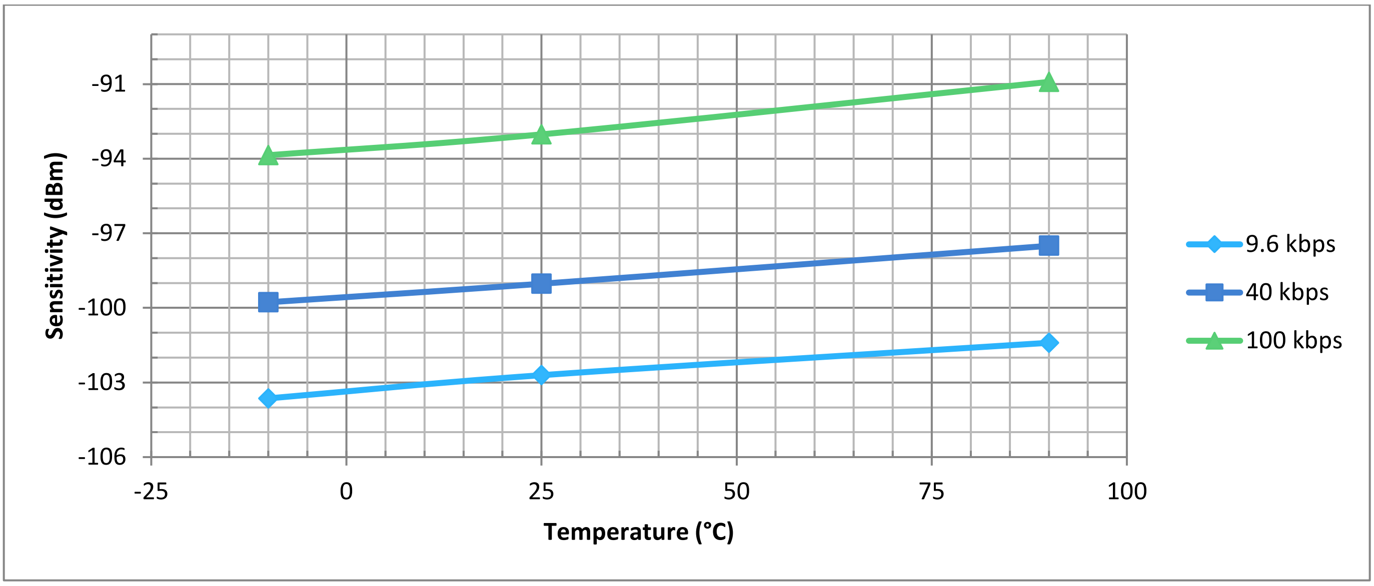


Figure 5.4: Typical sensitivity vs. temperature

Table 5.22: Receiver performance

Symbol	Description	Min	Typ	Max	Unit
$CCR_{9.6}$	Co-channel rejection, 9.6kbps	-	-3.9	-	dBc
$BI_{1MHZ-9.6}$	Blocking immunity[3] at Δf=1MHz, 9.6kbps	-	43.5	-	dBc
$BI_{2MHZ-9.6}$	Blocking immunity at Δf=2MHz, 9.6kbps	-	52.6	-	dBc
$BI_{5MHZ-9.6}$	Blocking immunity at Δf=5MHz, 9.6kbps	-	70.6	-	dBc
$BI_{10MHZ-9.6}$	Blocking immunity at Δf=10MHz, 9.6kbps	-	73.9	-	dBc
$BI_{100MHZ-9.6}$	Blocking immunity at Δf=100MHz, 9.6kbps	-	85.7	-	dBc
CCR_{40}	Co-channel rejection, 40kbps	-	-9.1	-	dBc
$BI_{1MHZ-40}$	Blocking immunity at Δf=1MHz, 40kbps	-	40.2	-	dBc
$BI_{2MHZ-40}$	Blocking immunity at Δf=2MHz, 40kbps	-	48.0	-	dBc
$BI_{5MHZ-40}$	Blocking immunity at Δf=5MHz, 40kbps	-	65.2	-	dBc
$BI_{10MHZ-40}$	Blocking immunity at Δf=10MHz, 40kbps	-	67.7	-	dBc
$BI_{100MHZ-40}$	Blocking immunity at Δf=100MHz, 40kbps	-	82.0	-	dBc
CCR_{100}	Co-channel rejection, 100kbps	-	-8.1	-	dBc
$BI_{1MHZ-100}$	Blocking immunity at Δf=1MHz, 100kbps	-	30.2	-	dBc
$BI_{2MHZ-100}$	Blocking immunity at Δf=2MHz, 100kbps	-	35.2	-	dBc
$BI_{5MHZ-100}$	Blocking immunity at Δf=5MHz, 100kbps	-	59.0	-	dBc
$BI_{10MHZ-100}$	Blocking immunity at Δf=10MHz, 100kbps	-	62.6	-	dBc
$BI_{100MHZ-100}$	Blocking immunity at Δf=100MHz, 100kbps	-	76.0	-	dBc
$RSSI_{RANGE}$	Dynamic range of the RSSI measurement	-	70.0	-	dB
$RSSI_{LSB}$	Resolution of the RSSI measurement	-	1.5	-	dB
P_{LO}	LO leakage at Δf=200kHz and Δf=325kHz	-	-84.4	-80.0	dBm
IIP3	Input 3rd order intercept point	-	-12.0	-	dBm
$BW_{9.6}$	Intermediate frequency filter bandwidth, 9.6kbps	-	300.0	-	kHz
BW_{40}	Intermediate frequency filter bandwidth, 40kbps	-	300.0	-	kHz
BW_{100}	Intermediate frequency filter bandwidth, 100kbps	-	600.0	-	kHz

[3] Blocker level is defined relative to the wanted receiving signal and measured with the wanted receiving signal 3dB above the sensitivity level

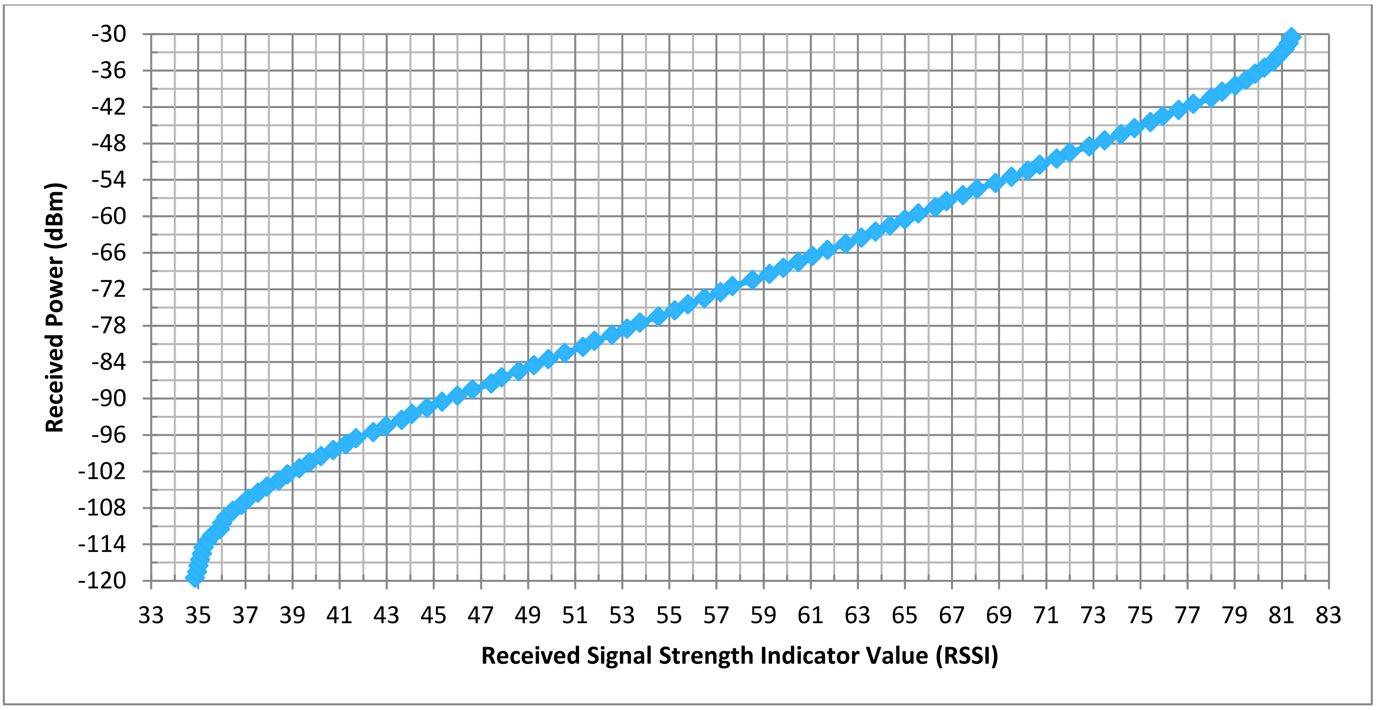


Figure 5.5: Typical input power vs. RSSI value

First-order approximation:

$$Received\ Power\ [dBm] \approx 1.56 \times RSSI - 161.45, \qquad where\ RSSI \in [40,80]$$

5.9.3 REGULATORY COMPLIANCE

The ZM5202 has been tested on the ZDP03A Z-Wave Development Platform to be compliant with the following regulatory standards. [4]

- **ACMA COMPLIANCE**
  - AS/NZS 4268
  - CISPR 22
- **CE COMPLIANCE**
  - EN 300 220-1/2
  - EN 301 489-1/3
  - EN 55022
  - EN 60950-1
  - EN 61000-4-2/3
  - EN 62479
- **FCC COMPLIANCE**
  - FCC CFR 47 Part 15 Subpart C §15.249
- **IC COMPLIANCE**
  - RSS-GEN
  - RSS-210
  - ANSI C63.10
- **MIC COMPLIANCE**
  - ARIB STD-T108

6 Z-WAVE FREQUENCIES

Table 6.1: Z-Wave RF specification

Data rate	9.6kbps	40kbps	100kbps	
Modulation	Frequency Shift Keying (FSK)	FSK	Gaussian Frequency Shift Keying (GFSK)	
Frequency deviation	f_C±20kHz	f_C±20kHz	f_C±29.3kHz	
Frequency accuracy	f_C±13ppm	f_C±13ppm	f_C±13ppm	
Coding	Manchester encoded	Non-return to Zero (NRZ)	NRZ	
United Arab Emirates	868.42 MHz	868.40 MHz	869.85 MHz	E
Australia	921.42 MHz	921.40 MHz	919.80 MHz	H
Brazil	921.42 MHz	921.40 MHz	919.80 MHz	H
Canada	908.42 MHz	908.40 MHz	916.00 MHz	U
Chile	908.42 MHz	908.40 MHz	916.00 MHz	U
China	868.42 MHz	868.40 MHz	869.85 MHz	E
European Union	868.42 MHz	868.40 MHz	869.85 MHz	E
Hong Kong	919.82 MHz	919.80 MHz	919.80 MHz	H
Israel	916.02 MHz	916.00 MHz	-	U
India	865.20 MHz	865.20 MHz	865.20 MHz	E
Japan	-	-	922.50 MHz	H
	-	-	923.90 MHz	H
	-	-	926.30 MHz	H
Korea	-	-	920.90 MHz	H
	-	-	921.70 MHz	H
	-	-	923.10 MHz	H
Mexico	908.42 MHz	908.40 MHz	916.00 MHz	U
Malaysia	868.12 MHz	868.10 MHz	868.10 MHz	E
New Zealand	921.42 MHz	921.40 MHz	919.80 MHz	H
Russia	869.02 MHz	869.00 MHz	-	E
Singapore	868.42 MHz	868.40 MHz	869.85 MHz	E
Taiwan	-	-	922.50 MHz	H
	-	-	923.90 MHz	H
	-	-	926.30 MHz	H
United States	908.42 MHz	908.40 MHz	916.00 MHz	U
South Africa	868.42 MHz	868.40 MHz	869.85 MHz	E

7 MODULE INFORMATION

7.1 MODULE MARKING

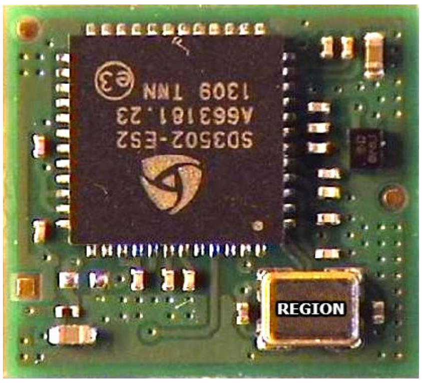


Figure 7.1: Marking placement

Table 7.1: Marking description

Regional information	REGION: E U H

7.2 MODULE DIMENSIONS

Table 7.2: Dimensions

Length	13.6mm +/- 0.3 mm
Width	12.5mm +/- 0.3 mm
Height	1.9mm +/- 0.3 mm

8 PROCESS SPECIFICATION

Specification	Description
MSL 3	Moisture Sensitivity Level designed and manufactured according to JEDEC J-STD-020C
REACH	REACH is a European Community Regulation on chemicals and their safe use (EC 1907/2006). It deals with the Registration, Evaluation, Authorisation and Restriction of Chemical substances
RoHS	Designed in compliance with **The Restriction of Hazardous Substances Directive (RoHS)**

9 PCB MOUNTING AND SOLDERING

9.1 RECOMMENDED PCB MOUNTING PATTERN

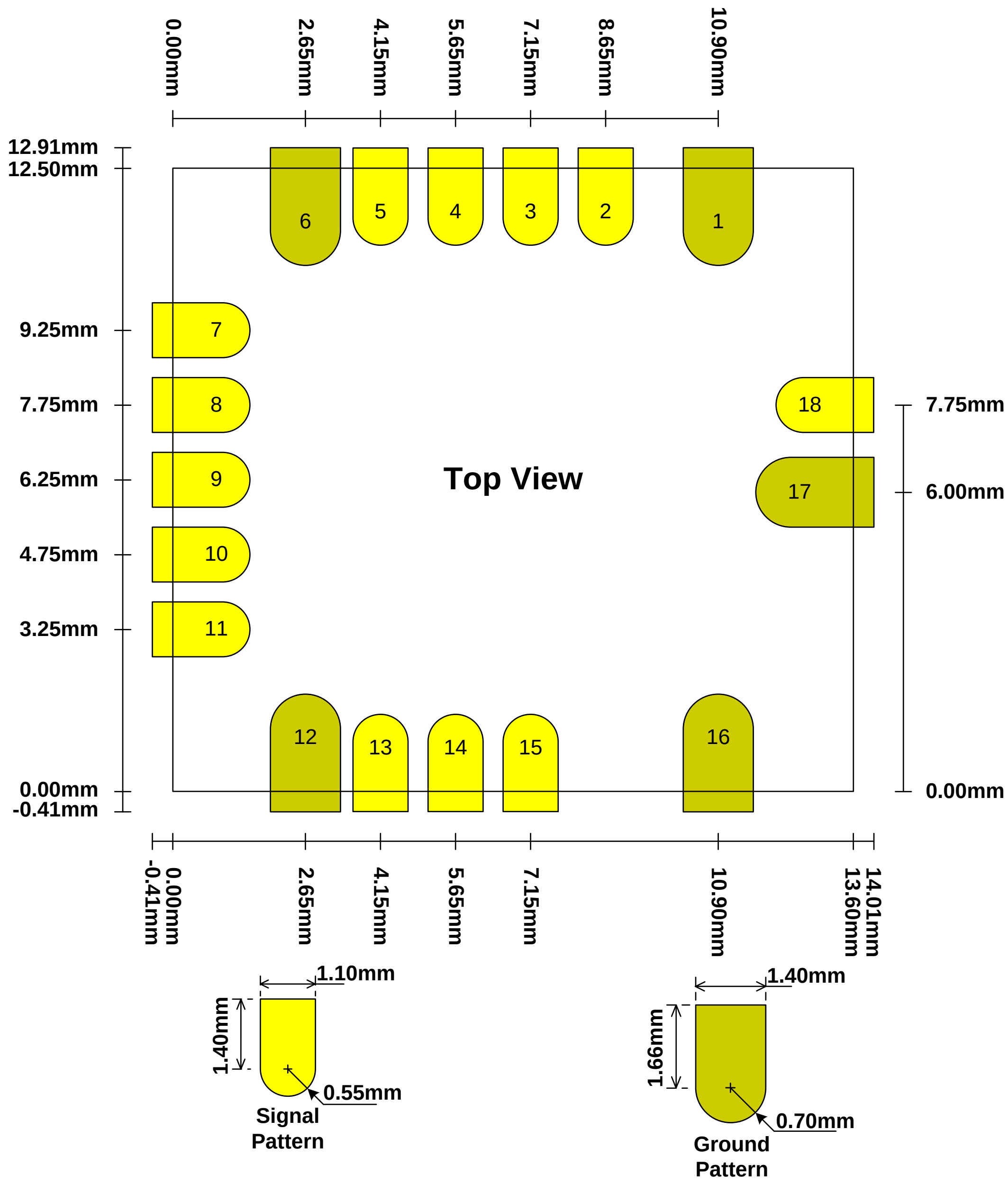


Figure 9.1: Top view of land pattern

SOLDERING INFORMATION

The soldering details to properly solder the ZM5202 module on standard PCBs are described below. The information provided is intended only as a guideline and Silicon Labs is not liable if a selected profile does not work.

See IPC/JEDEC J-STD-020D.1 for more information.

Table 9.1: Soldering details

PCB solder mask expansion from landing pad edge	0.1 mm
PCB paste mask expansion from landing pad edge	0.0 mm
PCB process	Pb-free (Lead free for RoHS [4]compliance)
PCB finish	Defined by the manufacturing facility (EMS) or customer
Stencil aperture	Defined by the manufacturing facility (EMS) or customer
Stencil thickness	Defined by the manufacturing facility (EMS) or customer
Solder paste used	Defined by the manufacturing facility (EMS) or customer
Flux cleaning process	Defined by the manufacturing facility (EMS) or customer

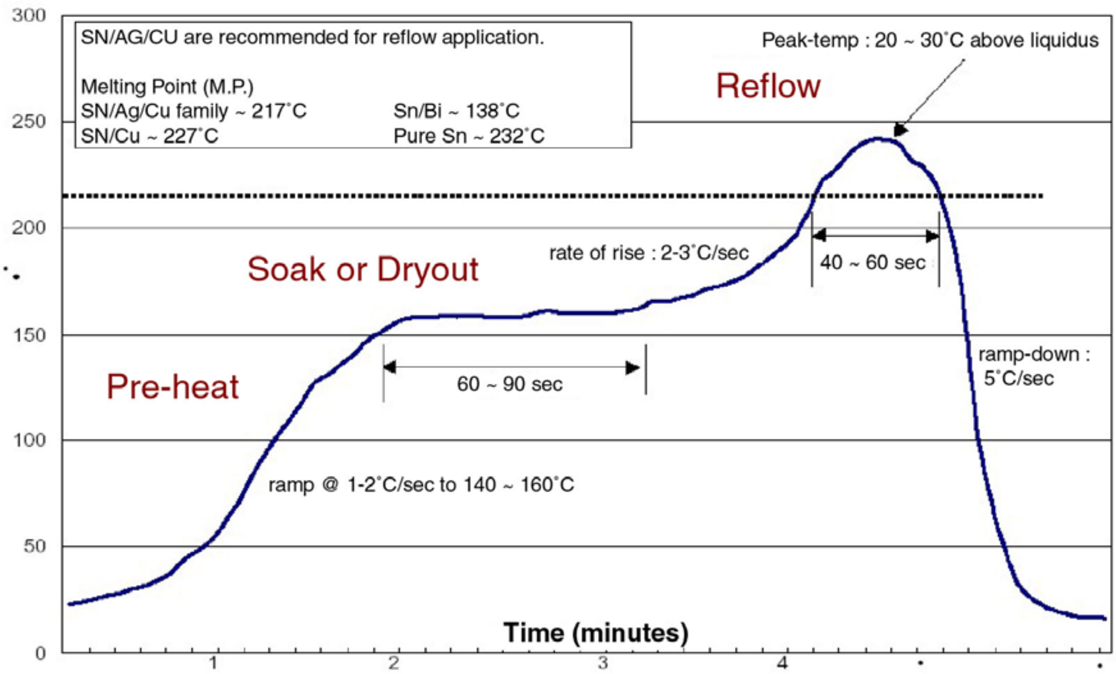


Figure 9.2: Typical reflow profile

[4] RoHS = Restriction of Hazardous Substances Directive, EU

10 ORDERING INFORMATION

Table 10.1: Ordering codes

Orderable Device	Status	Package Type	Pins	Minimum Order Quantity	Description
ZM5202AE-CME3R	ACTIVE	SOM	18	1000 pcs.	ZM5202 module, RevA, 868MHz Band, Tape and Reel
ZM5202AU-CME3R	ACTIVE	SOM	18	1000 pcs.	ZM5202 module, RevA, 908MHz Band, Tape and Reel
ZM5202AH-CME3R	ACTIVE	SOM	18	1000 pcs.	ZM5202 module, RevA, 921MHz Band, Tape and Reel

10.1 TAPE AND REEL INFORMATION

Shipment will be provided in tape with dimensions according to specifications in the following sections. Reel can be from two alternative sources A or B with following dimensions and design. Main difference between alternatives is design and visual look. Dimensions has been kept as equal as possible.

10.1.1 TAPE DIMENSIONS

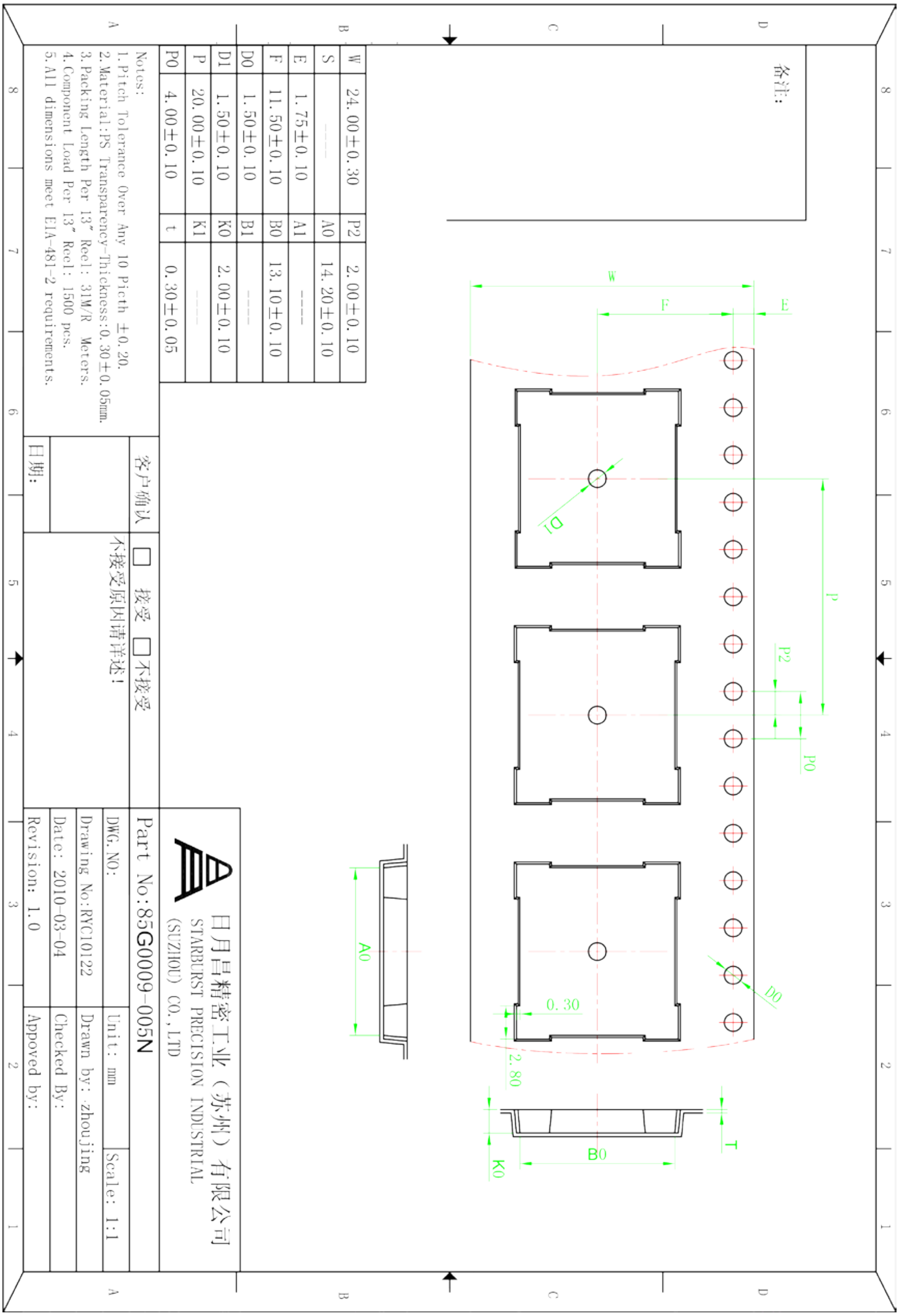
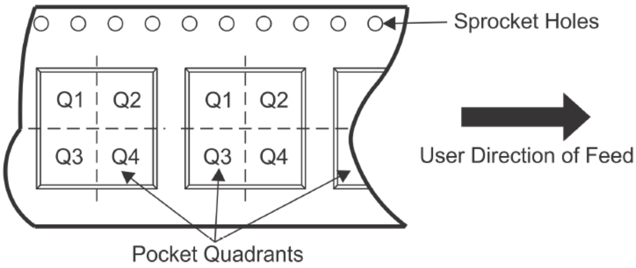


Figure 10.1: Tape information

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



Parameter	Value
Pin 1 Quadrant	Pocket Quadrant Q3

10.1.2 REEL SUPPLIER A

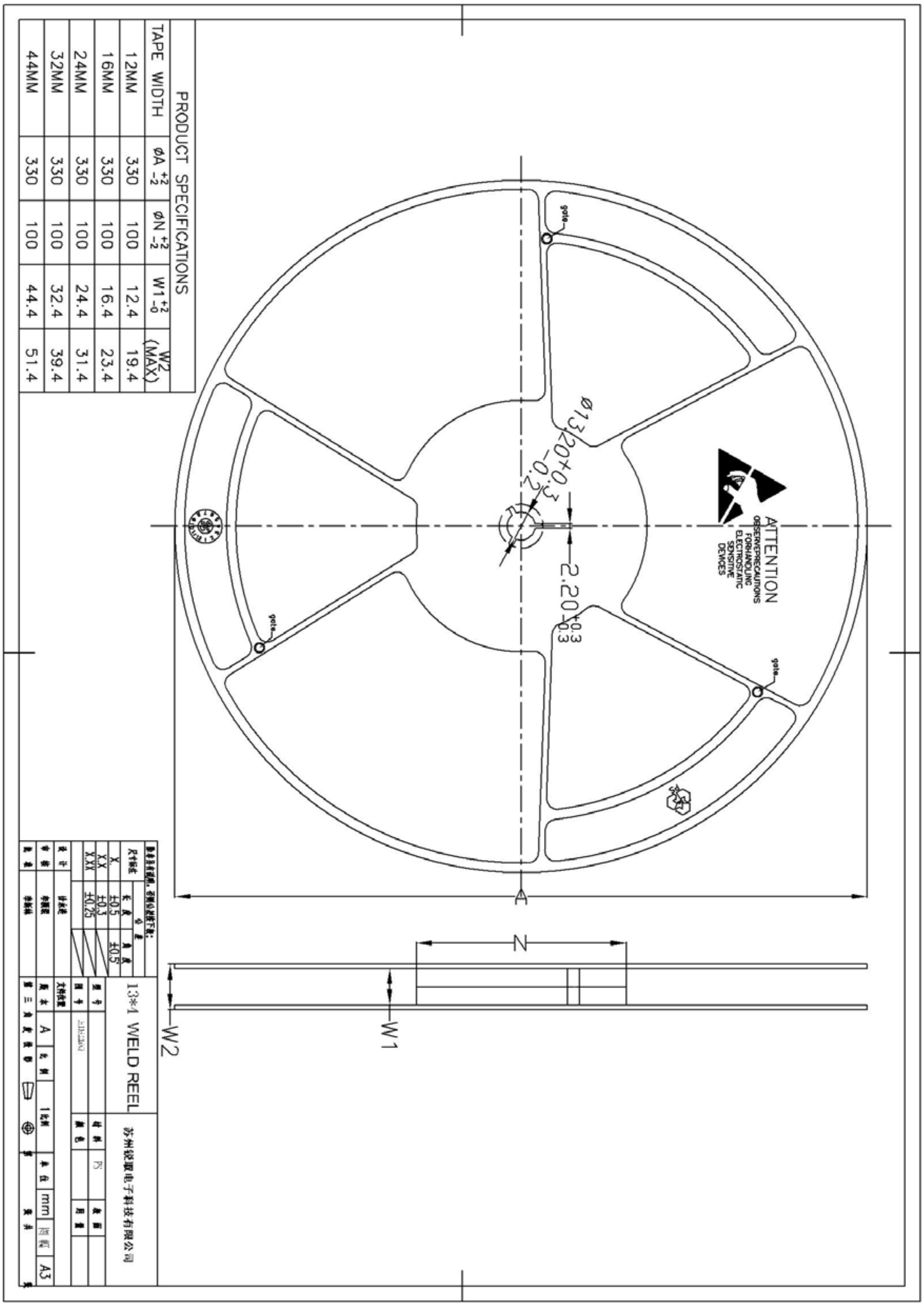
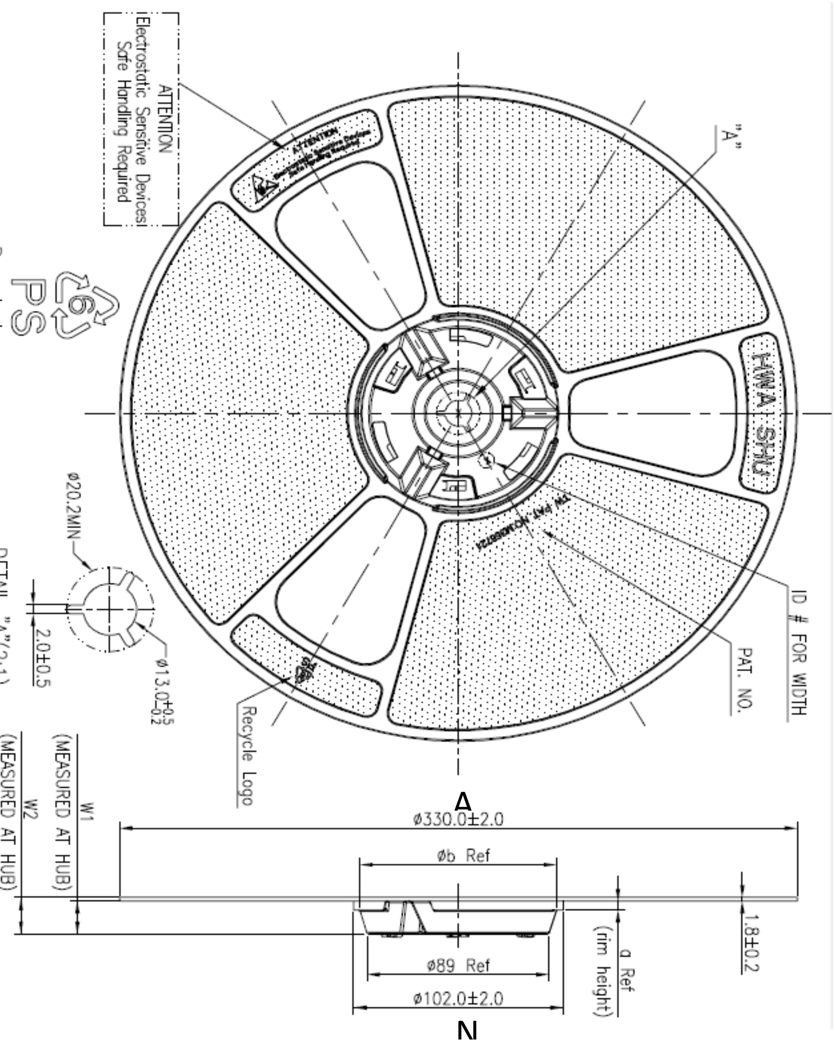
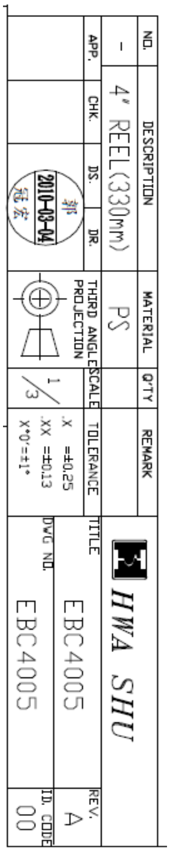


Figure 10.2: Reel information

10.1.3 REEL SUPPLIER B



Part Number	Color	Nominal	øA (+/-2 mm)	øN (+/-2 mm)	W1	W2 MAX
EBC408-210	BLUE	8 mm	330 mm	102 mm	8.5 (+0.70 mm , -0.30 mm)	11.2 mm
EBC416-210	BLUE	16 mm	330 mm	102 mm	16.5 (+0.70 mm , -0.30 mm)	19.2 mm
Combine reel	**BLUE**	**24 mm**	**330 mm**	**102 mm**	**25 (+0.70 mm , -0.30 mm)**	**30.4 mm**



11 ABBREVIATIONS

Abbreviation	Description
2FSK	2-key Frequency Shift Keying
2GFSK	2-key Gaussian Frequency Shift Keying
ACM	Abstract Control Model
ACMA	Australian Communications and Media Authority
ADC	Analog-to-Digital Converter
AES	Advanced Encryption Standard
API	Application Programming Interface
APM	Auto Programming Mode
AV	Audio Video
BOD	Brown-Out Detector
CBC	Cipher-Block Chaining
CDC	Communications Device Class
CE	Conformité Européenne
COM	Communication
CPU	Central Processing Unit
CRC	Cyclic Redundancy Check
D	Differential
D-	Differential Minus
D+	Differential Plus
DAC	Digital-to-Analog Converter
DC	Direct Current
DMA	Direct Memory Access
ECB	Electronic CodeBook
EMS	Electronic Manufacturing Services
ESD	Electro-Static Discharge
FCC	Federal Communications Commission
FER	Frame Error Rate
FET	Field Effect Transistor
FLiRS	Frequently Listening Routing Slave
FSK	Frequency Shift Keying
GFSK	Gaussian Frequency Shift Keying
GP	General Purpose
GPIO	General Purpose Input Output
I	Input
I/O	Input / Output
IC	Integrated Circuit
IF	Intermediate Frequency
IGBT	Insulated-Gate Bipolar Transistor
INT	Interrupt
IPC	Interconnecting and Packaging Circuits
IR	Infrared
IRAM	Indirectly addressable Random Access Memory
ISM	Industrial, Scientific, and Medical
ISP	In-System Programming
ITU	International Telecommunications Union
JEDEC	Joint Electron Device Engineering Council
LED	Light-Emitting Diode
lsb	Least Significant Bit
LSB	Least Significant Byte
MCU	Micro-Controller Unit
MIC	Ministry of Internal affairs and Communications, Japan

Abbreviation	Description
MISO	Master In, Slave Out
MOSI	Master Out, Slave In
msb	Most Significant Bit
MSB	Most Significant Byte
NMI	Non-Maskable Interrupt
NRZ	Non-Return-to-Zero
NVM	Non-Volatile Memory
NVR	Non-Volatile Registers
O	Output
OEM	Original Equipment Manufacturer
OFB	Output FeedBack
Pb	Lead
PCB	Printed Circuit Board
POR	Power-On Reset
PWM	Pulse Width Modulator
RAM	Random Access Memory
RF	Radio Frequency
RoHS	Restriction of Hazardous Substances
ROM	Read Only Memory
RS-232	Recommended Standard 232
RX	Receive
S	Supply
SAW	Surface Acoustic Wave
SCK	Serial Clock
SFR	Special Function Register
SiP	System-in-Package
SOM	System-On-Module
SPI	Serial Peripheral Interface
SRAM	Static Random Access Memory
T0	Timer 0
T1	Timer 1
TX	Transmit
UART	Universal Asynchronous Receiver Transmitter
USB	Universal Serial Bus
WUT	Wake-Up Timer
XRAM	External Random Access Memory
XTAL	Crystal
ZEROX	Zero Crossing

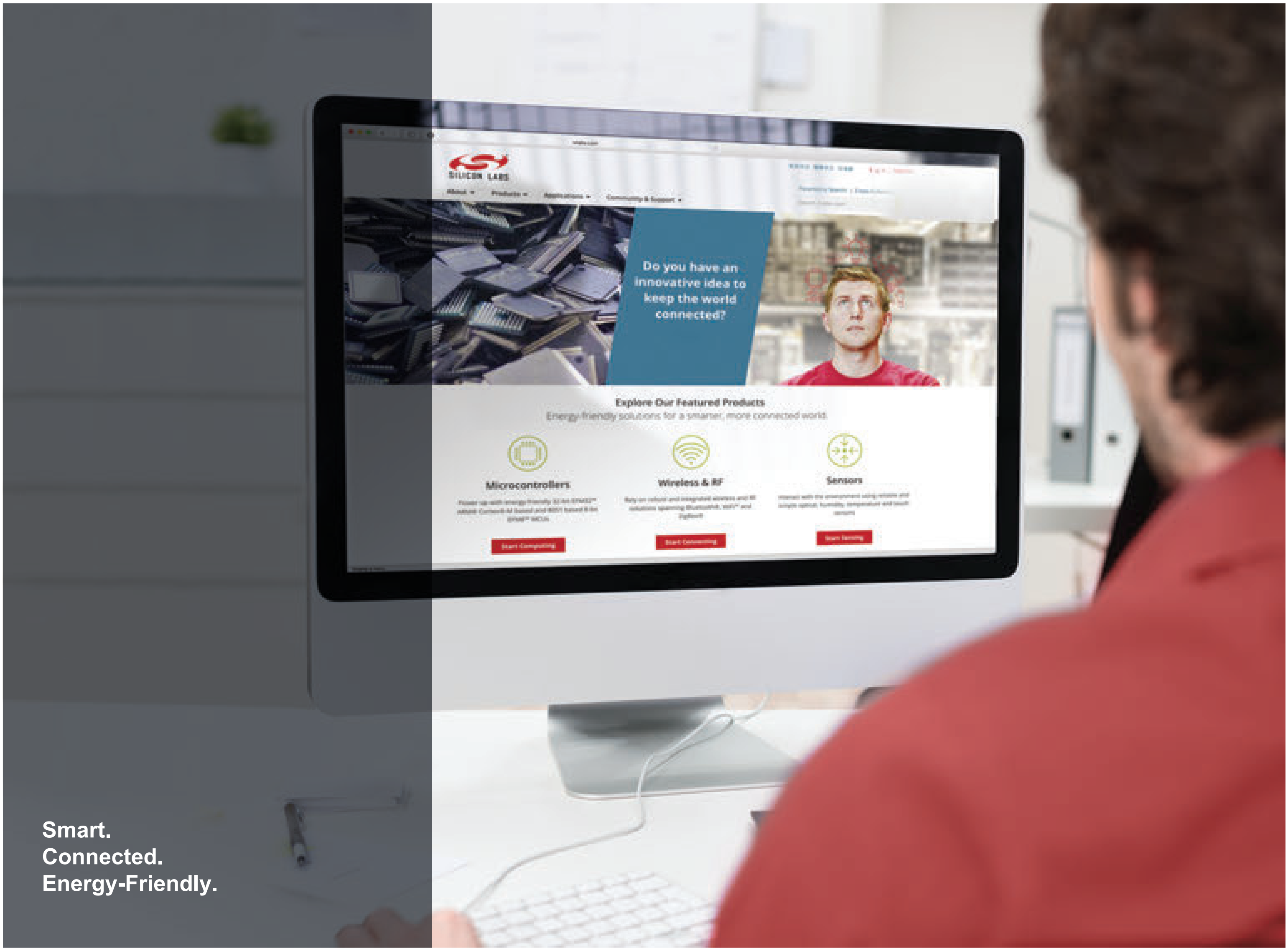
12 REVISION HISTORY

Date	Version	Affected	Revision
2018/02/19	15	§6, Table 6.1	Updated Korea frequency
2017/06/27	14	§ 5.9.1	Clarified transmitter is calibrated from factory
2017/04/11	13	Figure 4.1	Figure 4.1 updated with to scale drawing, and placement of pads, some notations changed from diameter to radius.
		Figure 9.1	Figure 9.1 updated dimensions and placement of land patterns to fit module pads.
2017/02/09	12	§ 10.1.1	Pin 1 Quadrant corrected to "Q3"
2016/12/20	11	Table 5.5	Cleaned up "TDB"
2016/11/24	10	§ 10	Add Reel information from source B
2016/10/26	9	Table 6.1	Corrected frequency accuracy to worst case figure
2016/4/29	8	$2.2.4	Updated wording in section 2.2.4 Crystal driver and system clock
2015/4/28	7	Figure 9.1	Updated to align with SD3502 recommendation.
		Table 9.2	Removed – information included in updated Figure 9.1
		§8	Added section Process Specification
		§10.1	Added orientation of component in tape
		Figure 4.1	Corrected length of Signal Pin and Ground Pin
		§7.2, Table 7.2	Added tolerances to module dimensions
2015/1/30	6B	Table 6.1	Added frequency accuracy
2013/12/13	5	Table 2.1	Entries in table of CPU modes rephrased
2013/12/12	4A	Table 2.1,	Reduced the RESET_N high time
		§2.4.1	Increased the RESET_N low time
2013/10/31	3B	§Cover,	Updated performance values
		Figure 2.1,	Added LED controller
		Table 2.3,	Updated INT1 pins
		Figure 2.7,	Updated caption
		Table 4.3,	Changed to master I/O mode
		§5.1,	Updated final test description
		Table 5.5, Figure 5.2,	Updated TX current consumption
		Table 5.20, Figure 5.3,	Updated TX power and performance
		Table 5.22,	Updated LO leakage
		§5.9.2	Updated equation for 1^{st}-order approximation
2013/10/29	3A	§Cover,	Updated performance values
		Figure 2.1,	Updated matching description
		§2.1,	Added CPU modes
		Table 2.2, Table 2.3,	Updated pin numbers
		§2.2.2,	Added source impedance formula
		§2.2.9,	Added LED controller
		Figure 2.5,	Updated SPI slave connection
		§2.2.12,	Added Timers
		§4.1,	Removed 'weak' from pull-up description
		Table 4.3,	Updated pin names
		Table 4.8,	Added LED interface pin
		Table 4.10,	Added Timer interface pins
		Table 5.1,	Added maximum RF input
		Table 5.5,	Updated current consumption values
		Figure 5.2,	Updated transmit current consumption
		Table 5.12,	Updated programming time
		Table 5.16, Table 5.18,	Added pull-up resistor value
		Table 5.20, Figure 5.3,	Updated TX power and harmonics
		§5.9.1,	Added mandatory TX calibration

Date	Version	Affected	Revision
		Table 5.21, Figure 5.4,	Updated sensitivity values
		Table 5.22,	Updated blocking and LO leakage
		Figure 5.5,	Updated RSSI values
		Figure 7.1	Updated module marking
2013/09/12	2A	§Cover,	Updated the features and module items
		§2.2.5,	Added GPIO description
		§2.2.10, §2.2.11,	Added peripheral designators
		Figure 4.1,	Added pin dimensions
		§5.9,	Removed impedance plots
		Table 5.15, Table 5.18,	Changed the supply voltage range and clock speed of external
		§6,	NVM
		Table 7.2	Corrected Korean frequency
			Added module dimensions
2013/06/03	1G	Table 2.3,	Removed empty line from interrupt table
		Table 5.8	Added state transition times
2013/05/31	1E	§All	Updated IO characteristics
2013/05/20	1C	§All	Updated layout, and data from the latest corner tests
2013/02/22	1A	§All	Preliminary draft released
2013/02/18	1A	§All	Initial draft

13 REFERENCES

[1] INS11681, Instruction, “500 Series Z-Wave Chip Programming Mode”
[2] DSH12436, Datasheet, “ZDB5202 Z-Wave Development Board”
[3] INS12213, Instruction, “500 Series Hardware Integration Guide”
[4] DSH11243, Datasheet, “ZDP03A, Z-Wave Development Platform”



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