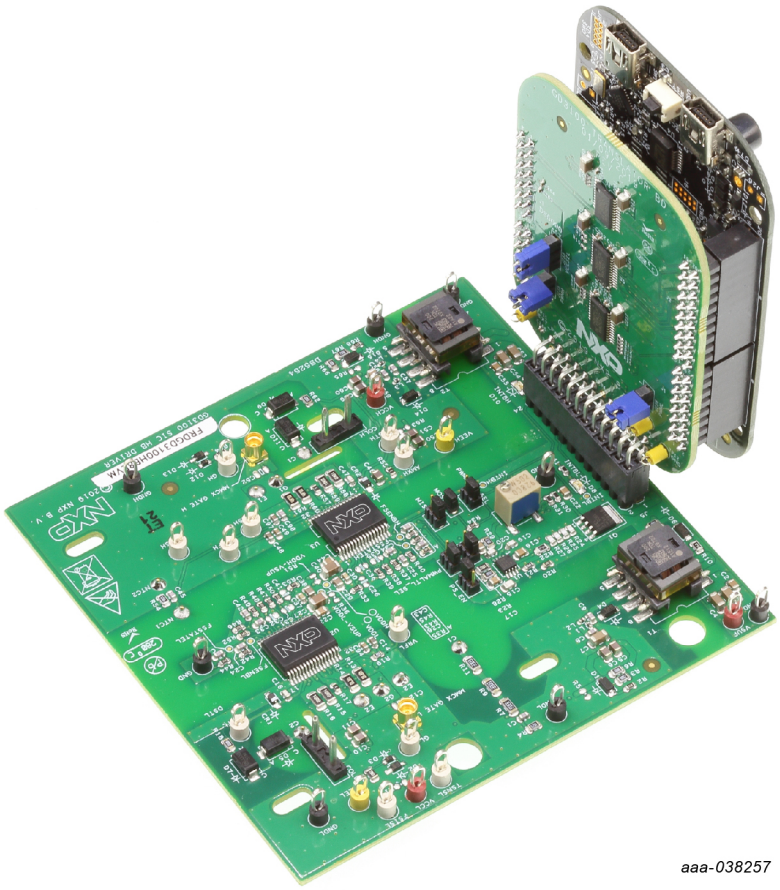
UM11440

FRDMGD3100HB8EVM half-bridge evaluation board

Rev. 1 — 4 August 2020 User guide

1 FRDMGD3100HB8EVM



aaa-038257

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2 Getting started

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The tool summary page for the FRDMGD3100HB8EVM evaluation board is at http://www.nxp.com/FRDMGD3100HB8EVM. The tool summary page provides information related to using the evaluation board. The page contains the following sections:

- Overview – A brief summary of the evaluation board and its capabilities
- Supported Devices – A list of devices that the evaluation board supports
- Specifications – An overview of the technical and functional specifications for the board
- Documents and Software/Design Resources – All of the information and resources required by users who have already purchased the FRDMGD3100HB8EVM. This section includes:
  - Design Tools & Files – Click on the Download button to download the board Bill of Materials and the Gerber files for the PCB assemblies.
  - Printed Circuit Boards and Schematics – Click on the Download button to download a .pdf version of the FRDMGD3100HB8EVM board schematics.

The Get Started link in the upper left of the menu bar provides information applicable to using the FRDMGD3100HB8EVM.

2.1 Kit contents/packing list

The FRDMGD3100HB8EVM kit contents include:

- Complete assembly of FRDMGD3100HB8EVM evaluation board
- 3.3 V to 5.0 V GD3100 translator board connected to FRDM-KL25Z
- USB cable, type A male/type mini B male, 3 ft
- 1.27 mm jumpers for configuration (included with kit boards)
- Quick start guide

2.2 Required equipment

The kit requires the following equipment:

- Compatible SiC module
- DC link capacitor compatible with the SiC module
- 30 µH to 50 µH, high current air core inductor for double pulse testing
- HV power supply with protection shield and hearing protection
- 25 V, 1.0 A DC power supply
- 500 MHz 2.5 GS/s 4-channel oscilloscope
- Rogowski coil, PEM Model CWT Mini HF60R, or CTW MiniHF30 (smaller diameter)
- Isolated high-voltage probe (CAL Test Electric CT2593-1, LeCroy AP030)
- Digital voltmeter

2.3 System requirements

The kit requires the following to function properly with the software:

- Windows 7 or higher operating system

3 Getting to know the hardware

3.1 Overview

The FRDMGD3100HB8EVM is a half-bridge evaluation kit populated with two MC33GD3100 single channel gate drive devices. The kit includes the Freedom KL25Z microcontroller hardware for interfacing a PC installed with SPIGen software for communication to the serial peripheral interface (SPI) registers on the GD3100 gate drive devices in either daisy chain or standalone configuration.

The GD3100 translator board is used to translate 3.3 V signals to 5.0 V signals between the MCU and the MC33GD3100 gate drivers. The evaluation kit can be connected to a compatible insulated gate bipolar transistor (IGBT) or SiC module for half-bridge evaluations and applications development.

3.2 Board features

- Capability to connect to P6 SiC module for half-bridge evaluations
- Negative VEE gate low drive level (−3.9 V DC)
- VCCREG regulated high gate drive level (+15 V DC)
- Jumper configurable for disabling dead time fault protection when short-circuit testing
- Easy access power, ground, and signal test points
- Easy to install and use SPIGen GUI for interfacing via SPI through PC; software includes double pulse and short-circuit testing capability
- DC link bus voltage monitor on low-side driver via AMUXIN and AOUT
- Negative temperature coefficient (NTC) connection and configurable for monitoring module temperature

3.3 Device features

Table 1. Device features

Device	Description	Features
MC33GD3100	The MC33GD3100 is an advanced single channel gate driver for IGBTs.	• Compatible with current sense and temp sense IGBTs • DESAT detection capability for detecting V_{CE} desaturation condition • Fast short-circuit protection for IGBTs with current sense feedback • Compliant with automotive safety integrity level (ASIL) C/D ISO 26262 functional safety requirements • SPI interface for safety monitoring, programmability, and flexibility • Integrated galvanic signal isolation • Integrated gate drive power stage capable of 10 A peak source and sink • Interrupt pin for fast response to faults • Compatible with negative gate supply • Compatible with 200 V to 1700 V IGBTs, power range > 125 kW

3.4 Board description

The FRDMGD3100HB8EVM is a half-bridge evaluation board populated with two MC33GD3100 single channel IGBT or SiC gate drive devices. The board supports connection to an FRDM-KL25Z microcontroller for SPI communication configuration programming and monitoring. The board includes DESAT circuitry for short-circuit detection and implementation of MC33GD3100 shutdown protection capabilities.

The evaluation board is designed to connect to a P6 SiC metal-oxide-semiconductor field-effect transistor (MOSFET) for evaluation of the MC33GD3100 performance and capabilities.

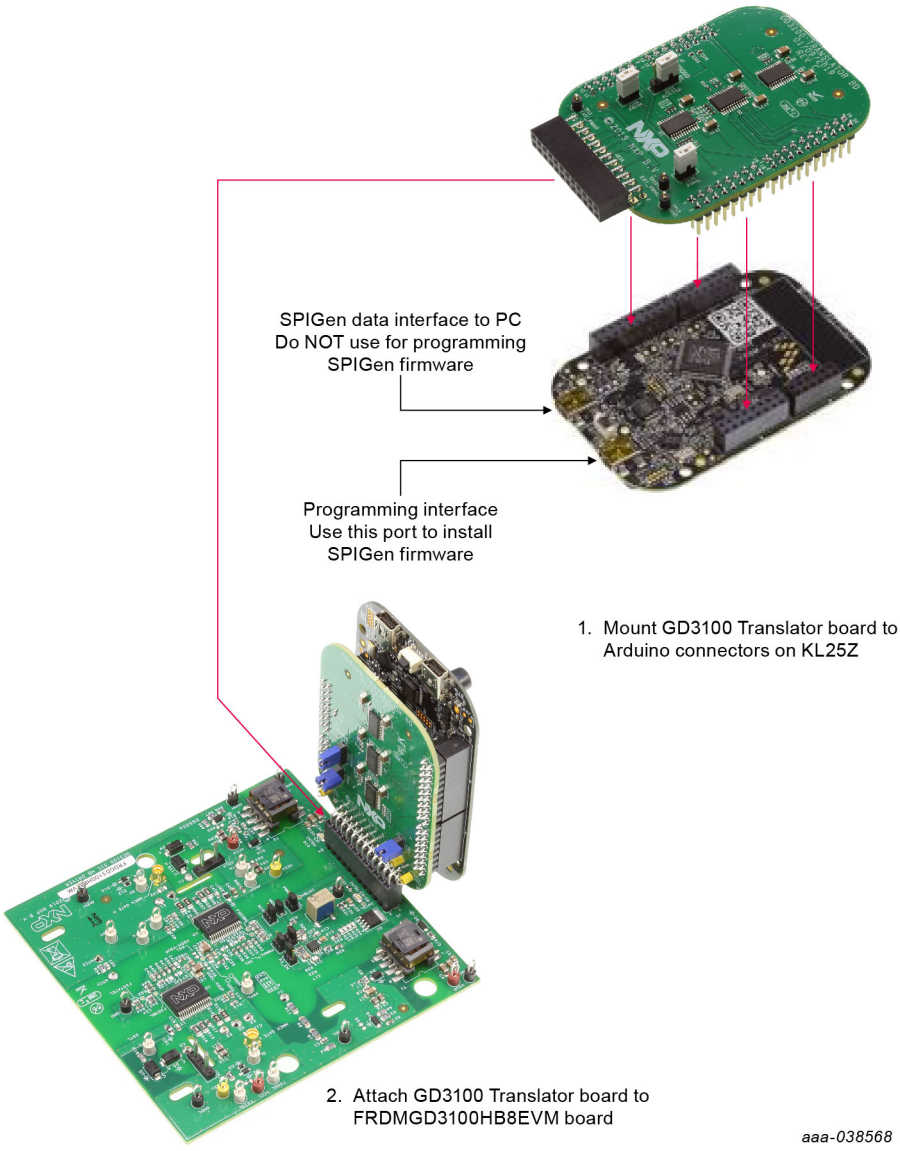

Figure 1. Connecting FRDM-KL25Z, FRDMGD3100HB8EVM and GD3100 translator board

3.4.1 Low-voltage logic and control connector

The low-voltage domain is 12 V VSUP domain that interfaces with the MCU and MC33GD3100 control registers through the 24-pin connector interface.

The low-side driver and high-side driver domains are driver control interfaces to SiC module single phase connections and test points.

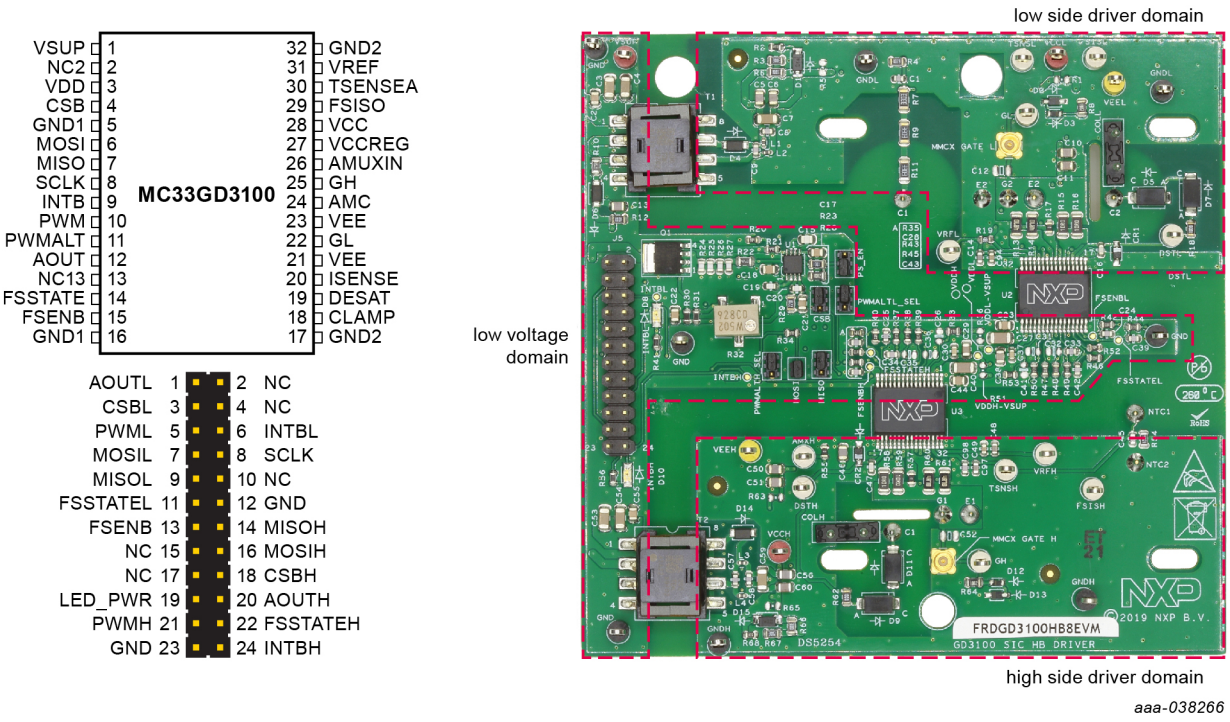

Figure 2. FRDMGD3100HB8EVM board voltage and interface domains

Table 2. Low-voltage domain 24-pin connector definitions

Pin	Name	Function
1	AOUTL	analog output duty cycle encoded signal (low side) for reading temperature via TSENSEA or voltage via AMUXIN
2	n.c.	not connected
3	CSBL	chip select bar (low side)
4	n.c.	not connected
5	PWML	pulse width modulation (PWM) input (low side)
6	INTBL	interrupt bar (low side)
7	MOSIL	master out slave in (low side)
8	SCLK	serial clock input
9	MISOL	master in slave out (low side)
10	n.c.	not connected
11	FSSTATEL	fail-safe state (low side)
12	GND	ground
13	FSENB	fail-safe enable (high side and low side)
14	MISOH	master in slave out (high side)
15	n.c.	not connected
16	MOSIH	master out slave in (high side)
17	n.c.	not connected

Pin	Name	Function
18	CSBH	chip select bar (high side)
19	LED_PWR	USB 3.3 V power for INTB LEDs (high side and low side)
20	AOUTH	duty cycle encoded signal (high side)
21	PWMH	PWM input (high side)
22	FSSTATEH	fail-safe state (high side)
23	GND	ground
24	INTBH	interrupt bar (high side)

3.4.2 Test point definitions

All test points are clearly marked on the evaluation board. Figure 3 shows the location of various test points.

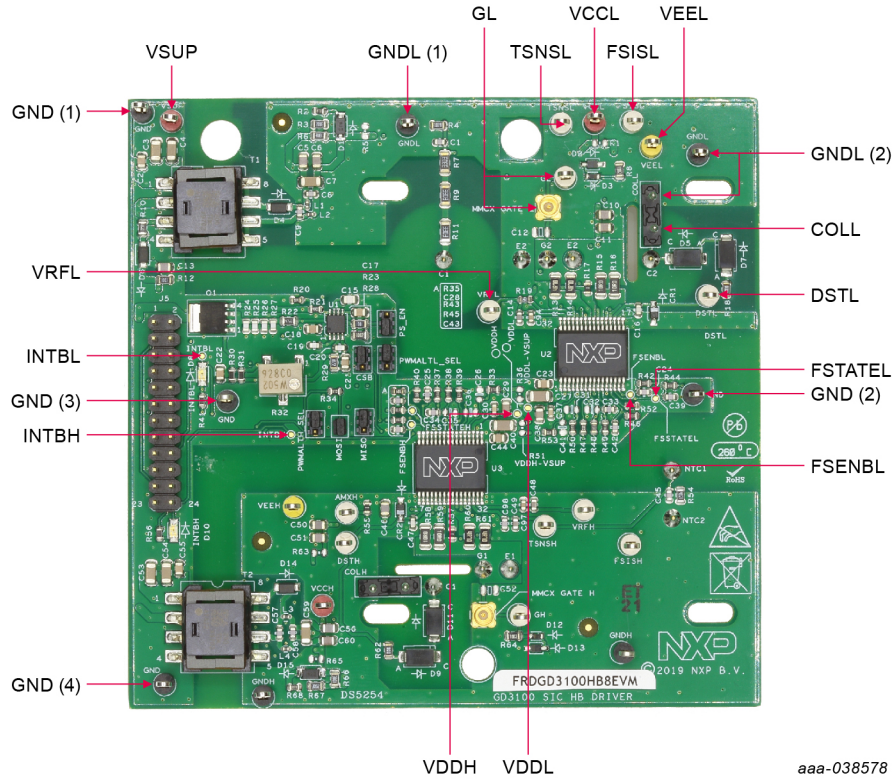

Figure 3. Key test point locations - Low voltage/low-side driver domains

Table 3. Test point definitions–low voltage/low-side driver domains

Name	Test Point	Definition
Low-voltage domain		
GND (1)	TP2	Grounding points for low-voltage domain
INTBH	TP20	Test point for interrupt bar high-side
INTBL	TP11	Test point for interrupt bar low-side
VSUP	TP26	DC voltage source connection point for VSUP power input of GD3100 devices. Typically supplied by vehicle battery +12 V DC.
Low-side driver domain		
COLL	J90	Collector test point/connection low-side
DSTL	TP10	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
FSENBL	TP12	Test point connection to low-side driver fail-safe enable pin (FSENB)
FSISL	TP6	Test point connection to low-side driver tri-state gate drive pin (FSISO)
FSTATEL	TP17	Test point connection to low-side driver fail-state state pin (FSSTATE)
GL	TP5	Module gate test point on low-side driver domain which is the charging pin of gate; including MMCX probe connection
GND (2)	TP13	Grounding point for low-side driver domain
GND (3)	TP16	Grounding point for low-side driver domain
GND (4)	TP27	Grounding point for low-side driver domain
GNDL (1)	TP3	Grounding point for isolated low-side driver grounding plane
GNDL (2)	TP7	Grounding point for isolated low-side driver grounding plane
TSNSL	TP8	Test point connection to low-side gate drive TSENSE pin
VCCL	TP1	Positive voltage supply test point for isolated circuitry and low-side driver domain
VDDH	TP18	Test point for internal power from MC33GD3100A1 (U3) VDD pin
VDDL	TP14	Test point for internal power from MC33GD3100A1 (U2) VDD pin
VEEL	TP4	Negative voltage supply test point for low-side driver gate of IGBT or SiC module
VRFL	TP9	5.0 V reference test point for isolated analog circuitry on low-side driver

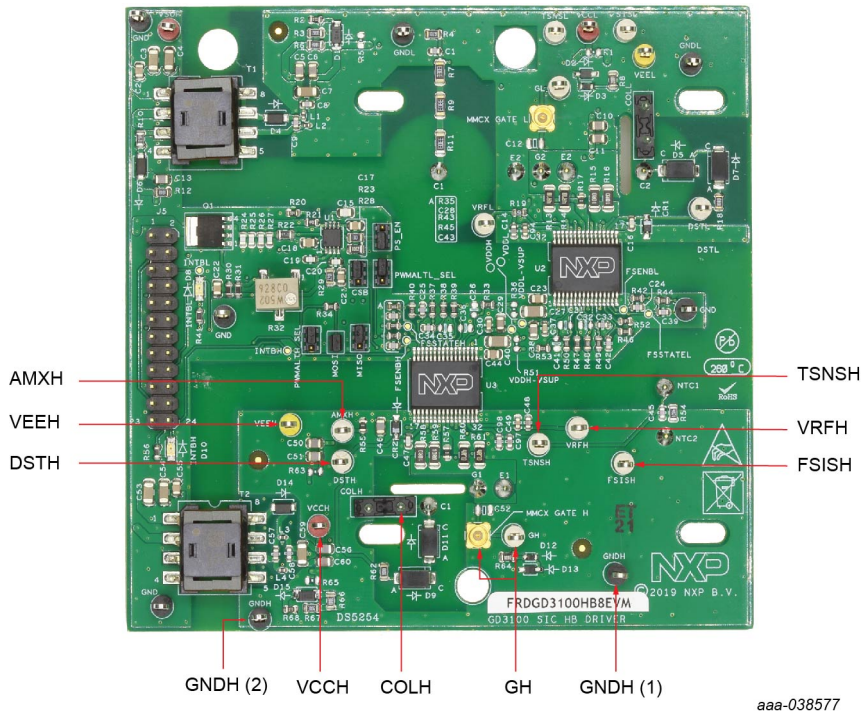

Figure 4. Test point definitions - high-side driver domain

Table 4. Test point definition - high-side driver

Name	Test point	Definition
AMXH	TP23	High-side driver test point for analog MUX input
COLH	J101	Collector test point/connection high-side
DSTH	TP25	V_{CE} desaturation test point connected to high-side driver DESAT pin and circuitry
FSISH	TP24	Test point connection to high-side driver tri-state gate drive pin (FSISO)
GH	TP28	Module gate test point on high-side driver domain which is the charging pin of gate; including MMCX probe connection
GNDH (1)	TP31	Grounding point for isolated high-side driver grounding plane
GNDH (2)	TP32	Grounding point for isolated high-side driver grounding plane
TSNSH	TP21	Test point connection to high-side gate drive TSENSE pin
VCCH	TP29	Positive voltage supply test point for isolated circuitry and high-side driver domain
VEEH	TP30	Negative voltage supply test point for high-side driver gate of IGBT or SiC module
VRFH	TP22	5.0 V reference test point for isolated analog circuitry on high-side driver

3.4.3 Power supply and jumper configuration

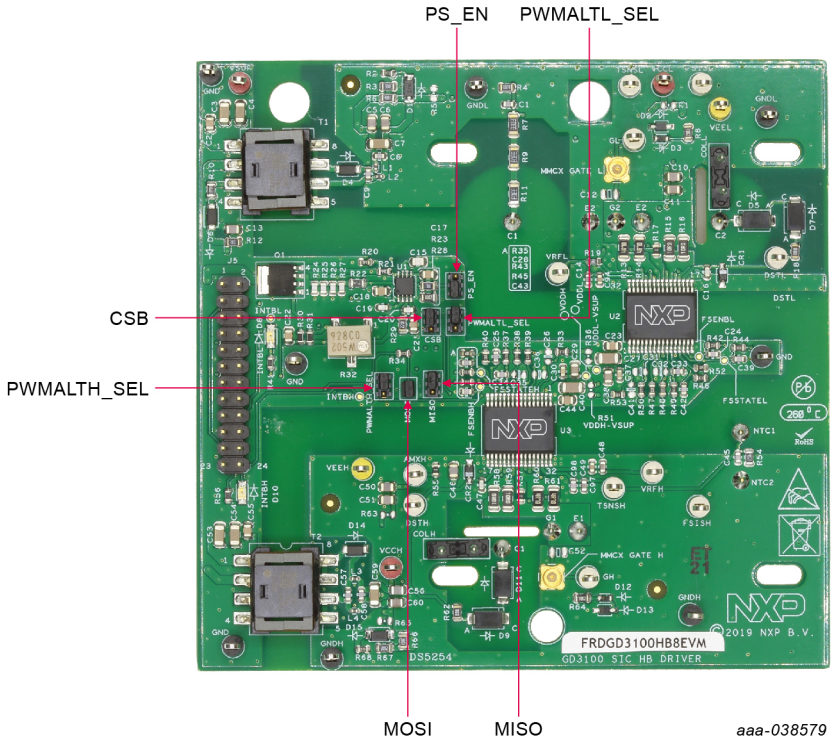

Figure 5. Power supply and jumper configuration

Table 5. Jumper definitions

Jumper	Position	Function
PWMALTL_SEL (J4)	1-2	Dead time fault protection enabled (high side)
	2-3	Dead time fault protection disabled (use for short-circuit testing)
PS_EN (J2)	1–2	Flyback power supply enable controlled from MCU
	2–3	Flyback power supply enable always on
CSB (J3)	1–2	Normal operation
	2–3	Daisy chain operation
PWMALTH_SEL (J7)	1-2	Dead time fault protection enabled (low side)
	2-3	Dead time fault protection disabled (use for short-circuit testing)
MOSI (J8)	Open	Daisy chain operation
	Close	Normal operation
MISO (J6)	1-2	Normal operation
	2-3	Daisy chain operation

Table 6. Power Supply Definition

Component	Definition
Flyback MOSFET (Q1)	AEC Q101-compliant logic level N-channel MOSFET
Potentiometer (R32)	Adjusts resistor R3 for VCCH/VCCL and VEEH/VEEL Tune VCC-GNDISO FOR +17V

3.4.4 Bottom view

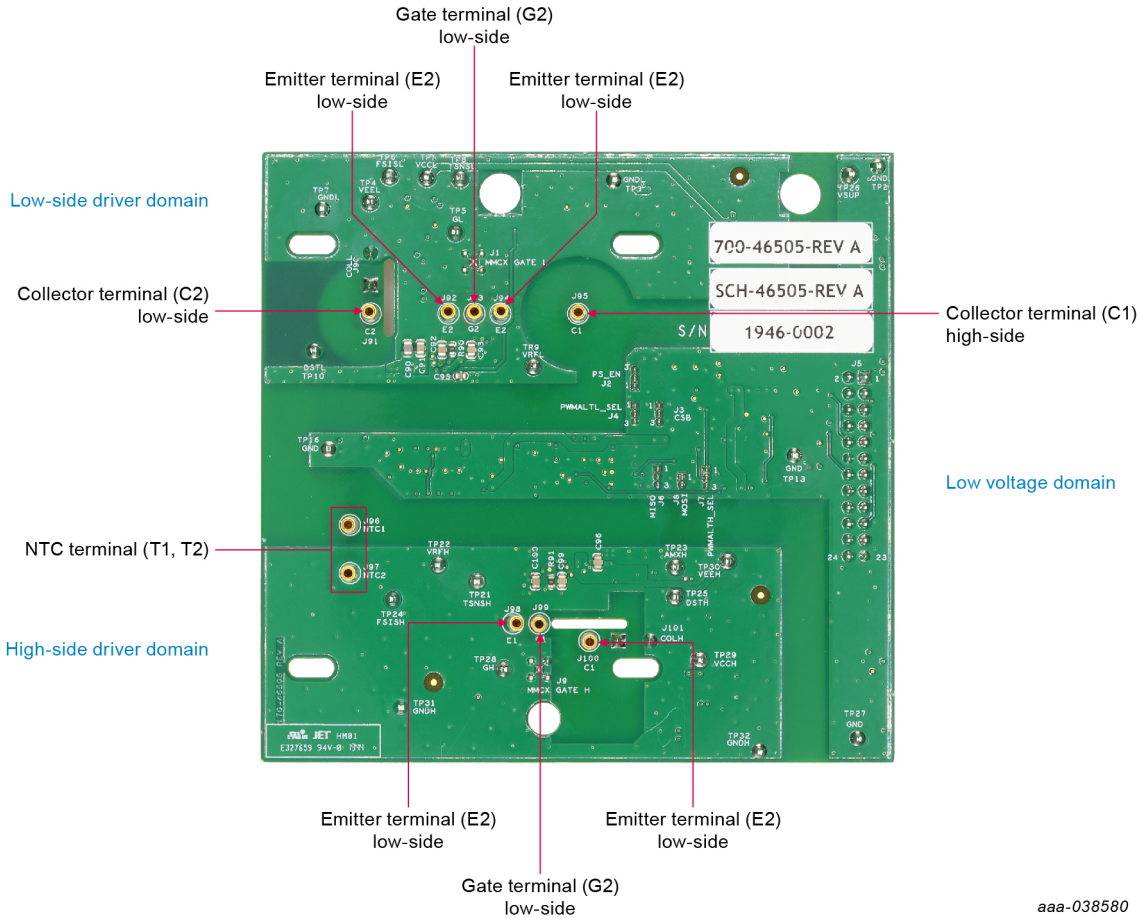

Figure 6. FRDMGD3100HB8EVM bottom view

3.4.5 Gate drive resistors

- RGH - gate high resistor in series with the GH pin at the output of the MC33GD3100 gate high driver and P6 SiC module gate that controls the turn-on current for SiC MOSFET gate.
- RGL - gate low resistor in series with the GL pin at the output of the MC33GD3100 gate low driver and P6 SiC module gate that controls the turn-off current for SiC MOSFET gate.
- RAMC - series resistor between P6 SiC module gate and AMC input pin of the MC33GD3100 driver for gate sensing and active Miller clamping.

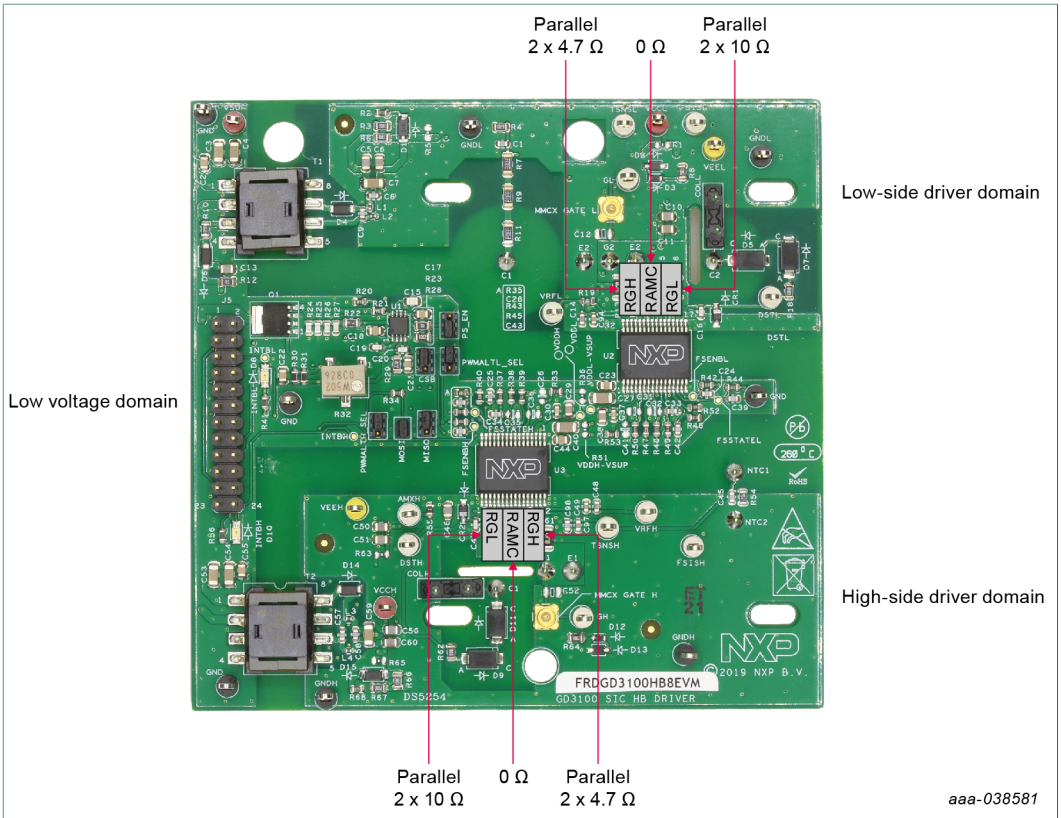

Figure 7. Gate drive resistors

3.4.6 LED interrupt indicators

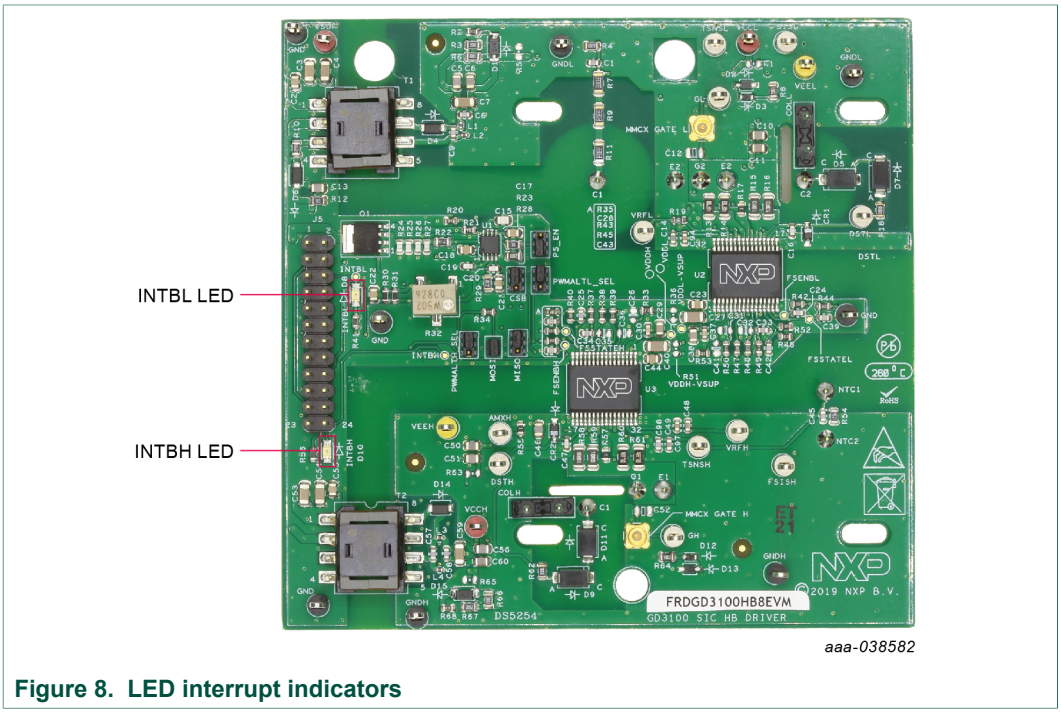

Figure 8. LED interrupt indicators

Table 7. LED interrupt indicators

LED	Description
Low-side INTB	connected to the INTB output pin of low-side driver indicating reported fault status when on (active LOW)
High-side INTB	connected to the INTB interrupt output pin of high-side driver indicating reported fault status when on (active LOW)

3.5 Kinetis KL25Z Freedom board

The Freedom KL25Z is an ultra low-cost development platform for Kinetis L series MCU built on Arm Cortex-M0+ processor.

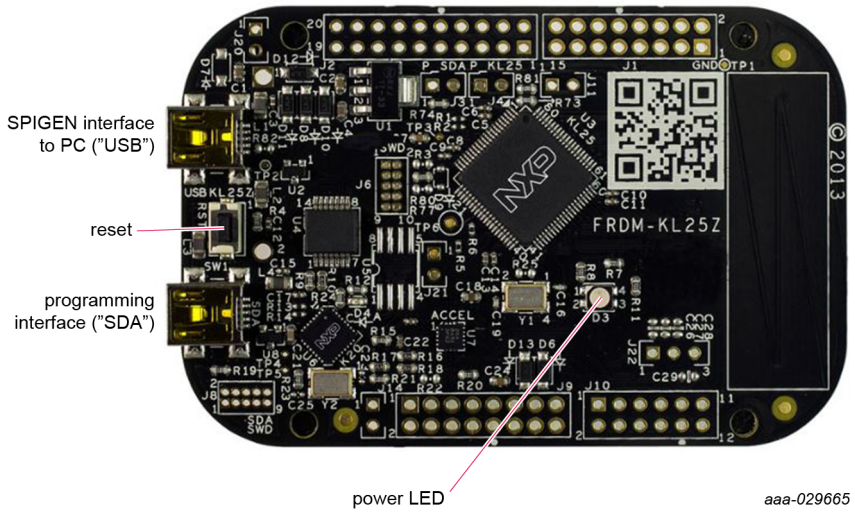

Figure 9. Freedom development platform

3.6 3.3 V to 5.0 V translator board

KITGD3100TREVB translator enables level shifting of signals from MCU 3.3 V to 5.0 V SPI communication.

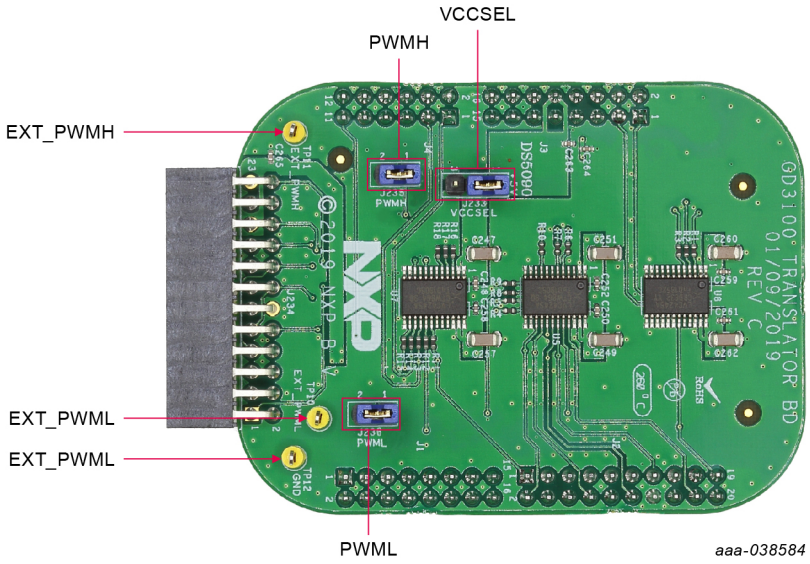

Figure 10. Translator board

Table 8. Translator board jumper definitions

Jumper/Test Point	Position	Function
Jumper		
PWMH_SEL (J235)	1-2	Selects PWM high-side control from KL25Z MCU
	Open	External PWM high-side control
PWML_SEL (J236)	1-2	Selects PWM low-side control from KL25Z MCU
	Open	External PWM low-side control
VCCSEL (J233)	1-2	Selects 5.0 V for 5.0 V compatible gate drive
	2-3	Selects 3.3 V for 3.3 V compatible gate drive
Test points		
EXT_PWMH (TP11)	—	Test point connection for terminal PWM control
EXT_PWML (TP10)	—	Test point connection for terminal PWM control
GND (TP12)	—	Grounding point

4 Configuring the hardware

FRDMGD3100HB8EVM is connected to a GD3100 translator board and a FRDM-KL25Z board as shown in Figure 11. Double pulse and short-circuit testing can be conducted using a Windows based PC with SPIGen software.

Suggested equipment needed for test:

- Rogowski coil high-current probe
- High-voltage differential voltage probe
- High sample rate digital oscilloscope with probes
- DC link capacitor
- SiC MOSFET P6 module
- Windows based PC
- High-voltage DC power supply for DC link voltage
- Low-voltage DC power supply for VSUP
  - +12 V DC gate drive board low-voltage domain
- Voltmeter for monitoring high-voltage DC link supply
- Load coil for double pulse and short-circuit testing

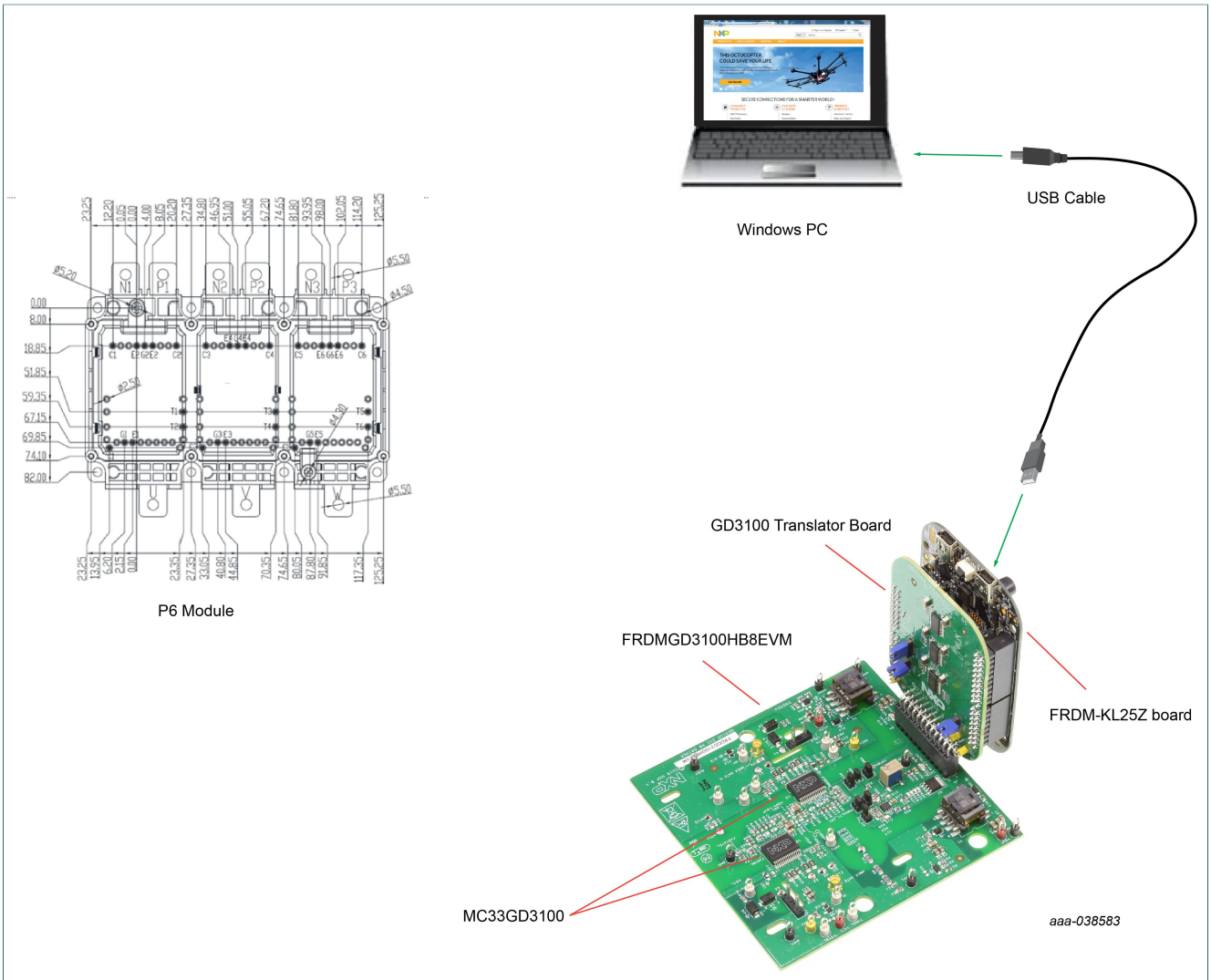

Figure 11. Evaluation board and system setup

5 Installation and use of software tools

Software for FRDMGD3100HB8EVM is distributed with the SPIGen GUI tool (available on NXP.com). Necessary firmware comes pre-installed on the FRDM-KL25Z with the kit.

Even if the user intends to test with other software or PWM, it is recommended to install this software as a backup or to help debugging.

5.1 Installing SPIGen on your computer

The latest version of SPIGen supports the MC33GD3100 and is designed to run on any Windows 10, Windows 8, or Windows 7 based operating system. To install the software, do the following:

1. Go to www.nxp.com/SPIGen and click **Download**.
2. When the SPI generator (SPIGen) software page appears, click **Download** and select the version associated with your PC operating system.
3. If instructed for the SPIGen wizard to create a shortcut, an SPIGen icon appears on the desktop. By default, the SPIGen executable file is installed at **C:\Program Files (x86)\SPIGen**.
   Installing the device drivers overwrites any previous SPIGen installation and replaces it with a current version containing the MC33GD3100 drivers. However, configuration files (.spi) from the previous version remain intact.

5.2 Configuring the FRDM-KL25Z microcode

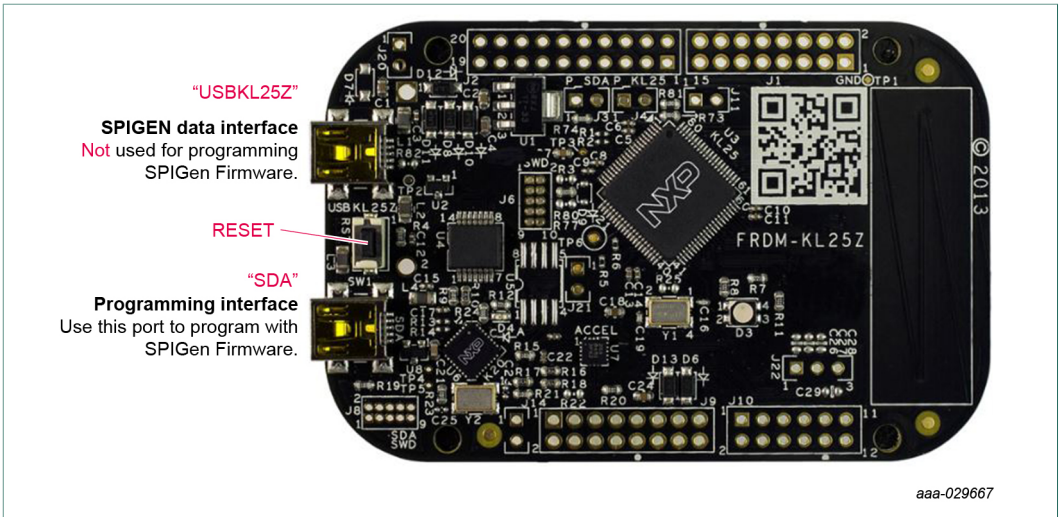

Figure 12. FRDM-KL25Z setup and interface

By default, the FRDM-KL25Z delivered with this kit is preprogrammed with the current and most up-to-date firmware available for the kit.

A way to check quickly that the microcode is programmed and the board is functioning properly, is to plug the KL25Z into the computer, open SPIGen, and verify that the software version at the bottom is 5.4.7 (see Figure 13).

If a loss of functionality following a board reset, reprogramming, or a corrupted data issue, the microcode may be rewritten per the following steps:

1. To clear the memory and place the board in boot loader mode, hold down the reset button while plugging a USB cable into the **OpenSDA** USB port.
2. Verify that the board appears as a BOOTLOADER device and continue with step 3. If the board appears as KL25Z, you may go to step 6.
3. Download the **Firmware Apps** .zip archive from the PEmicro OpenSDA webpage (http://www.pemicro.com/opensda/). Validate your email address to access the files.
4. Find the most recent MDS-DEBUG-FRDM-KL25Z_Pemicro_v***.SDA and copy/drag-and-drop into the **BOOTLOADER** device.
5. Reboot the board by unplugging and replugging the connection to the **OpenSDA** port. Verify now that the device appears as a KL25Z device to continue.
6. Locate the most recent KL25Z firmware; which is distributed as part of the SPIGen package.
   a. From the SPIGen install directory, which is located in the **SPI Dongle Firmware** folder and is named in the form “UsbSPIDongleKL25Z_GD3100_v***.srec”.
   b. This .srec file is a product/family-specific configuration file for FRDM-KL25Z containing the pin definitions, SPI/PWM generation code, and pin mapping assignments necessary to interface with the translator board as part of FRDMGD31RPEVM.
7. With the KL25Z still plugged through the **OpenSDA** port, copy/drag-and-drop the .srec file into the KL25Z device memory. Once done, disconnect the USB and plug into the other USB port, labeled **KL25Z**.
   a. The device may not appear as a distinct device to the computer while connected through the KL25Z USB port, this is normal.
8. The FRDM-KL25Z board is now fully set up to work with FRDMGD31RPEVM and the SPIGen GUI.
   a. There is no software stored or present on either the driver or translator boards, only on the FRDM-KL25Z MCU board.

All uploaded firmware is stored in non-volatile memory until the reset button is hit on the FRDM-KL25Z. There is no need to repeat this process upon every power up, and there is no loss of data associated with a single unplug event.

5.3 Using the SPIGen graphical user interface

The SPIGen graphical user interface is available from http://www.nxp.com/SPIGen as an evaluation tool demonstrating MC33GD3100-specific functionality, configuration, and fault reporting. SPIGen also includes basic capacity for the FRDMGD31RPEVM to control an IGBT or SiC module, enabling double pulse or short-circuit testing.

SPI messages can be realized graphically or in hexadecimal format. CSB is selectable to address one or both MC33GD3100 on the board. See Figure 13 for SPIGen graphical user interface for MC33GD3100 internal register read and write access.

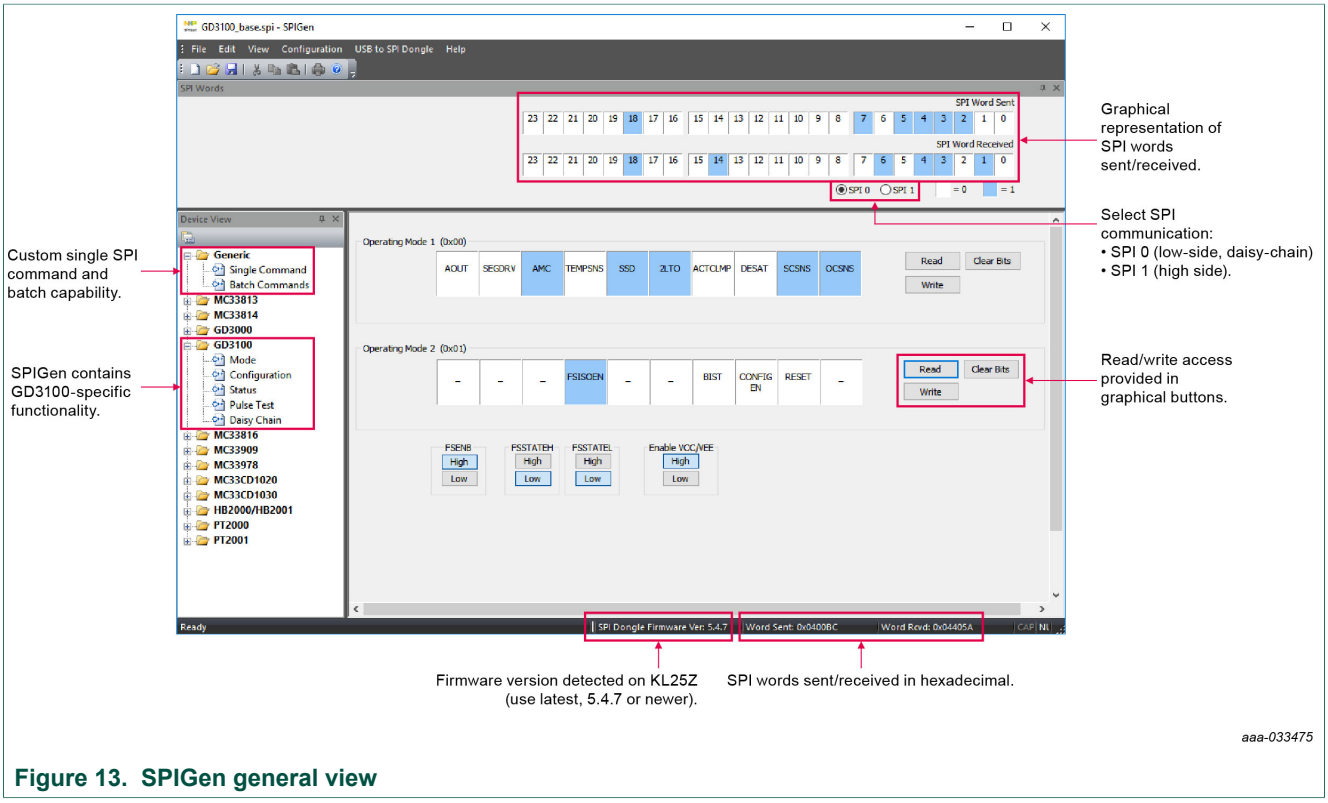

Figure 13. SPIGen general view

Some general guidelines on SPIGen usage:

- When attempting to change operating modes, configuration registers, or status mask bits, ensure the CONFIG_EN bit in the MODE2 register is set to logic 1. Fault status bits can be cleared without CONFIG_EN being set to logic 1.
- On mode, configuration, and status views, read operations send identical back-to-back commands so the response is obtained upon a single click on the “Read” button. This behavior is normal SPI operation, but is implemented this way for the convenience of the end-user.
- On all views, write operations are only performed once per click.

5.3.1 Mode registers

See Figure 14 for an overview of control options available on the “Mode” view on SPIGen. See the MC33GD3100 data sheet for a complete description of MODE1 and MODE2 registers and pin functionalities. The onboard flyback power supply provides VCC and VEE for the HV domains and can be enabled (default) or disabled in the event an external supply or characteristic is desired.

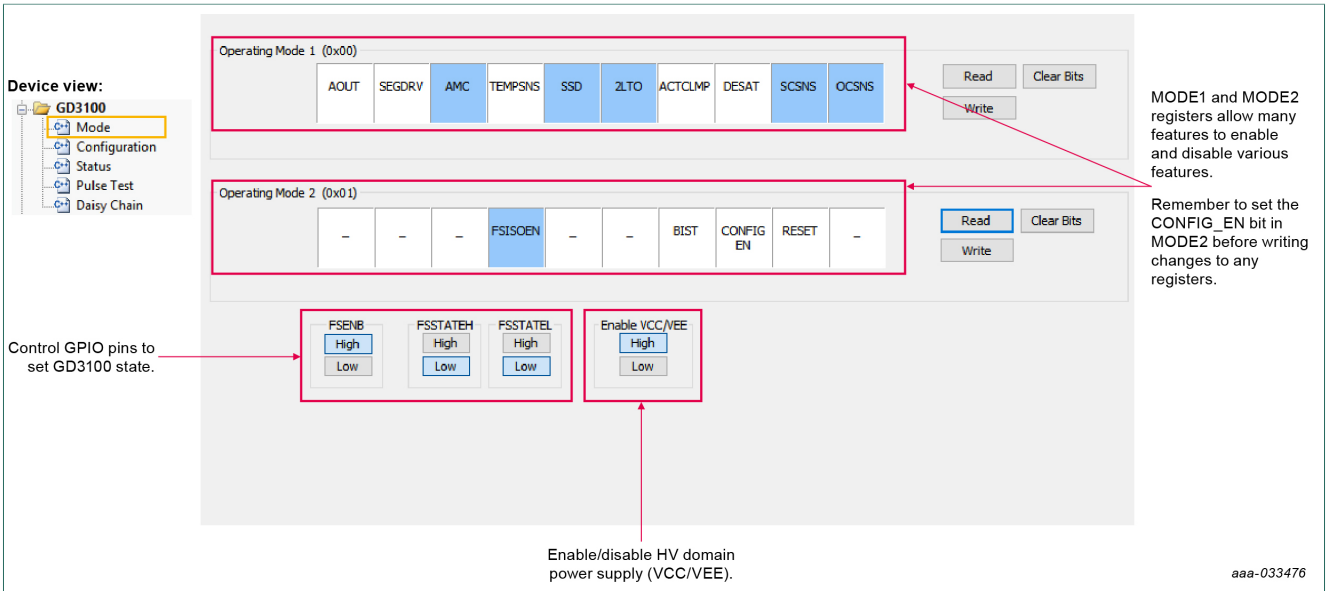

Figure 14. Mode registers and GPIO control view

5.3.2 Configuration register

See the MC33GD3100 data sheet for configuration register descriptions.

When attempting to change configuration parameters, ensure the CONFIG_EN bit in the MODE2 register is set to logic 1. Read operations send identical back-to-back commands so the response is obtained upon a single click on the **Read** button. Write operations are only performed once per click.

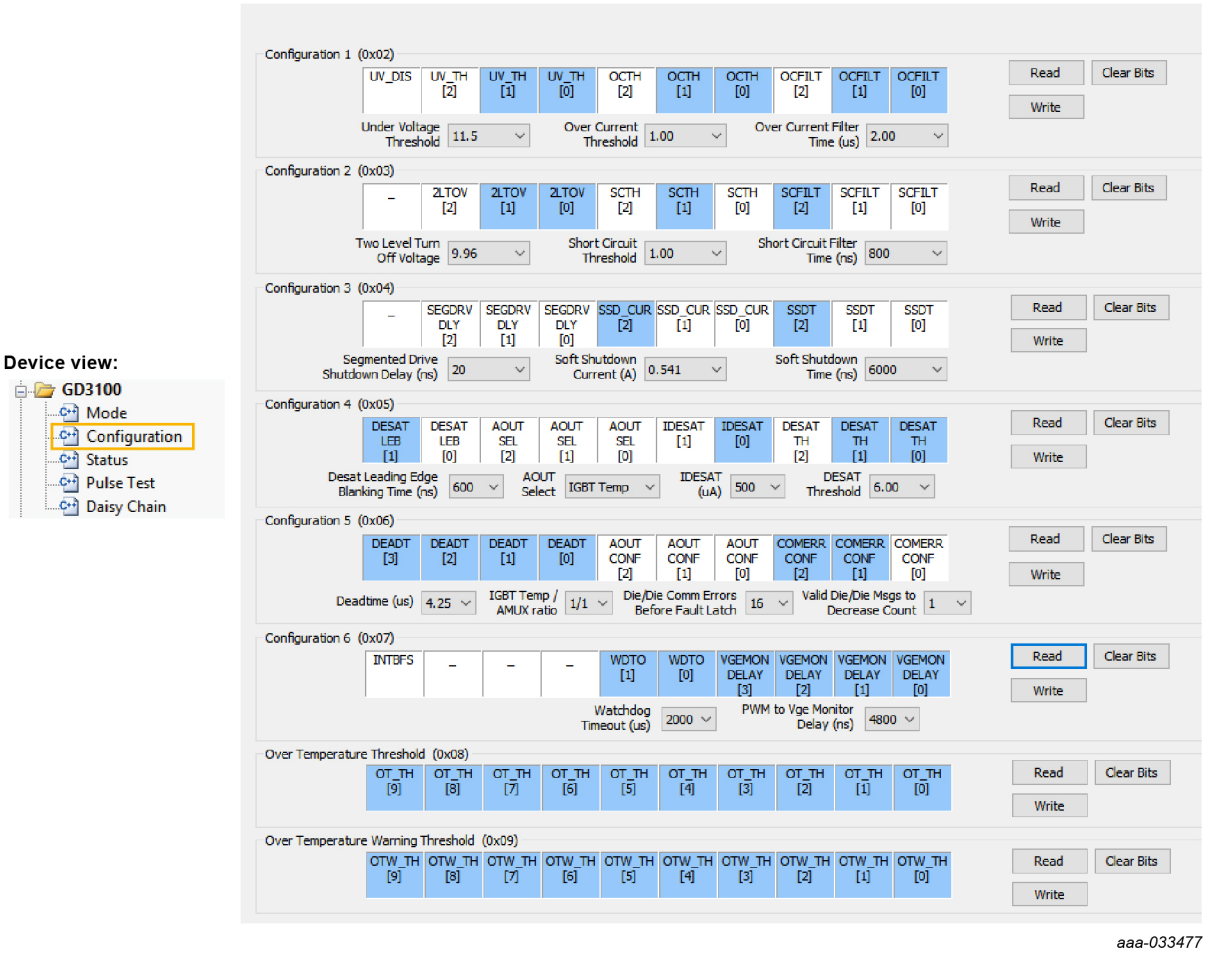

Figure 15. Configuration registers view

5.3.3 Status and mask register

See the MC33GD3100 data sheet for status and mask SPI register descriptions. INTB indicators mirror the status of the INTB pin on both high-side and low-side MC33GD3100 simultaneously. However, only one (either high side or low side) can be read at a time over SPI (selected by “SPI 0” or “SPI 1”) in this view.

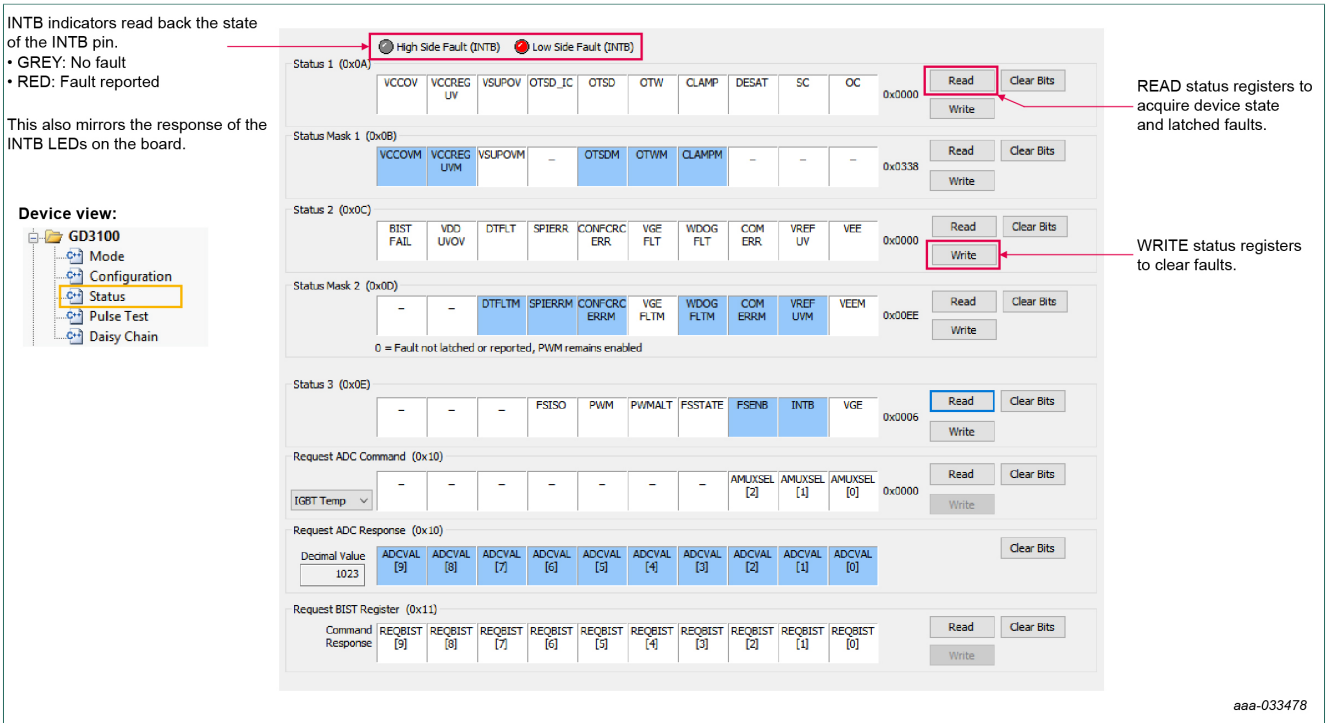

Figure 16. Status, mask, and REQADC registers view

5.3.4 Pulse test

The pulse test view allows a few simple waveforms to be applied to the PWM and PWMALT pins, to evaluate with an IGBT or SiC module.

For short-circuit testing, it is recommended to bypass dead time protection. Dead time protection can be disabled as described in Section 3.4.3. The jumpers PWMLSEL and PWMHSEL are used to disable the dead time fault protection.

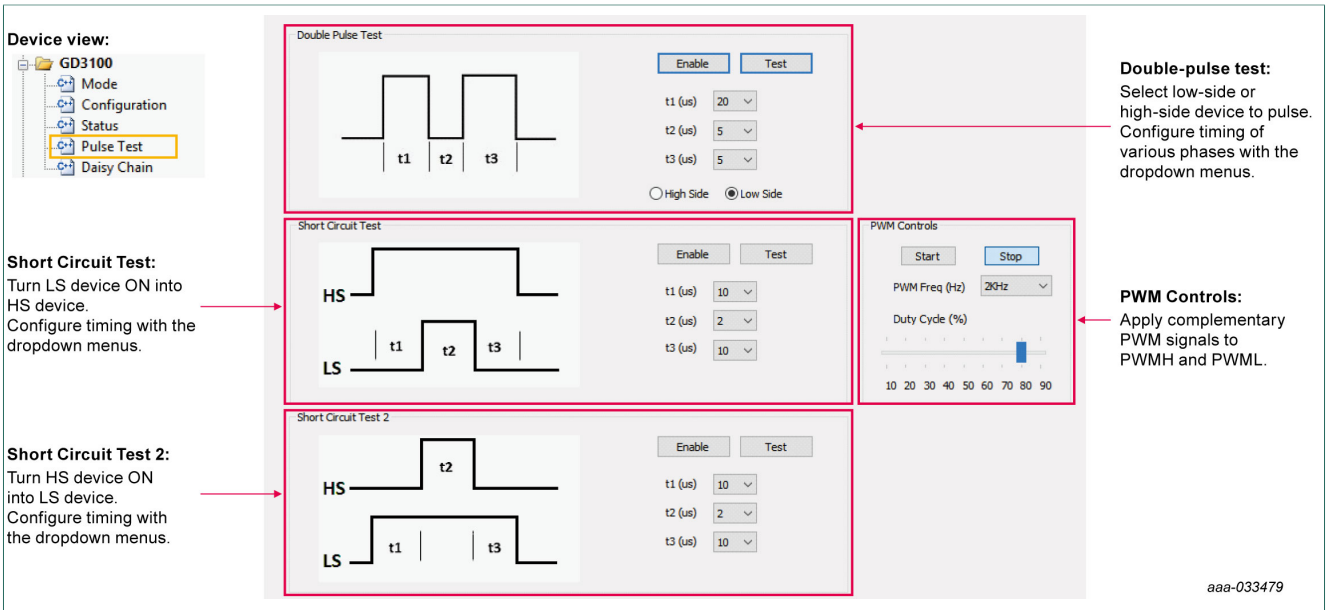

Figure 17. Pulse test view

5.3.5 Single command

The single command view contains a log of recent commands, displayed in hexadecimal format. Single SPI commands can be saved and recalled by name. Commands defined here are available for scripting in the batch commands page. SPI words sent and received (initiated from any tab) are logged here in hexadecimal and can be saved and exported in a text file. This view does not support daisy-chain length command structure (n × 24 bit length, where n > 1).

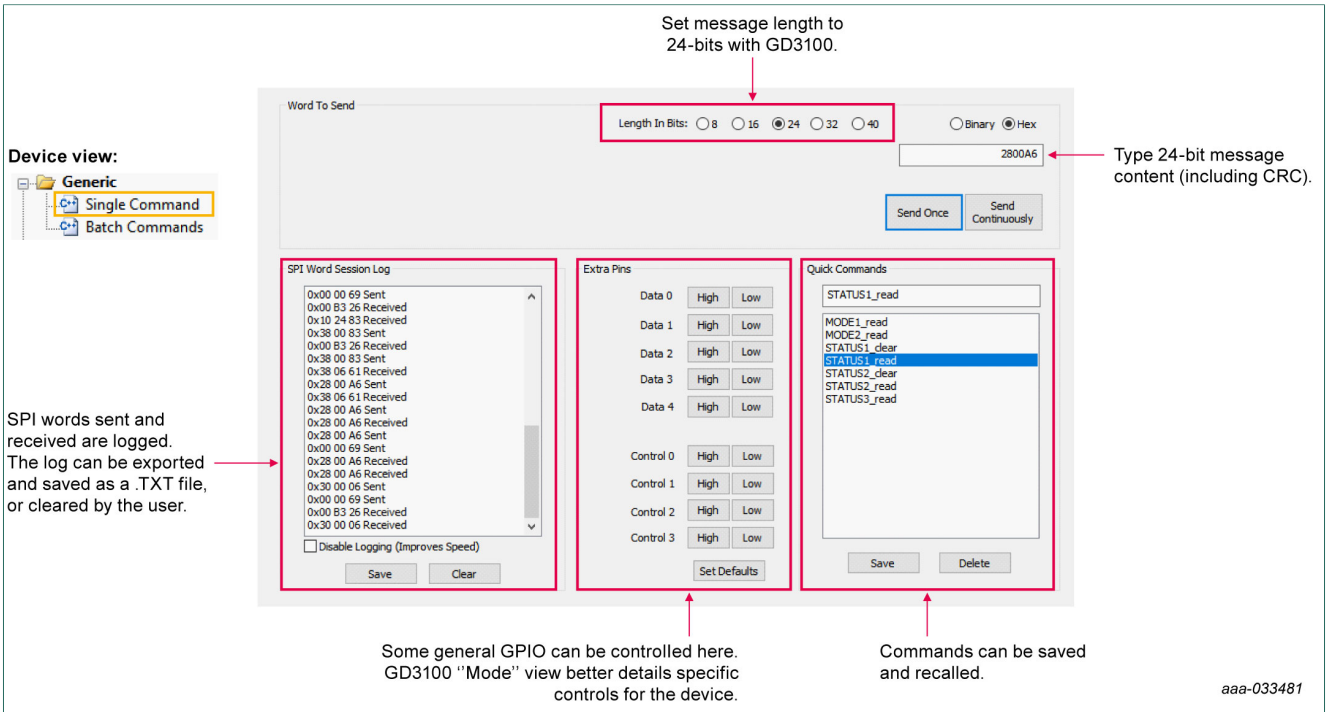

Figure 18. Single command view

5.3.6 Batch command

The batch command view allows creation of scripts containing commands defined by the single command page. Batches can be named, saved, and recalled. Batch commands are useful for quickly initializing the device after power-up.

The batch commands sent can be logged and saved in a text file. The SPI words sent/received can be viewed in hexadecimal and exported back in the single command view. This view does not support daisy-chain length command structure (n × 24 bit length, where n > 1).

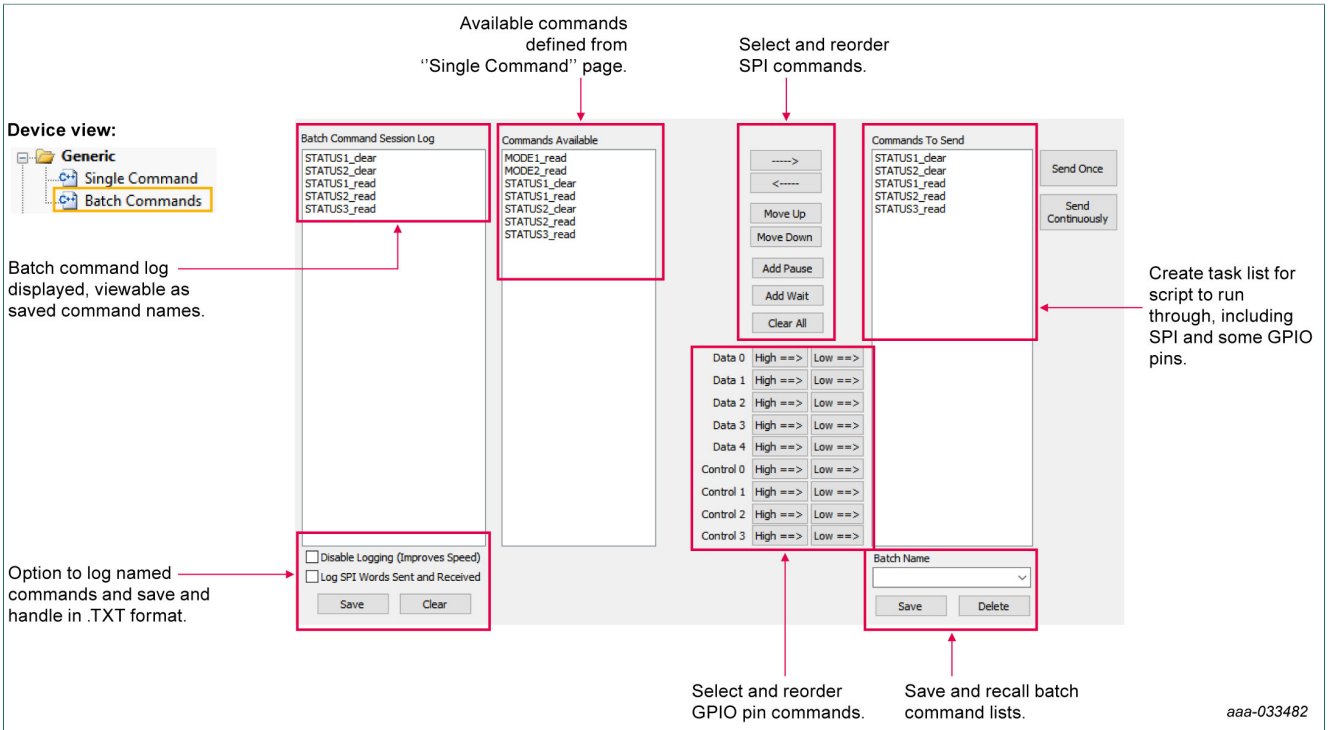

Figure 19. Batch command view

5.4 Troubleshooting

Some common issues and troubleshooting procedures are detailed below. This is not an exhaustive list by any means, and additional debug may be needed:

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (no fault reported)	Check PWM jumper position on translator board	Incorrect PWM jumpers obstruct signal path but not report fault	Set PWMH_SEL (J235) and PWML_SEL (J236) jumpers properly, for desired control method: • 3.3 V to 5.0 V translator board reviewed in Section 3.6
	Check correct firmware is in use for translator board version	Firmware includes pin definitions and pinout for KL25Z corresponding to routing and pin allocation on specific translator board revision	Check firmware version in SPIGen, according to Figure 13. Match this to microcode needed for translator board revision, stated in Section 5.2, step 6.
	Check PWM control signal	Ensure that proper PWM signal is reaching MC33GD3100	Monitor EXT_PWML (TP10) and EXT_PWMH (TP11) for commanded PWM state
	Check FSENB status (see MC33GD3100 pin 15, STATUS3)	PWM is disabled when FSENB = LOW	Set pin FSENB = HIGH to continue
	Check CONFIG_EN bit (MODE2)	PWM is disabled when CONFIG_EN is logic 1	Write CONFIG_EN = logic 0 to continue

Problem	Evaluation	Explanation	Corrective action(s)
No PWM output (fault reported)	Check VGE fault (VGE_FLT)	A short on IGBT or SiC module gate, or too low of VGEMON delay setting causes VGE fault, locking out PWM control of the gate.	Clear VGE_FLT bit (STATUS2) to continue. Increase VGEMON delay setting (CONFIG6). If safe operating condition can be guaranteed, set VGE_FLTM (MSK2) bit to logic 0, to mask fault.
	Check for short-circuit fault (SC) in STATUS1 register	SC is a severe fault that disables PWM. SC fault cannot be masked	Clear SC fault to continue. Consider adjusting SC fault settings on MC33GD3100: • Adjust short-circuit threshold setting (CONFIG2) • Adjust short-circuit filter setting (CONFIG2)
PWM output is good, but with persistent fault reported	Check for dead time fault (DTFLT) in STATUS2 register	Dead time is enforced, but fault indicates that PWM controls signals are in violation	Clear DTFLT fault bit (STATUS2). Check PWMHSEL (J10) and PWMLSEL (J9) are configured to bypass dead time faults. Consider adjusting dead time settings on MC33GD3100: • Change mandatory PWM dead time setting (CONFIG5) • Mask dead time fault (MSK2)
	Check for overcurrent (OC) fault in STATUS1 register	OC fault latches, but does not disable PWM. OC fault cannot be masked.	Clear OC fault bit (STATUS1). Adjust OC fault detection settings on MC33GD3100: • Adjust overcurrent threshold setting (CONFIG1) • Adjust overcurrent filter setting (CONFIG1)
PWM or FSSTATE rising edge has longer delay than falling edge	Check translator output voltage versus MC33GD3100 VDD voltage	Low translator output voltage (compared with correct VDD at MC33GD3100) causes the high threshold at the MC33GD3100 pin to be crossed later than commanded	Check translator output voltage selection (J233) is configured to the same level as the MC33GD3100 VDD Check VCCSEL supply or translator outputs on the translator board for excessive loading or supply droop/pulldown
WDOG_FLT reported on startup	Check VSUP and VCC are powered	On initialization, watchdog fault is reported when one die is powered up before the other	Check VSUP and VCC both have power applied. Clear WDOG_FLT bit (STATUS2) to continue.
SPIERR reported on startup	Check KL25Z/translator connection	On initialization, SPIERR can occur when the SPI bus is open, or when MC33GD3100 IC is powered up before the translator (which provides CSB).	Clear SPIERR fault to continue. Reinitialize power to MC33GD3100 after translator is powered (over USB).
SPIERR reported after SPI message	Check bit length of message sent	There is SPIERR if SCLK does not see a n*24 multiple of cycles	Use 24-bit message length for SPI messages
	Check CRC	SPIERR faults if CRC provided in sent message is not good	Use SPIGen to generate commands with valid CRC. The command can be copied in binary or hexadecimal and sent from another program.
	Check for sufficient dead time between SPI messages	SPIERR fault bit is set when the time between SPI messages (txfer_delay) received is too short. Minimum required delay time is 19 µs.	Check time between CSB rising edge (old message end) and CSB falling edge (new message start) during normal SPI read, and ensure transfer delay dead time check. SPIERR can also be cleared in BIST.
VCCREGUV reported on startup	Check VCCREG potential	Caused by low VCC	Clear VCCREGUV fault bit (STATUS1). Tune VCC-GNDISO potential with power supply set resistor (R32).

Problem	Evaluation	Explanation	Corrective action(s)
VREFUV reported on startup	Check HV domain is powered correctly	Related to slow rise time of VCC supply on HV domain, or failed VREF regulator	Clear VREFUV bit (STATUS2). Reset HV domain supply if fault bit does not clear.
	Check VCC for undervoltage condition	Low VCC is visible indirectly through other HV domain faults	Tune VCC-GNDISO using R32 feedback
VCCOV fault reported on startup	Check VEE level on suspect domain.	If VEE level is not at desired negative voltage it could cause excessive VCC level.	Check Zener diode in power supply circuit for proper value in setting VEE level. Clear VCCOV bit (STATUS1) to continue.
	Check VCC-GNDISO potential	PWM is disabled during a VCC overvoltage (20 V nom.)	Tune VCC-GNDISO potential to suitable level with power supply set resistor (R32). Clear VCCOV bit (STATUS1) to continue.
No PWM during short circuit test	Check PWMxSEL jumpers	Incorrect configuration of PWMALT pins prevent short-circuit test by enforcing dead time	For short-circuit test, set PWMLSEL (J9) and PWMHSEL (J10) to bypass dead time. See Section 3.4.3 for details.
Bad SPI data, appears to repeat previous response	Check VSUP/VDD for undervoltage condition	VDD_UV latches SPI buffer contents, preventing updated fault reporting.	Check voltage provided at VDD pin (pin 3). On each read, compare the address from the sent command and response (a difference indicates that the SPI response is latched due to inactive). Read multiple addresses to ensure a good comparison.
	Check enable VCC/VEE is set to HIGH in SPIGen GUI; see Figure 13	VCC/VEE can be enabled/disabled in software.	Enable VCC/VEE from SPIGen.
	Check VCC for undervoltage	Unpowered VCC prevents HV domain from updating data	Tune VCC-GNDISO using R32 feedback

6 Schematics, board layout, and bill of materials

The board schematics, board layout, and bill of materials are available at http://www.nxp.com/FRDMGD3100HB8EVM.com .

7 References

[1] Tool summary page for FRDMGD3100HB8EVM http://www.nxp.com/FRDMGD3100HB8EVM.com

[2] Tool summary page for FRDM-GD3100EVM http://www.nxp.com/FRDM-GD3100EVM

[3] Product summary page for GD3100 device http://www.nxp.com/GD3100

8 Revision history

Revision history

Revision	Date	Description
v.1	20200804	Initial version

9 Legal information

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