Description

The PJ75 series is a set of three-terminal low power high voltage regulators implemented in CMOS technology. They allow input voltages as high as 36V. They are available with several fixed output voltages ranging from 2.8V to 5.0V. Because of the low power dissipation, PJ75 series are widely used in a variety of equipment such as audio device, video device, communication device and so on.

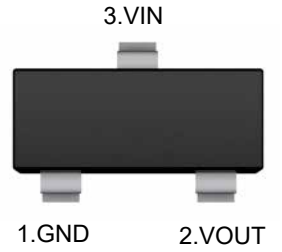
Features

- Low power consumption
- Low voltage drop
- Low temperature coefficient
- High input voltage (up to 36V)
- Quiescent current : 2.5μA
- Output voltage tolerance: ±2%

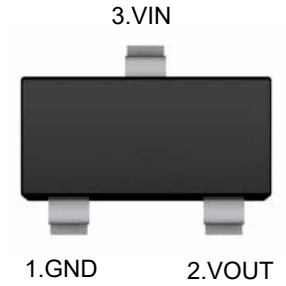
Applications

- Battery-Powered Equipment
- Ultra Low Power Microcontrollers
- Notebook Computers

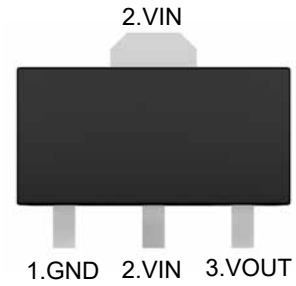
SOT-23



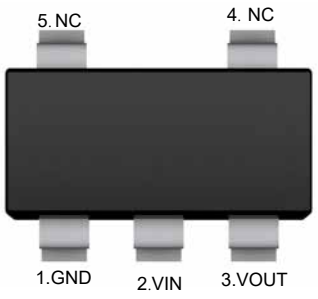
SOT-23-3



SOT-89



SOT-23-5



Functional Pin Description

Pin Name	Pin Function
NC	NO Connected
GND	Ground
VOUT	Output Voltage
VIN	Power Input Voltage

Marking Code Note

Output Voltage	Package	Marking Code
2.8V~5V	SOT-23	75XX
2.8V~5V	SOT-23-3	75XXC
2.8V~5V	SOT-23-5	75XXE
2.8V~5V	SOT-89	75XX

Note . XX : Output Voltage

Ordering Information

PJ75- □□□□□

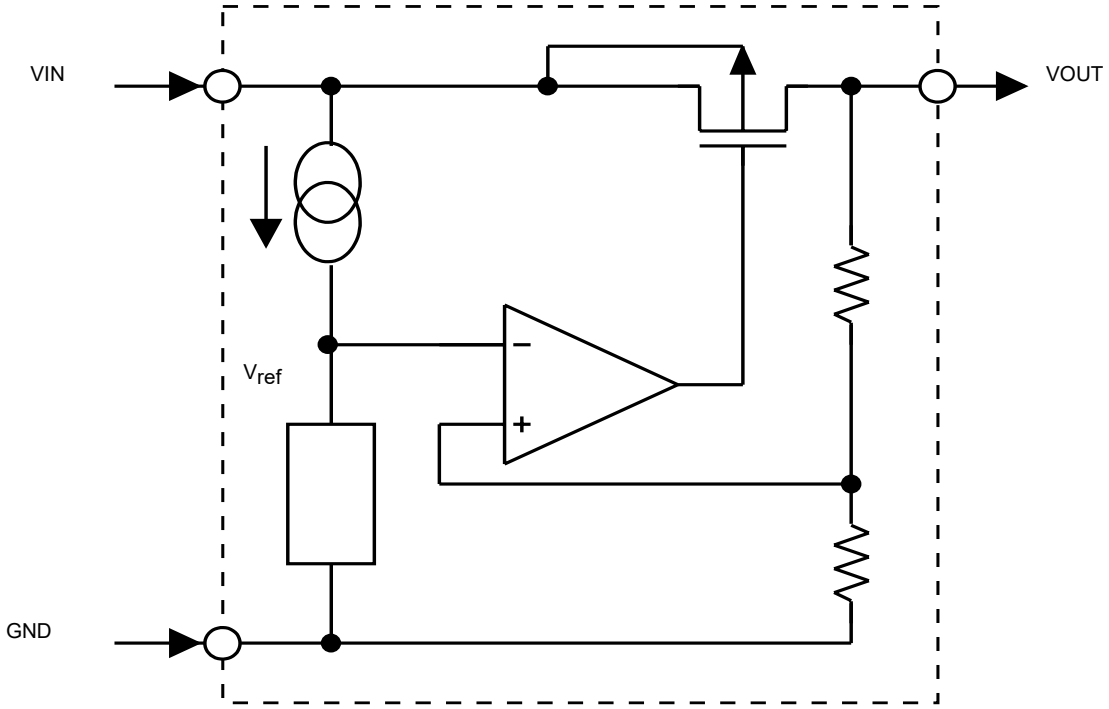
Package Type
SA : SOT-23 SC : SOT-23-3
SQ : SOT-89 SE : SOT-23-5

Output Voltage
28 : 2.8V 30 : 3.0V
33 : 3.3V 36 : 3.6V
40 : 4.0V 44 : 4.4V 50 : 5V

Output current tap
L: 100mA

Revision:A

Function Block Diagram



Absolute Maximum Ratings

Ratings at 25℃ ambient temperature unless otherwise specified.

Parameter		Value	Unit
Supply Voltage		-0.3 ~ +36	V
Power Dissipation	SOT-23	300	mW
	SOT-23-3	400	mW
	SOT-23-5	400	mW
	SOT-89	600	mW
Thermal Resistance,Junction-to-Ambient	SOT-23	330	°C/W
	SOT-23-3	380	°C/W
	SOT-23-5	300	°C/W
	SOT-89	180	°C/W
Operating Ambient Temperature		-40 ~ +85	°C
Storage temperature range		-50 ~ +125	°C

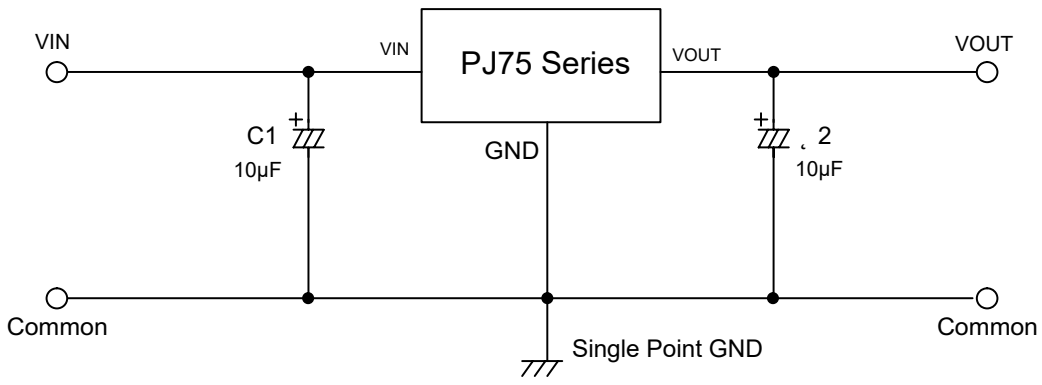
Electrical Characteristics

(V_{IN}=V_{OUT}+2, C_{IN}=10μF, C_{OUT}=10μF, T_A=25℃ , unless otherwise noted.)

Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Input Voltage	V_{IN}		--	--	36	V
Output Voltage Accuracy	ΔV_{OUT}	I_{OUT}=10mA	-2	--	+2	%
Output Current	I_{OUT}	V_{IN}=V_{OUT}+2V	70	100	--	mA
Quiescent Current	I_Q	I_{OUT}=0mA	--	2.5	3	μA
Dropout Voltage Note1	V_{DROP}	2.8V≤V_{OUT}≤3.0V, I_{OUT}=1mA	--	30	100	mV
		3.0V<V_{OUT}≤5.0V, I_{OUT}=1mA	--	25	55	
Line Regulation	ΔV_{LINE}	V_{IN}=V_{OUT}+2 to 30V,I_{OUT}=1mA	--	--	0.2	%/V
Load Regulation	ΔV_{LOAD}	V_{IN}=V_{OUT}+2V,1mA<I_{OUT}<50mA	--	25	60	mV
Thermal Shutdown Temperature	$\Delta V_{OUT}/V_{OUT}$ ×ΔT_A	V_{IN}=V_{OUT}+2V,I_{OUT}=10mA -40°C≤T_A≤85°C	--	100	--	°C

Note 1. The dropout voltage is defined as V_{IN} – V_{OUT}, when V_{OUT} is 98% of the normal value of V_{OUT}.

Typical Application Circuit



Applications Information

Input Capacitor

A 1μF ceramic capacitor is recommended to connect between VIN and GND pins to decouple input power supply glitch and noise. The amount of the capacitance may be increased without limit. This input capacitor must be located as close as possible to the device to assure input stability and less noise. For PCB layout, a wide copper trace is required for both VIN and GND.

Output Capacitor

An output capacitor is required for the stability of the LDO. The recommended minimum output capacitance is 1μF, ceramic capacitor is recommended, and temperature characteristics are X7R or X5R. Higher capacitance values help to improve load/line transient response. The output capacitance may be increased to keep low undershoot/overshoot. Place output capacitor as close as possible to V_{OUT} and GND pins.

Thermal Considerations

For continuous operation, do not exceed absolute maximum junction temperature. The maximum power dissipation depends on the thermal resistance of the IC package, PCB layout, rate of surrounding airflow, and difference between junction and ambient temperature. The maximum power dissipation can be calculated by the following formula：

$P_{D(MAX)} = (T_{J(MAX)} - T_A) / R_{\theta JA}$

Where $T_{J(MAX)}$ is the maximum operation junction temperature 125 ℃, T_A is the ambient temperature and the $R_{\theta JA}$ is the ju nction to ambient thermal resistance.

The power dissipation definition in device is：

$P_D = (V_{IN} - V_{OUT}) \times I_{OUT} + V_{IN} \times I_Q$

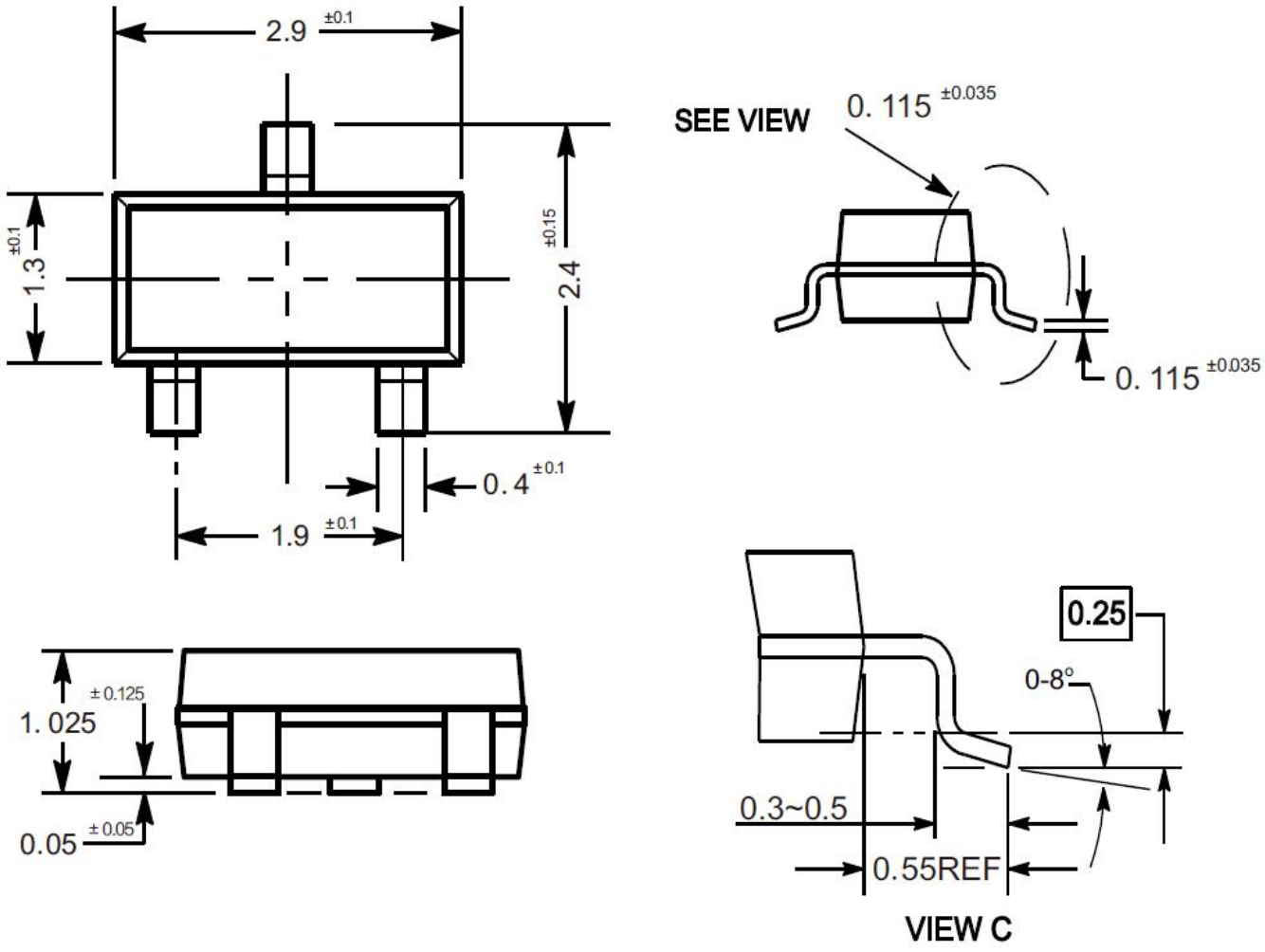
Layout Consideration

By placing input and output capacitors on the same side of the PCB as the LDO, and placing them as close as is practical to the package can achieve the best performance. The ground connections for input and output capacitors must be back to the PJ75 Series ground pin using as wide and as short of a copper trace as is practical.Connections using long trace lengths, narrow trace widths, and connections through via must be avoided. These add parasitic inductances and resistance that results in worse performance especially during transient conditions.

Package Outline

SOT-23

Dimensions in mm



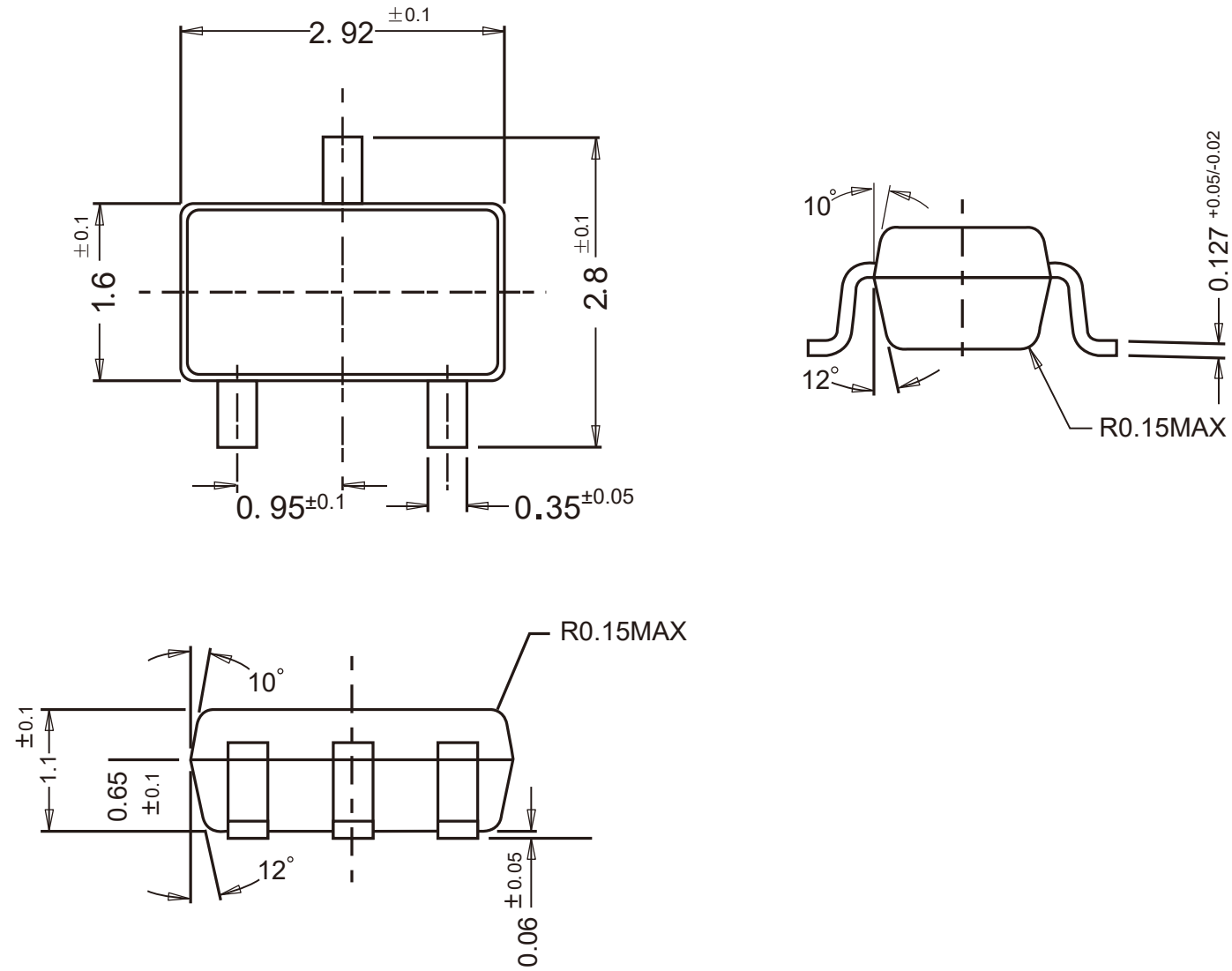
Ordering Information

Device	Package	Shipping
PJ75 Series	SOT-23	3,000PCS/Reel&7inches

Package Outline

SOT-23-3

Dimensions in mm



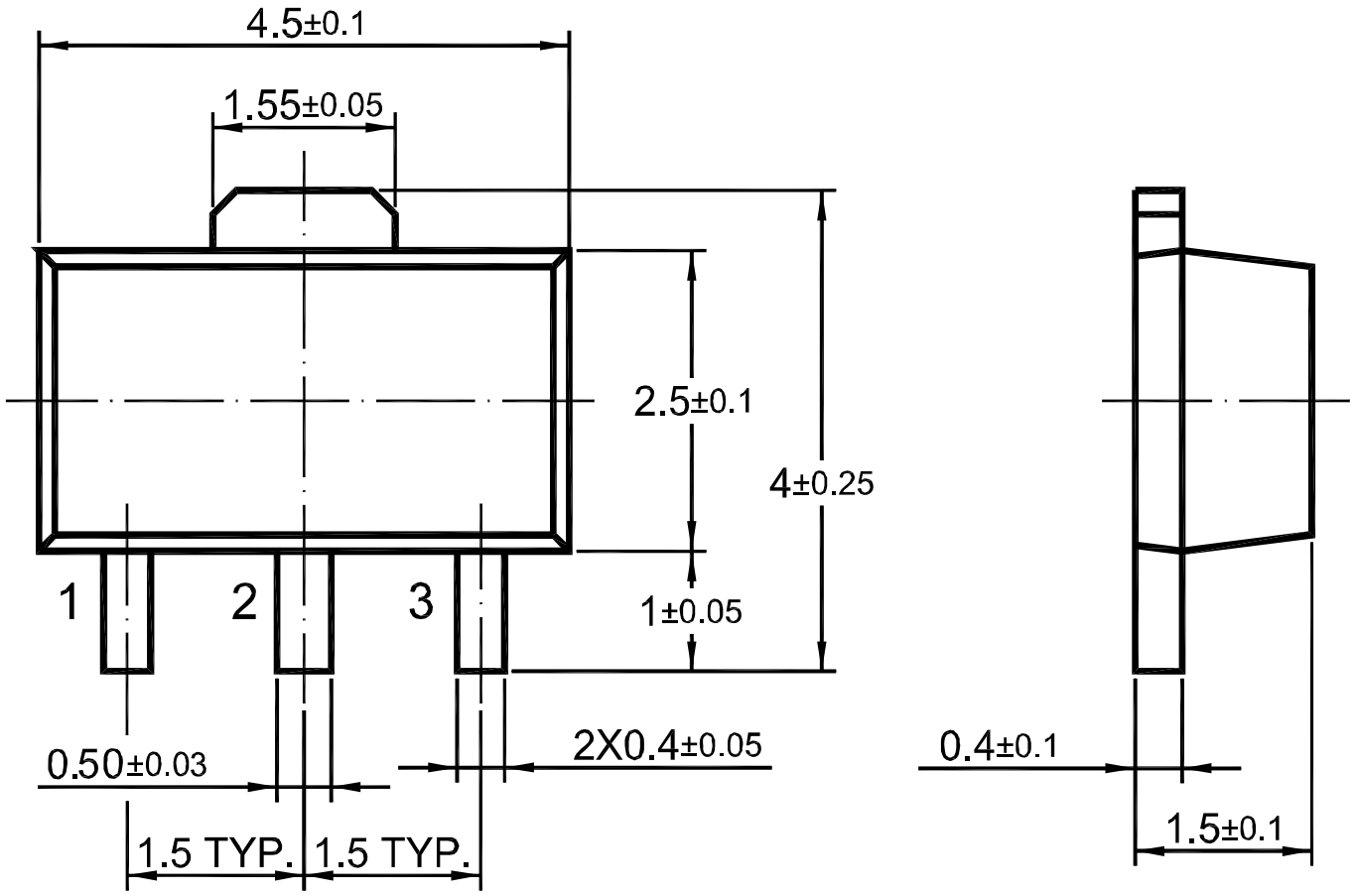
Ordering Information

Device	Package	Shipping
PJ75 Series	SOT-23-3	3,000PCS/Reel&7inches

Package Outline

SOT-89

Dimensions in mm



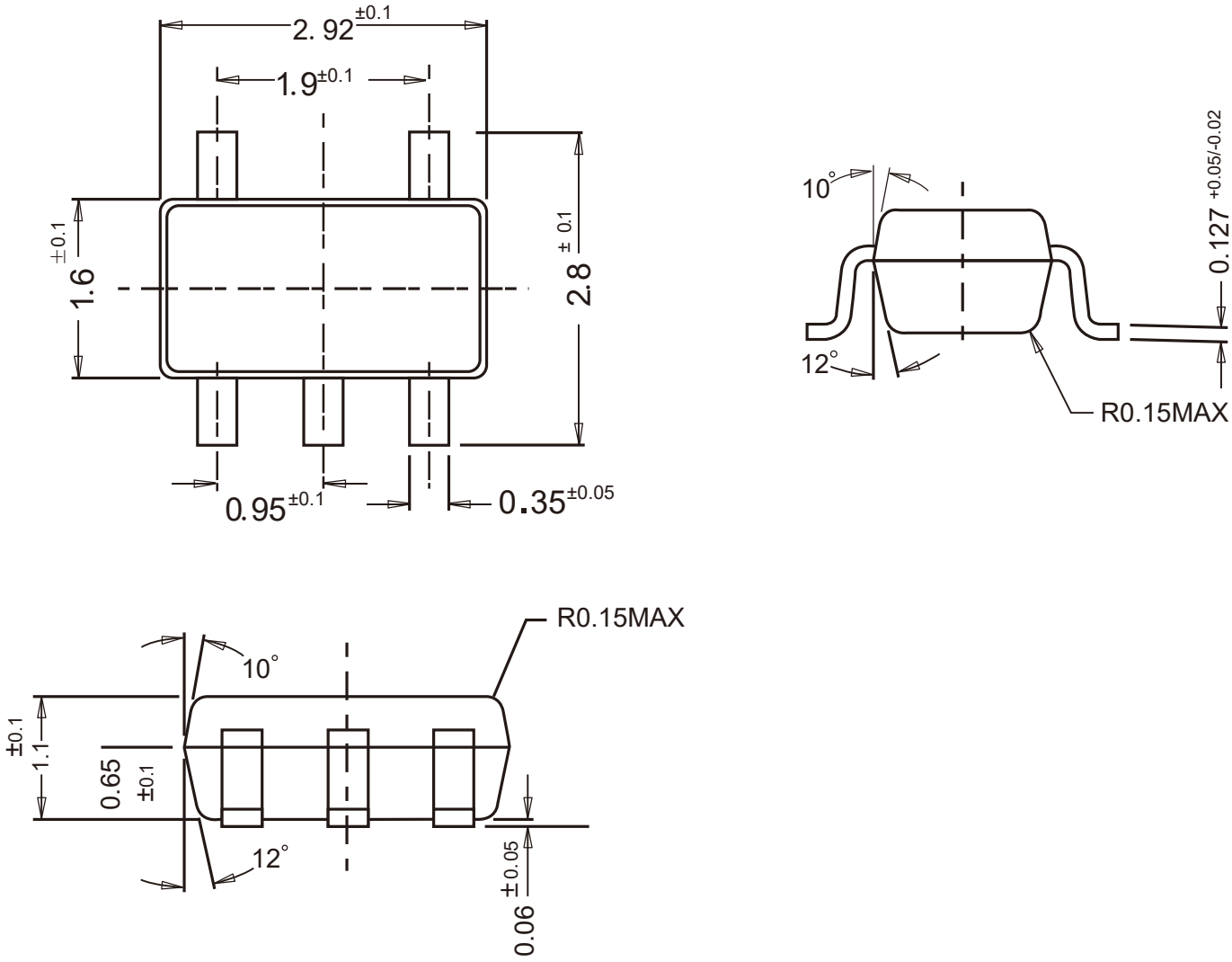
Ordering Information

Device	Package	Shipping
PJ75 Series	SOT-89	3,000PCS/Reel&13inches

Package Outline

SOT-23-5

Dimensions in mm



Ordering Information

Device	Package	Shipping
PJ75 Series	SOT-23-5	3,000PCS/Reel&7inches