Description：

SP705/706/707/708/813 series is a family of microprocessor (uP) supervisory circuit that monitors microprocessor's supply voltage and battery voltage. SP705/706/707/708/813 series integrates uP reset circuit with 200ms delay, Watchdog, manual reset circuit and a power fail comparator with 1.22V threshold. These devices reduce system complexity, hence improve system reliability.

SP705/706/707/708/813 series has several functional options. Each device generates a reset signal when VCC is lower than reset threshold. In addition, SP705, SP706 and SP813 have a watchdog timer whose timeout period is 1.6s. SP707 and SP708 provide both active low and active high reset signals, but have no watchdog function. SP813 are same as SP705/706 except active high reset is provided instead of active low.

SP705/706/707/708/813 series is ideal for applications in automotive systems, computers, controllers and intelligent instruments. All devices are available in 8 pin DIP and 8 pin SOP package.

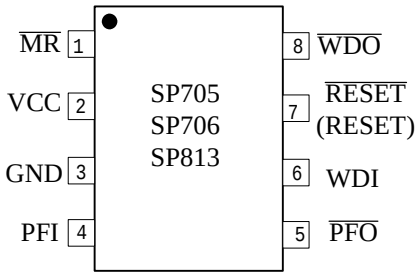
Applications：

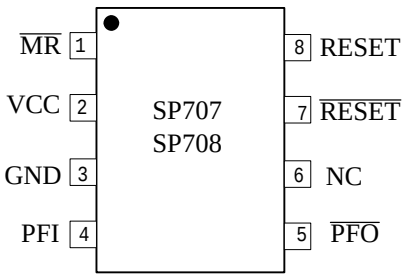
- Computers
- Controllers
- Intelligent instruments
- Automotive systems

Features：

- Guaranteed reset valid at V_{CC}=1.15V
- Reset threshold can be from 2.6V to 5.0V with 0.1V step.
- Low operating current: 52uA @5V
- Reset pulse width: 200ms
- Independent watchdog timer, 1.6s timeout(SP705/706/813)
- Voltage monitor for power fail or low battery warning
- Pin-to-pin compatible with industry standard 705/706/707/708/813
- Available in DIP8 and SOP8

Pin Assignment:





Typical Application Circuit:

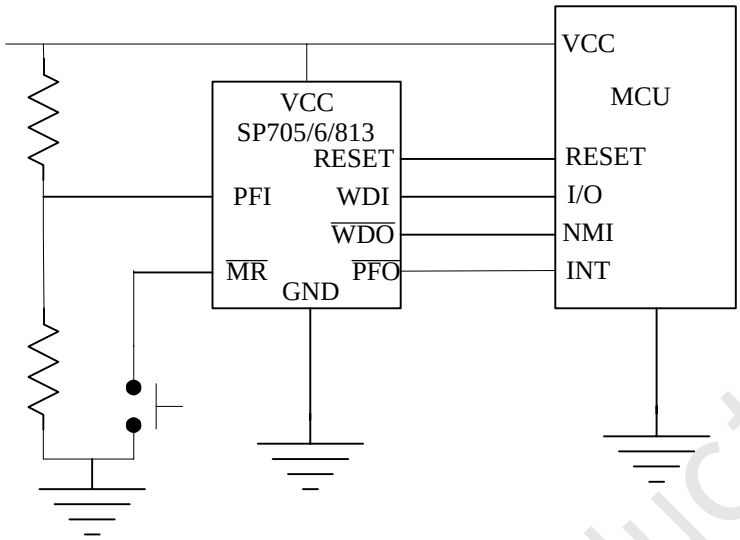


Figure 1 Typical Application Circuit

Device Function Reference Table

Part No.	Reset threshold	Reset active Low or High	Watchdog Function	Operating Temperature
SP705	4.65V	Low	Yes	－40℃--85℃
SP707	4.65V	Low and High	No	－40℃--85℃
SP813L	4.65V	High	Yes	－40℃--85℃
SP706	4.4V	Low	Yes	－40℃--85℃
SP708	4.4V	Low and High	No	－40℃--85℃
SP813M	4.4V	High	Yes	－40℃--85℃
SP706J	4.0V	Low	Yes	－40℃--85℃
SP708J	4.0V	Low and High	No	－40℃--85℃
SP813J	4.0V	High	Yes	－40℃--85℃
SP706T	3.08V	Low	Yes	－40℃--85℃
SP708T	3.08V	Low and High	No	－40℃--85℃
SP813T	3.08V	High	Yes	－40℃--85℃
SP706S	2.93V	Low	Yes	－40℃--85℃
SP708S	2.93V	Low and High	No	－40℃--85℃
SP813S	2.93V	High	Yes	－40℃--85℃
SP706R	2.63V	Low	Yes	－40℃--85℃
SP708R	2.63V	Low and High	No	－40℃--85℃
SP813R SP706P)	2.63V	High	Yes	－40℃--85℃

Note: Please contact our sales office for other reset threshold from 2.6V to 5.0V

Ordering Information:

Ordering Code = Part No. + Package Code

P: stands for DIP8
S: stands for SOP8

Refer to Device Function Reference Table on Page 2

Block Diagram:

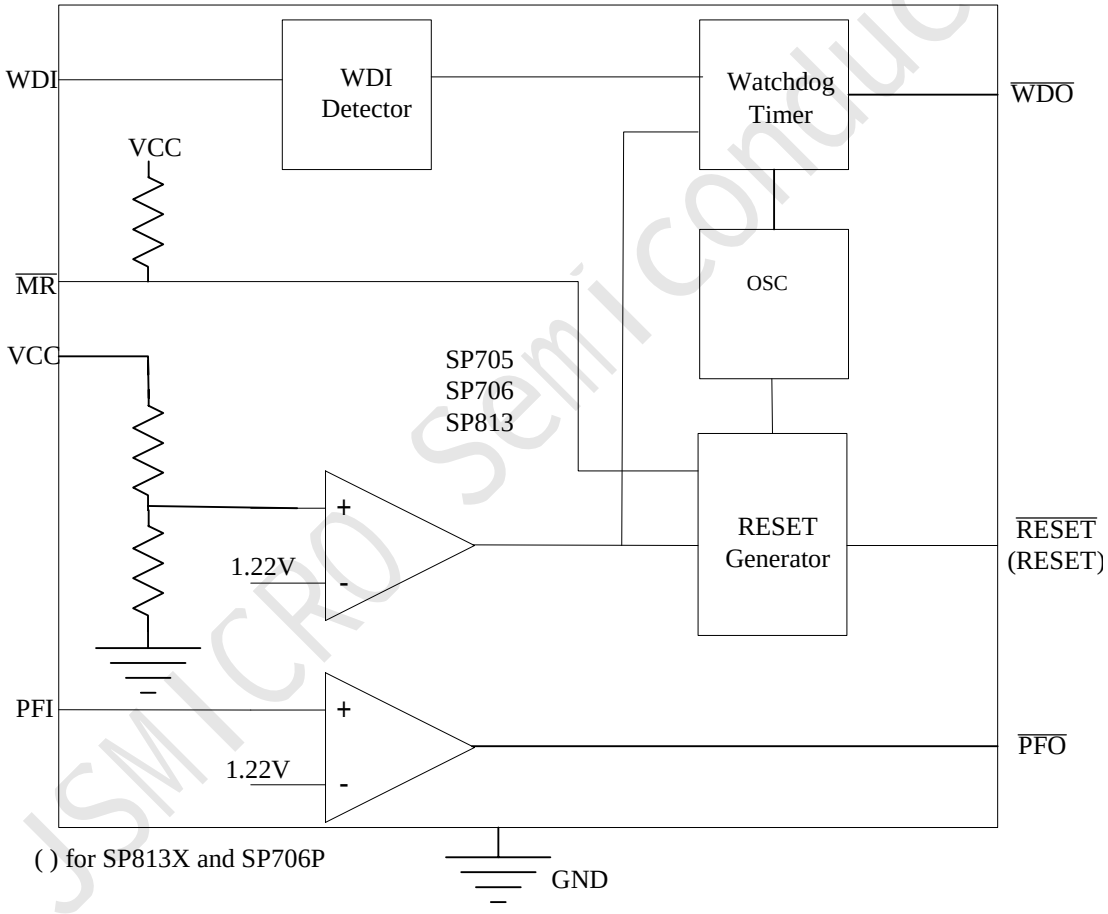


Figure 2 SP705/706/813 block Diagram

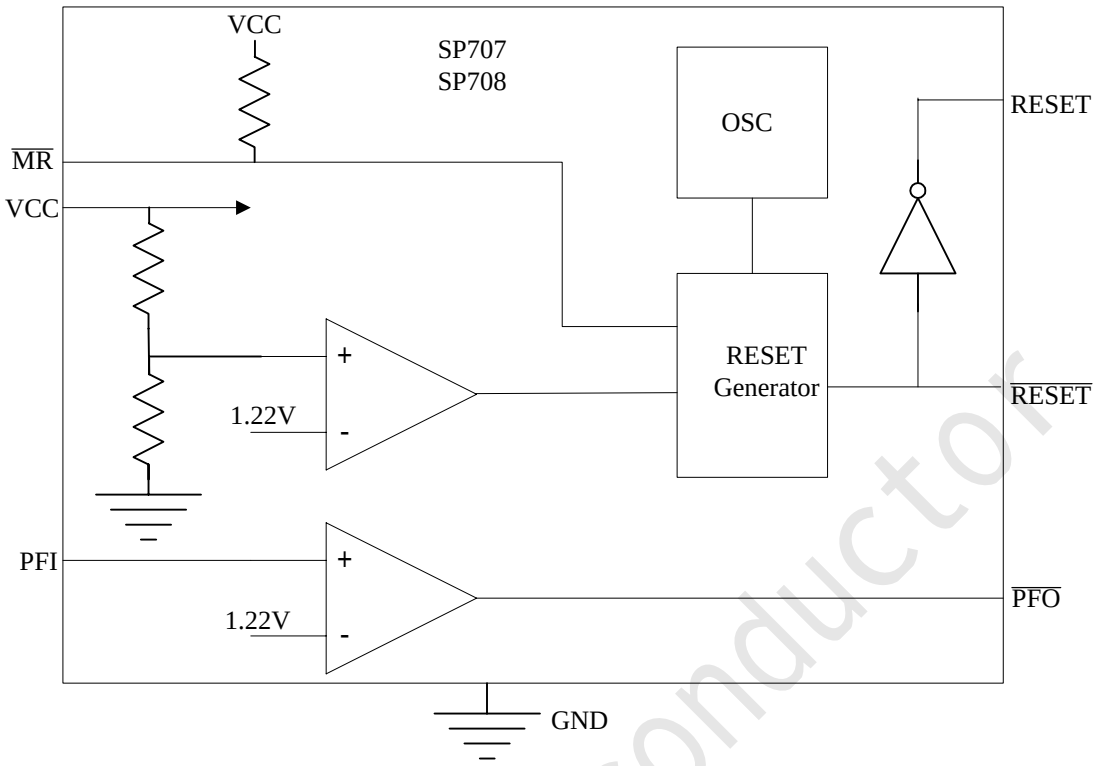


Figure 3 SP707/708 Block Diagram

Pin Description：

Pin No.			Name	Function Description
SP705 SP706X	SP707 SP708X	SP813X SP706P		
1	1	1	$\overline{MR}$	Manual reset input. When voltage at $\overline{MR}$ is pulled low, a reset pulse will be triggered. The active low input has a pull up current. It can be driven by TTL or CMOS logic as well as shorted to GND with a switch.
2	2	2	VCC	Positive supply input
3	3	3	GND	Negative supply input
4	4	4	PFI	Power fail monitor input. When the voltage at PFI is below 1.22V，PFO goes low . Connect PFI to GND or VCC when not used.
5	5	5	$\overline{PFO}$	Power fail monitor output. When the voltage at PFI is less than 1.22V, PFO goes low; otherwise PFO goes high.
6		6	WDI	Watchdog input. If WDI remains high or low for 1.6s, the on chip watchdog timer runs out and WDO goes low. Floating WDI or connecting WDI to high impedance three state buffer disables watchdog function. The watchdog timer clears whenever RESET is asserted, or WDI is three stated, or WDI sees a rising or falling edge.
7	7		$\overline{RESET}$	Active low reset output. $\overline{RESET}$ stays in low if VCC is lower than reset threshold; it remains in low for 200ms after VCC becomes higher than reset threshold or $\overline{MR}$ goes from low to high.(Figure 5)
8		8	$\overline{WDO}$	Watchdog output. WDO goes low if watchdog timer finishes its 1.6s count, and will not go high again until the watchdog timer is cleared. Whenever VCC is below reset threshold, WDO stays low, and as soon as VCC rises above reset threshold, WDO goes high without delay.
	8	7	RESET	Active high reset output. RESET stays in high if VCC is lower than reset threshold; it remains in high for 200ms after VCC becomes higher than reset threshold or $\overline{MR}$ goes from low to high.(Figure 5)

Absolute Maximum Ratings：

Terminal Voltage(With respect to GND)：

V_{CC}……-0.3V to 6.0V

Other Inputs ……..……..-0.3V to 6.0V

Terminal Current

V_{CC}…….20mA

GND……20mA

All Input Pins……..20mA

All Output Pins……20mA

Thermal Resistance (DIP8)……120℃/W

Power Dissipation (SOP8)……190℃/W

Maximum Junction Temperature…...150℃

Operating Temperature…...－40℃ to 85℃

Storage Temperature…....－65℃ to 150℃

Lead Temperature(Soldering)……..300℃

ESD Rating(HBM)…….2KV

Stresses beyond those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions above those indicated in the operational sections of the specifications is not implied. Exposure to Absolute Maximum Rating Conditions for extended periods may affect device reliability.

Electrical Characteristics

(V_{CC}=5V, T_A=－40℃ to 85℃, Typical values are measured at T_A=25℃,unless otherwise noted)

Parameters	Symbol	Test Conditions		Min	Typ	Max	Unit
Operating Voltage Range	V_{CC}			1.15		5.5	V
Supply Current	I_{VCC}	SP705/706X/813X			52	105	uA
		SP707/708X			30	60	
Reset Threshold	V_{RES}	SP705/707/813L		4.5	4.65	4.75	V
		SP706/708/813M		4.25	4.4	4.5	
		SP706J/708J/813J		3.9	4.0	4.1	
		SP706T/708T/813T		3.0	3.08	3.15	
		SP706S/708S/813S		2.85	2.93	3.0	
		SP706P/706R/708R/813R		2.55	2.63	2.70	
Reset Threshold Hysteresis	H_{VRES}				$0.01V_{RES}$		V
Reset Pulse Width	t_{RES}			140	200	280	ms
$\overline{RESET}$ or RESET Output Voltage	V_{OH1}	I_{SOURCE}=800uA		V_{CC}-1.2			V
		I_{SOURCE}=8uA,V_{CC}=1.2V		1.0			
	V_{OL1}	I_{SINK}=3.2mA				0.3	V
		I_{SINK}=150uA,V_{CC}=1.2V				0.3	
Watchdog timeout period	t_{WD}			1	1.6	2.25	s
WDI Pulse Width	t_{WP}	V_{CC}=5V		50			ns
		V_{CC}<4.5V		120			
WDI Input Threshold		Low				$0.16V_{CC}$	V
		High	V_{CC}=5V	3.5			
			V_{CC}<4.5V	$0.75V_{CC}$			

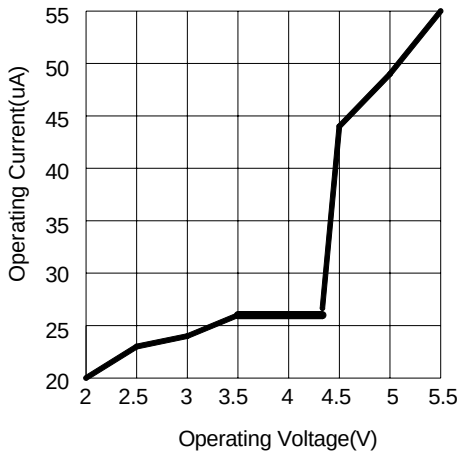
Electrical Characteristics (Continued)

Parameters	Symbol	Test Conditions		Min.	Typ.	Max.	Unit
WDI Pull up Resistance		$V_{CC}>V_{RES}$		125	250	500	KΩ
WDI Pull down Resistance		$V_{CC}>V_{RES}$		88	175	350	KΩ
WDO Output Voltage	V_{OH2}	I_{SOURCE}=800uA		V_{CC}-1.2			V
	V_{OL2}	I_{SINK}=3.2mA				0.3	
MR Pull up Current		MR=0V	V_{CC}=5V	100	250	600	uA
			V_{CC}=4V	60	152	360	
			V_{CC}=3V	32	75	180	
			V_{CC}=2.5V	20	44	105	
MR Pulse Width	T_{MR}	V_{CC}=5V		150			ns
		V_{CC}<4.5V		500			
MR Input Threshold		V_{CC}=5V	Low			0.8	V
			High	2.0			
		V_{CC}<4.5V	Low			0.16V_{CC}	
			High	0.65V_{CC}			
MR's Delay to RESET	t_{MD}	V_{CC}=5V				250	ns
		V_{CC}<4.5V				750	
PFI Input Threshold	V_{PFI}			1.184	1.22	1.256	V
PFI Input Current	I_{PFI}				0		nA
PFO Output Voltage	V_{OH3}	I_{SOURCE}=800uA		V_{CC}-1.2			V
	V_{OL3}	I_{SINK}=3.2mA				0.3	

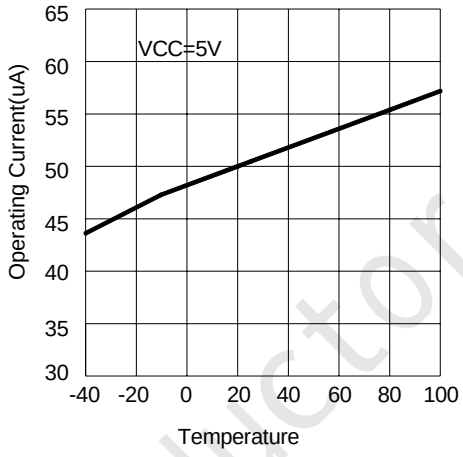
Note : Parts are 100% production tested at 25°C. Specifications over full temperature range are guaranteed by 6-sigma statistical process control and by design

Typical Operating Characteristics

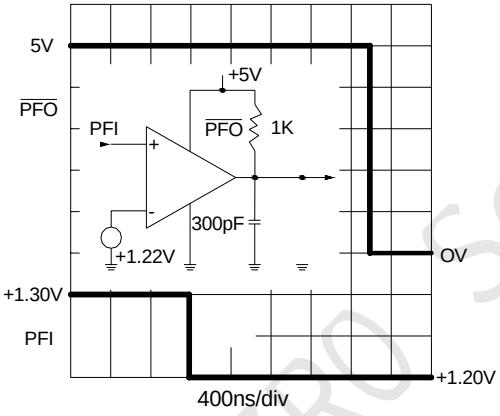
SP706 Operating Current vs. Operating Voltage



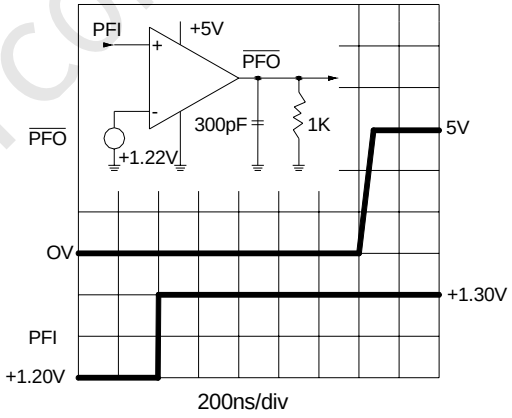
SP706 Operating Current vs. Temperature



Power-fail Comparator assertion Response Time



Power-fail Comparator De-assertion Response Time



Detailed Description：

SP705/706/707/708/813 series is a microprocessor supervisory circuit that monitors the power supply to digital circuits such as microprocessor, controller and memory . These devices assert reset during power up, power down or brownout condition to prevent code execution errors.

RESET output

On power up, once VCC reaches 1.15V, SP705/706/707/708/813 series output a reset signal . As VCC increases, the reset signal stays valid; When VCC rises above reset threshold, an internal timer releases RESET ($\overline{\text{RESET}}$) after 200ms. RESET ($\overline{\text{RESET}}$) becomes valid once VCC dips below reset threshold during power down or in brownout condition. If brownout occurs in the middle of a previously initiated

reset pulse, the pulse will continue for at least another 140ms. On power down , once VCC falls below reset threshold, RESET stays valid and is guaranteed in the correct logic state until VCC drops below 1.15V for the whole temperature range. Please refer to Figure 5.

SP705/706 series provide active low $\overline{RESET}$ signal；SP707/708 series provide both active high and active low RESET signals；SP813 series provide active high RESET signal.

Watchdog Timer

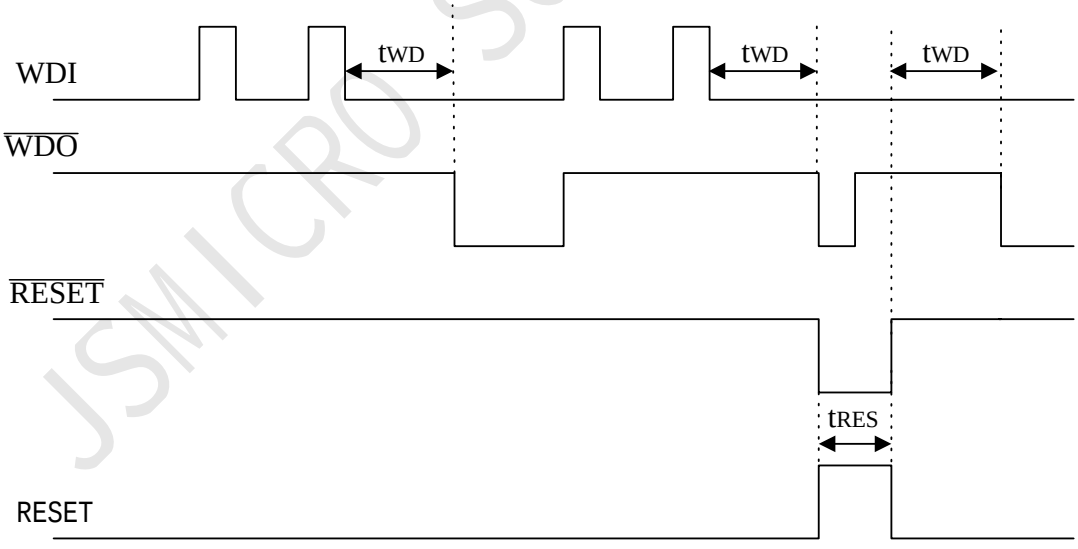
SP705/706/813 series have an independent watchdog timer that can monitor uP's activity. If uP does not toggle the watchdog input (WDI) within 1.6s and WDI is not three-stated, WDO goes low. As long as RESET is asserted, or WDI is three-stated, or WDI is left floating, the watchdog timer stays cleared and will not count, in this case WDO is in high state. When VCC stays below reset threshold, WDO goes low whether or not the watchdog timer has timed out yet. Please refer to figure 4.

Manual Reset

Manual reset input allows reset signal to be triggered by push button or switch. The push button or switch is effectively debounced by 140ms minimum reset pulse width. $\overline{MR}$ is TTL/CMOS logic compatible. $\overline{MR}$ can be used to force a watchdog timeout to generate a reset pulse in SP705/706/813 series by connecting WDO to $\overline{MR}$ Please refer to Figure 5.

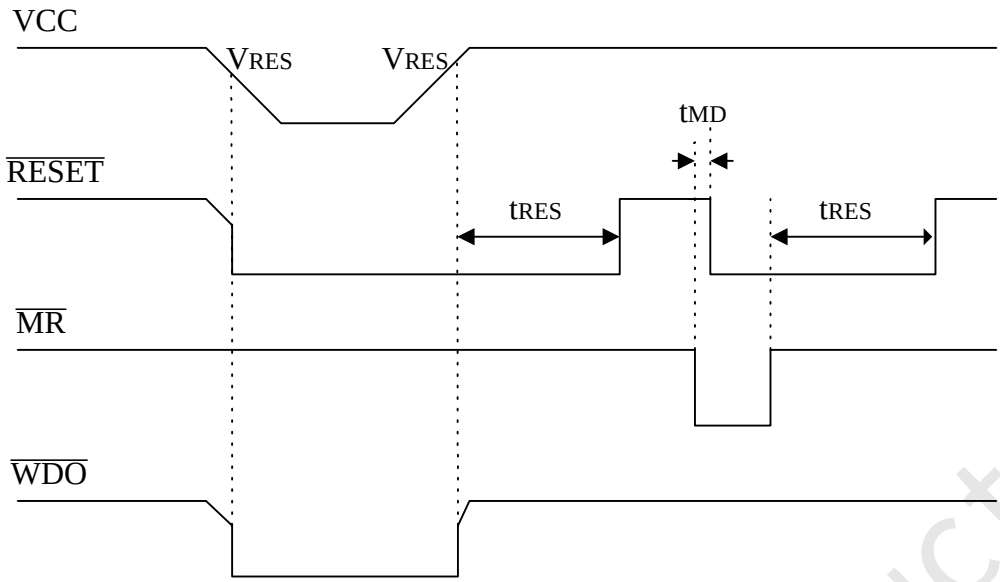
Power fail Comparator

The power fail comparator can be used for various purpose because its output and noninverting input are not internally connected. The inverting input is internally connected to a 1.22V reference voltage.



Note 1: $\overline{RESET}$ (RESET) is triggered by $\overline{MR}$
Note 2: RESET is for SP813X and SP706P only

Figure 4 Watchdog Timing



Note: Active high RESET is the inverse of the $\overline{\text{RESET}}$ shown

Figure 5 $\overline{\text{RESET}}$,$\overline{\text{MR}}$ and $\overline{\text{WDO}}$ timing with WDI floating

Application Information

Ensuring a Valid $\overline{\text{RESET}}$ Output Down to VCC=0V

When VCC falls below 1.15V, the SP705/706/707/708 series $\overline{\text{RESET}}$ output no longer sinks current, it becomes an open circuit, hence $\overline{\text{RESET}}$ output is at undetermined voltage. If a pull-down resistor is added from $\overline{\text{RESET}}$ pin to GND as shown in Figure 6, then $\overline{\text{RESET}}$ output will be held at low state. The resistor's value is not critical. it should be about 100KΩ, large enough not to load $\overline{\text{RESET}}$, small enough to pull RESET to ground.

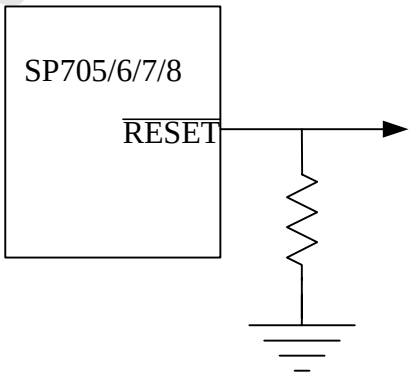


Figure 6 RESET Valid to Ground Circuit

Monitoring voltages other than the unregulated DC Input

You can monitor voltages other than the unregulated DC by connecting a voltage divider to PFI and adjusting the ratio appropriately. If required, add a hysteresis by connecting a resistor (with a value approximately 10 times the sum of 2 resistors in voltage divider network) between PFI and PFO. A capacitor between PFI and GND will reduce the power fail circuit's sensitivity to high-frequency noise on

the line being monitored. RESET can be asserted on the other voltage in addition to VCC line by connecting PFO pin to MR pin, in this case, a RESET pulse will be initiated when PFI drops below 1.22V. Figure 7 shows SP705/706/707/708 series configured to assert RESET when VCC falls below reset threshold, or when +12V power supply falls below 10V.

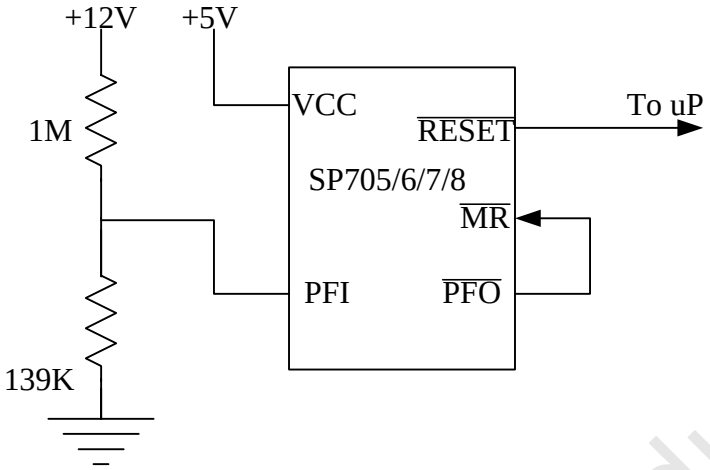


Figure 7 Monitoring Both +5V and +12V

Monitoring a Negative Voltage

The power fail comparator can also monitor a negative supply rail as shown in Figure 8. When the negative rail is good (A negative voltage of large magnitude), PFO is low, and when the negative rail is degraded(A negative voltage of less magnitude), PFO is high. By adding the resistors and transistor as shown, a high PFO triggers a RESET pulse. As long as PFO remains high, the SP705/706/707/708/813 series will keep RESET asserted. Note that the circuit's accuracy depends on the PFI threshold tolerance, the VCC line and the resistors.

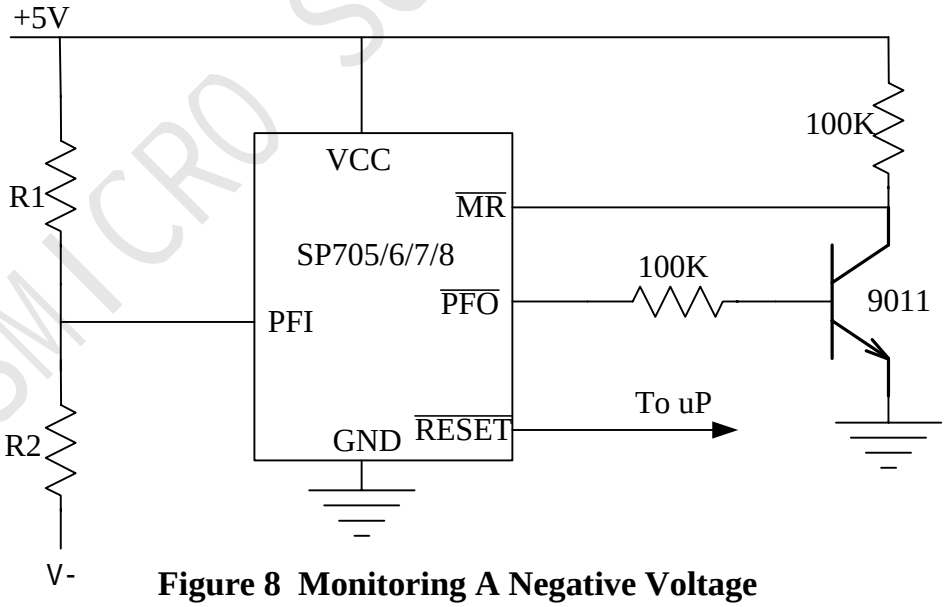


Figure 8 Monitoring A Negative Voltage

Interfacing to uPs with Bidirectional Reset Pins

uPs with bi-directional reset pins, such as the MOTOROLA 68HC11 series, can contend with SP705/706/707/708/813 series RESET output. For example, if the RESET output is driven high and uP wants to pull it low, indeterminate logic levels may result. To correct this, connect a 4.7KΩ resistor

between the RESET output and the uP reset I/O as shown in Figure 9. Buffer the RESET output to other system components.

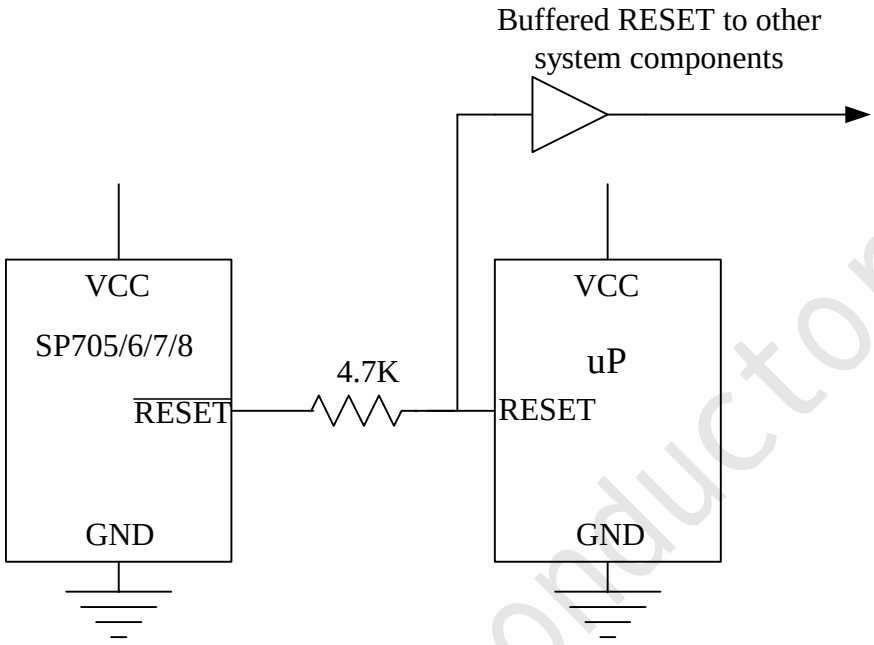
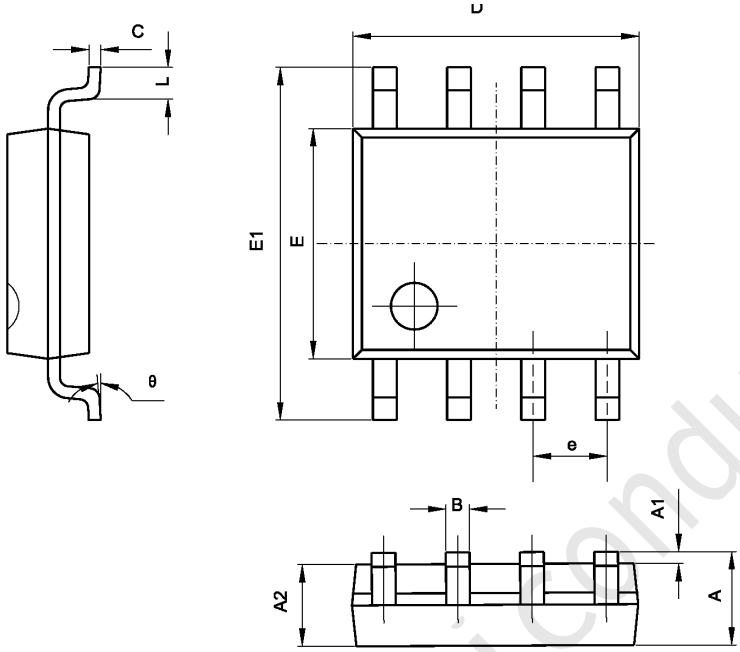


Figure 9 Interfacing to uPs with Bidirectional Reset I/O

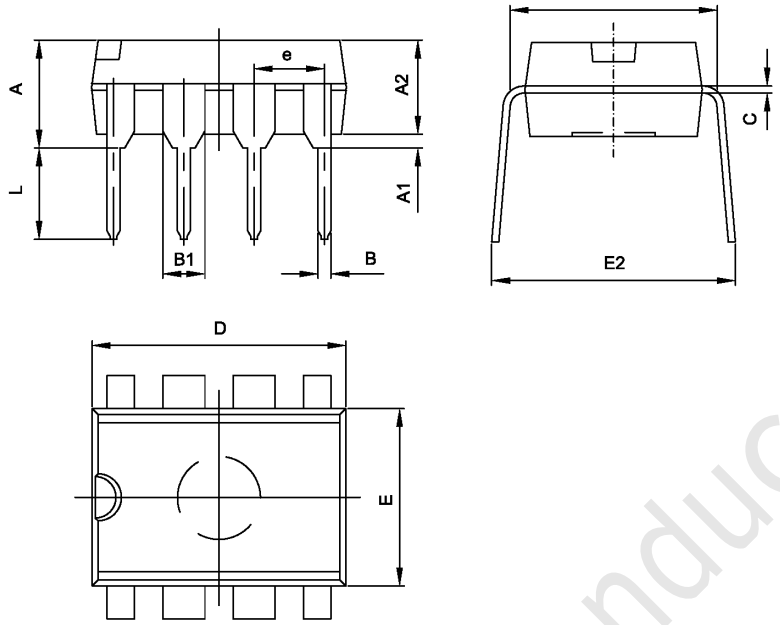
Package Information

SOP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
B	0.330	0.510	0.013	0.020
C	0.190	0.250	0.007	0.010
D	4.780	5.000	0.188	0.197
E	3.800	4.000	0.150	0.157
E1	5.800	6.300	0.228	0.248
e	1.270(TYP)		0.050(TYP)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

DIP8 Package Outline Dimensions



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	3.710	4.310	0.146	0.170
A1	0.510		0.020	
A2	3.200	3.600	0.126	0.142
B	0.360	0.560	0.014	0.022
B1	1.524(TYP)		0.060(TYP)	
C	0.204	0.360	0.008	0.014
D	9.000	9.400	0.354	0.370
E	6.200	6.600	0.244	0.260
E1	7.620(TYP)		0.300(TYP)	
e	2.540(TYP)		0.100(TYP)	
L	3.000	3.600	0.118	0.142
E2	8.200	9.400	0.323	0.370