TEXAS INSTRUMENTS

**OPA991-Q1, OPA2991-Q1, OPA4991-Q1**
SBOSA12H – MARCH 2020 – REVISED MARCH 2024

# OPAx991-Q1 Automotive, 40V Rail-to-Rail Input or Output, Low Offset Voltage, Low Noise Op Amp

## 1 Features

- AEC-Q100 qualified for automotive applications
  - Temperature grade 1: –40°C to +125°C, $T_A$
  - Device HBM ESD classification level 2A
  - Device CDM ESD classification level C6
- Low offset voltage: ±125µV
- Low offset voltage drift: ±0.3µV/°C
- Low noise: 10.8nV/√Hz at 1kHz
- High common-mode rejection: 130dB
- Low bias current: ±10pA
- Rail-to-rail input and output
- Wide bandwidth: 4.5MHz GBW
- High slew rate: 21V/µs
- High capacitive load drive: 1nF
- MUX-friendly/comparator inputs
  - Amplifier operates with differential inputs up to supply rail
  - Amplifier can be used in open-loop or as comparator
- Low quiescent current: 560µA per amplifier
- Wide supply: ±1.35V to ±20V, 2.7V to 40V
- Robust EMIRR performance

## 2 Applications

- Optimized for AEC-Q100 grade 1 applications
- Infotainment and cluster
- Passive safety
- Body electronics and lighting
- HEV/EV inverter and motor control
- On-board (OBC) and wireless charger
- Powertrain current sensor
- Advanced driver assistance systems (ADAS)
- High-side current sensing

## 3 Description

The OPAx991-Q1 family (OPA991-Q1, OPA2991-Q1, and OPA4991-Q1) is a family of high voltage (40V) general purpose operational amplifiers for automotive application. These devices offer exceptional DC precision and AC performance, including rail-to-rail input or output, low offset (±125µV, typical), low offset drift (±0.3µV/°C, typical), low noise (10.8nV/√Hz and 1.8µV$_{PP}$), and 4.5MHz bandwidth.
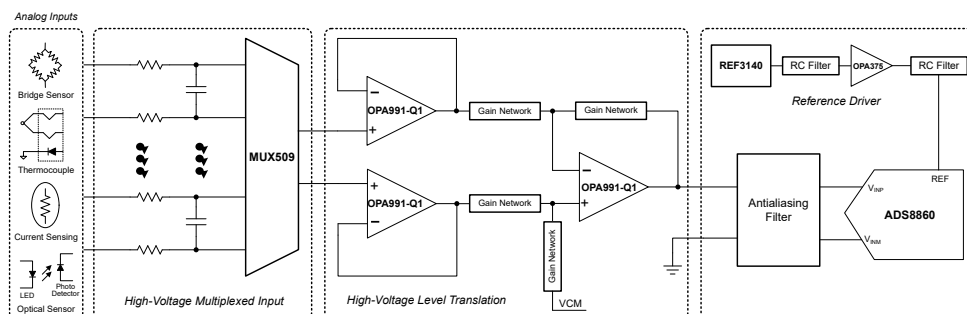
Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75mA), high slew rate (21V/µs), and high capacitive load drive (1nF) make the OPAx991-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

The OPAx991-Q1 family of op amps is available in standard packages (such as SOT-23, SC70, SOIC, VSSOP, and TSSOP) and is specified from –40°C to 125°C.

### Package Information

| PART NUMBER | CHANNEL COUNT | PACKAGE[1] | PACKAGE SIZE[2] |
|---|---|---|---|
| OPA991-Q1 | Single | DBV (SOT-23, 5) | 2.9mm × 2.8mm |
| | | DBV (SOT-23, 6) | 2.9mm × 2.8mm |
| | | DCK (SC70, 5) | 2mm × 2.1mm |
| OPA2991-Q1 | Dual | DGK (VSSOP, 8) | 3mm × 4.9mm |
| | | PW (TSSOP, 8) | 3mm × 6.4mm |
| | | D (SOIC, 8) | 4.9mm × 6mm |
| OPA4991-Q1 | Quad | DYY (SOT-23, 14) | 4.2mm × 3.26mm |
| | | PW (TSSOP, 14) | 5mm × 6.4mm |
| | | D (SOIC, 14) | 8.65mm × 6mm |

(1) For all available packages, see the orderable addendum at the end of the data sheet.

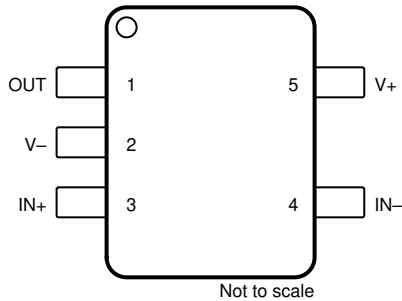(2) The package size (length × width) is a nominal value and includes pins, where applicable.
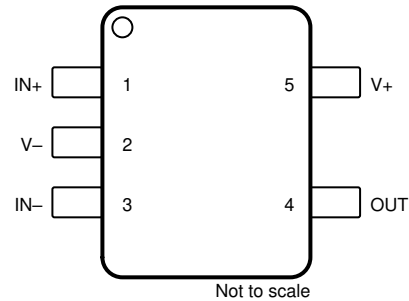


**OPAx991-Q1 in a High-Voltage Signal Chain**

# Table of Contents

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

# 4 Pin Configuration and Functions



**Figure 4-1. OPA991-Q1 DBV Package,
5-Pin SOT-23
(Top View)**



**Figure 4-2. OPA991-Q1 DCK Package,
5-Pin SC70
(Top View)**

**Table 4-1. Pin Functions: OPA991-Q1**

| PIN | | | TYPE[1] | DESCRIPTION |
|---|---|---|---|---|
| NAME | DBV | DCK | | |
| IN+ | 3 | 1 | I | Noninverting input |
| IN- | 4 | 3 | I | Inverting input |
| OUT | 1 | 4 | O | Output |
| V+ | 5 | 5 | — | Positive (highest) power supply |
| V− | 2 | 2 | — | Negative (lowest) power supply |

(1)   I = input, O = output
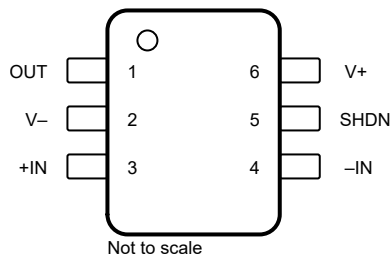


**Figure 4-3. OPA991S-Q1 DBV Package,
6-Pin SOT-23
(Top View)**

**Table 4-2. Pin Functions: OPA991S-Q1**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN+ | 3 | I | Noninverting input |
| IN− | 4 | I | Inverting input |
| OUT | 1 | O | Output |
| SHDN | 5 | I | Shutdown: low = amplifier enabled, high = amplifier disabled. See *Shutdown* section for more information. |
| V+ | 6 | — | Positive (highest) power supply |
| V− | 2 | — | Negative (lowest) power supply |

1.   I = input, O = output

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

Not to scale

**Figure 4-4. OPA2991-Q1 D, PW, and DGK Package,**
**8-Pin SOIC, TSSOP, and VSSOP**
**(Top View)**

**Table 4-3. Pin Functions: OPA2991-Q1**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| IN1– | 2 | I | Inverting input, channel 1 |
| IN2– | 6 | I | Inverting input, channel 2 |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| V+ | 8 | — | Positive (highest) power supply |
| V– | 4 | — | Negative (lowest) power supply |

(1)    I = input, O = output

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

```
            ○
OUT1  ┤ 1          14 ├  OUT4
IN1−  ┤ 2          13 ├  IN4−
IN1+  ┤ 3          12 ├  IN4+
V+    ┤ 4          11 ├  V−
IN2+  ┤ 5          10 ├  IN3+
IN2−  ┤ 6           9 ├  IN3−
OUT2  ┤ 7           8 ├  OUT3
```

Not to scale

**Figure 4-5. OPA4991-Q1 D, DYY, and PW Package,**
**14-Pin SOIC, SOT-23, and TSSOP**
**(Top View)**

**Table 4-4. Pin Functions: OPA4991-Q1**

| PIN | | TYPE[1] | DESCRIPTION |
|---|---|---|---|
| NAME | NO. | | |
| IN1+ | 3 | I | Noninverting input, channel 1 |
| IN1− | 2 | I | Inverting input, channel 1 |
| IN2+ | 5 | I | Noninverting input, channel 2 |
| IN2− | 6 | I | Inverting input, channel 2 |
| IN3+ | 10 | I | Noninverting input, channel 3 |
| IN3− | 9 | I | Inverting input, channel 3 |
| IN4+ | 12 | I | Noninverting input, channel 4 |
| IN4− | 13 | I | Inverting input, channel 4 |
| OUT1 | 1 | O | Output, channel 1 |
| OUT2 | 7 | O | Output, channel 2 |
| OUT3 | 8 | O | Output, channel 3 |
| OUT4 | 14 | O | Output, channel 4 |
| V+ | 4 | — | Positive (highest) power supply |
| V− | 11 | — | Negative (lowest) power supply |

(1)     I = input, O = output

# 5 Specifications

## 5.1 Absolute Maximum Ratings

over operating ambient temperature range (unless otherwise noted) [1]

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| Supply voltage, $V_S$ = (V+) – (V–) | | 0 | 42 | V |
| Signal input pins | Common-mode voltage [3] | (V–) – 0.5 | (V+) + 0.5 | V |
| | Differential voltage [3] | | $V_S$ + 0.2 | V |
| | Current [3] | –10 | 10 | mA |
| Output short-circuit [2] | | Continuous | | |
| Operating ambient temperature, $T_A$ | | –55 | 150 | °C |
| Junction temperature, $T_J$ | | | 150 | °C |
| Storage temperature, $T_{stg}$ | | –65 | 150 | °C |

(1) Operation outside the *Absolute Maximum Ratings* may cause permanent device damage. *Absolute Maximum Ratings* do not imply functional operation of the device at these or any other conditions beyond those listed under *Recommended Operating Conditions*. If used outside the *Recommended Operating Conditions* but within the *Absolute Maximum Ratings,* the device may not be fully functional, and this may affect device reliability, functionality, performance, and shorten the device lifetime.

(2) Short-circuit to ground, one amplifier per package. This device has been designed to limit *electrical* damage due to excessive output current, but extended short-circuit current, especially with higher supply voltage, can cause excessive heating and eventual *thermal* destruction. See the *Thermal Protection* section for more information.

(3) Input pins are diode-clamped to the power-supply rails. Input signals that may swing more than 0.5 V beyond the supply rails must be current limited to 10 mA or less.

## 5.2 ESD Ratings

| | | | VALUE | UNIT |
|---|---|---|---|---|
| $V_{(ESD)}$ | Electrostatic discharge | Human body model (HBM), per AEC Q100-002[1] | OPA991SQDBVRQ1 only | ±1000 | V |
| | | | All other devices | ±2000 | |
| | | Charged device model (CDM), per AEC Q100-011 | | ±1000 | |

(1) AEC Q100-002 indicates HBM stressing is done in accordance with the ANSI/ESDA/JEDEC JS-001 specification.

## 5.3 Recommended Operating Conditions

over operating ambient temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---|---|---|---|---|
| $V_S$ | Supply voltage, (V+) – (V–) | 2.7 | 40 | V |
| $V_I$ | Input voltage range | (V–) – 0.1 | (V+) + 0.1 | V |
| $V_{IH}$ | High level input voltage at shutdown pin (amplifier disabled) | (V–) + 1.1 | (V–) + 20[1] | V |
| $V_{IL}$ | Low level input voltage at shutdown pin (amplifier enabled) | (V–) | (V-) + 0.2 | V |
| $T_A$ | Specified ambient temperature | –40 | 125 | °C |

(1) Cannot exceed V+.

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.4 Thermal Information for Single Channel

| THERMAL METRIC [1] | | OPA991-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | DCK (SC70) | DBV (SOT-23) | | |
| | | 5 PINS | 6 PINS | 5 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 202.6 | 167.8 | 187.4 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 101.5 | 107.9 | 86.2 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 47.8 | 49.7 | 54.6 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.8 | 33.9 | 27.8 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 47.4 | 49.5 | 54.3 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1)     For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.5 Thermal Information for Dual Channel

| THERMAL METRIC [1] | | OPA2991-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | DGK (VSSOP) | |
| | | 8 PINS | 8 PINS | 8 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 132.6 | 185.1 | 176.5 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 73.4 | 74.0 | 68.1 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 76.1 | 115.7 | 98.2 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 24.0 | 12.3 | 12.0 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 75.4 | 114.0 | 96.7 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1)     For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

## 5.6 Thermal Information for Quad Channel

| THERMAL METRIC [1] | | OPA4991-Q1 | | | UNIT |
|---|---|---|---|---|---|
| | | D (SOIC) | PW (TSSOP) | DYY (SOT-23) | |
| | | 14 PINS | 14 PINS | 14 PINS | |
| $R_{\theta JA}$ | Junction-to-ambient thermal resistance | 101.4 | 118.0 | 110.7 | °C/W |
| $R_{\theta JC(top)}$ | Junction-to-case (top) thermal resistance | 57.6 | 47.6 | 55.9 | °C/W |
| $R_{\theta JB}$ | Junction-to-board thermal resistance | 57.3 | 60.9 | 35.3 | °C/W |
| $\psi_{JT}$ | Junction-to-top characterization parameter | 18.5 | 6.0 | 2.3 | °C/W |
| $\psi_{JB}$ | Junction-to-board characterization parameter | 56.9 | 60.4 | 35.1 | °C/W |
| $R_{\theta JC(bot)}$ | Junction-to-case (bottom) thermal resistance | N/A | N/A | N/A | °C/W |

(1)     For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.7 Electrical Characteristics

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{O\,UT}$ = $V_S$ / 2, unless otherwise noted.

| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OFFSET VOLTAGE** | | | | | | | |
| $V_{OS}$ | Input offset voltage | $V_{CM}$ = V– | | | ±125 | ±895 | µV |
| | | | $T_A$ = –40°C to 125°C | | | ±925 | |
| $dV_{OS}/dT$ | Input offset voltage drift | | $T_A$ = –40°C to 125°C | | ±0.3 | | µV/°C |
| PSRR | Input offset voltage versus power supply | $V_{CM}$ = V–, $V_S$ = 4 V to 40 V | $T_A$ = –40°C to 125°C | | ±0.3 | ±1 | µV/V |
| | | $V_{CM}$ = V–, $V_S$ = 2.7 V to 40 V[3] | | | ±1 | ±5 | |
| | Channel separation | f = 0 Hz | | | 5 | | µV/V |
| **INPUT BIAS CURRENT** | | | | | | | |
| $I_B$ | Input bias current | | | | ±10 | | pA |
| $I_{OS}$ | Input offset current | | | | ±10 | | pA |
| **NOISE** | | | | | | | |
| $E_N$ | Input voltage noise | f = 0.1 Hz to 10 Hz | | | 1.8 | | µV$_{PP}$ |
| | | | | | 0.3 | | µV$_{RMS}$ |
| $e_N$ | Input voltage noise density | f = 1 kHz | | | 10.8 | | nV/√Hz |
| | | f = 10 kHz | | | 9.4 | | |
| $i_N$ | Input current noise | f = 1 kHz | | | 82 | | fA/√Hz |
| **INPUT VOLTAGE RANGE** | | | | | | | |
| $V_{CM}$ | Common-mode voltage range | | | (V–) – 0.1 | | (V+) + 0.1 | V |
| CMRR | Common-mode rejection ratio | $V_S$ = 40 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair) | $T_A$ = –40°C to 125°C | 107 | 130 | | dB |
| | | $V_S$ = 4 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair) | | 82 | 100 | | |
| | | $V_S$ = 2.7 V, (V–) – 0.1 V < $V_{CM}$ < (V+) – 2 V (Main input pair)[3] | | 75 | 95 | | |
| | | $V_S$ = 2.7 V to 40 V, (V+) – 1 V < $V_{CM}$ < (V+) + 0.1 V (Aux input pair) | | | 85 | | |
| **INPUT CAPACITANCE** | | | | | | | |
| $Z_{ID}$ | Differential | | | | 100 ‖ 9 | | MΩ ‖ pF |
| $Z_{ICM}$ | Common-mode | | | | 6 ‖ 1 | | TΩ ‖ pF |
| **OPEN-LOOP GAIN** | | | | | | | |
| $A_{OL}$ | Open-loop voltage gain | $V_S$ = 40 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V | | 120 | 145 | | dB |
| | | | $T_A$ = –40°C to 125°C | | 142 | | |
| | | $V_S$ = 4 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V | | 104 | 130 | | |
| | | | $T_A$ = –40°C to 125°C | | 125 | | |
| | | $V_S$ = 2.7 V, $V_{CM}$ = V– (V–) + 0.1 V < $V_O$ < (V+) – 0.1 V[3] | | 101 | 120 | | |
| | | | $T_A$ = –40°C to 125°C | | 118 | | |
| **FREQUENCY RESPONSE** | | | | | | | |
| GBW | Gain-bandwidth product | | | | 4.5 | | MHz |
| SR | Slew rate | $V_S$ = 40 V, G = +1, $C_L$ = 20 pF | | | 21 | | V/µs |
| $t_S$ | Settling time | To 0.01%, $V_S$ = 40 V, $V_{STEP}$ = 10 V , G = +1, $C_L$ = 20 pF | | | 2.5 | | µs |
| | | To 0.01%, $V_S$ = 40 V, $V_{STEP}$ = 2 V , G = +1, $C_L$ = 20 pF | | | 1.5 | | |
| | | To 0.1%, $V_S$ = 40 V, $V_{STEP}$ = 10 V , G = +1, $C_L$ = 20 pF | | | 2 | | |
| | | To 0.1%, $V_S$ = 40 V, $V_{STEP}$ = 2 V , G = +1, $C_L$ = 20 pF | | | 1 | | |
| | Phase margin | G = +1, $R_L$ = 10 kΩ, $C_L$ = 20 pF | | | 60 | | ° |
| | Overload recovery time | $V_{IN}$ × gain > $V_S$ | | | 400 | | ns |
| THD+N | Total harmonic distortion + noise [1] | $V_S$ = 40 V, $V_O$ = 3 $V_{RMS}$, G = 1, f = 1 kHz | | | 0.00021% | | |

## 5.7 Electrical Characteristics (continued)

For $V_S$ = (V+) – (V–) = 2.7 V to 40 V (±1.35 V to ±20 V) at $T_A$ = 25°C, $R_L$ = 10 kΩ connected to $V_S$ / 2, $V_{CM}$ = $V_S$ / 2, and $V_{O\,UT}$ = $V_S$ / 2, unless otherwise noted.

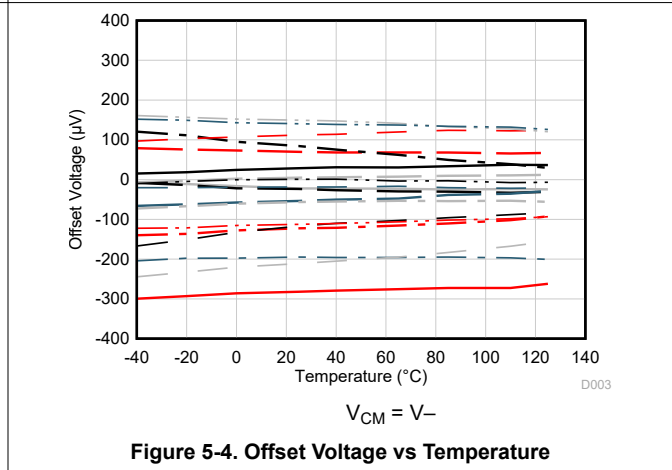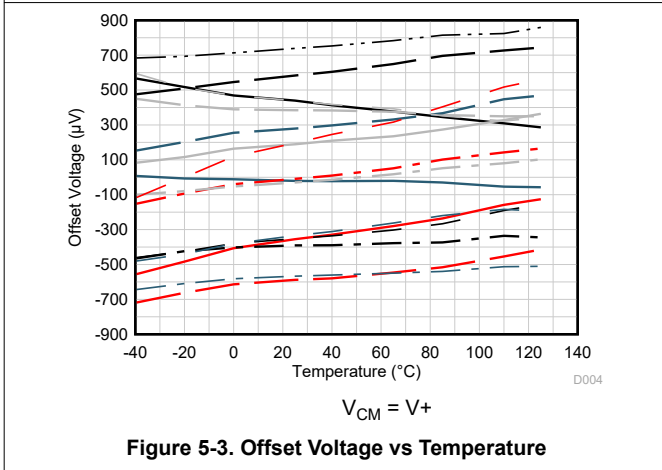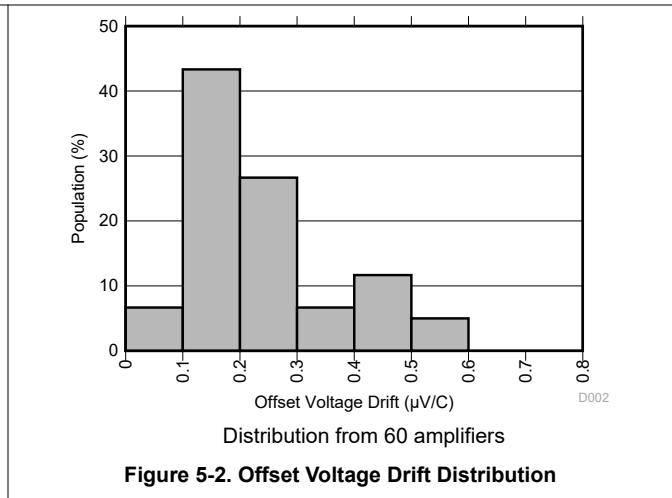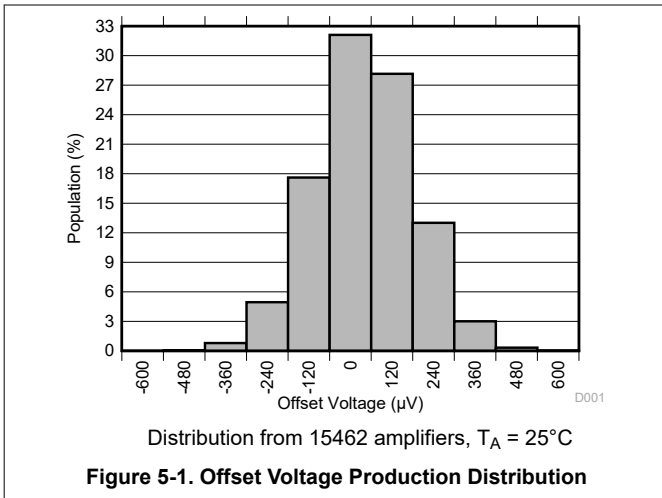| PARAMETER | | TEST CONDITIONS | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|---|
| **OUTPUT** | | | | | | | |
| | Voltage output swing from rail | Positive and negative rail headroom | $V_S$ = 40 V, $R_L$ = no load[3] | | 5 | 10 | mV |
| | | | $V_S$ = 40 V, $R_L$ = 10 kΩ | | 50 | 55 | |
| | | | $V_S$ = 40 V, $R_L$ = 2 kΩ | | 200 | 250 | |
| | | | $V_S$ = 2.7 V, $R_L$ = no load[3] | | 1 | 6 | |
| | | | $V_S$ = 2.7 V, $R_L$ = 10 kΩ | | 5 | 12 | |
| | | | $V_S$ = 2.7 V, $R_L$ = 2 kΩ | | 25 | 40 | |
| $I_{SC}$ | Short-circuit current | | | | ±75 | | mA |
| $C_{LOAD}$ | Capacitive load drive | | | | 1000 | | pF |
| $Z_O$ | Open-loop output impedance | f = 1 MHz, $I_O$ = 0 A | | | 525 | | Ω |
| **POWER SUPPLY** | | | | | | | |
| $I_Q$ | Quiescent current per amplifier | $V_{CM}$ = V–, $I_O$ = 0 A | | | 560 | 685 | µA |
| | | $V_{CM}$ = V–, $I_O$ = 0 A, (OPA991-Q1) | | | 560 | 691 | |
| | | $V_{CM}$ = V–, $I_O$ = 0 A | $T_A$ = –40°C to 125°C | | | 750 | |
| | | $V_{CM}$ = V–, $I_O$ = 0 A, (OPA991-Q1) | | | | 769 | |
| **SHUTDOWN** | | | | | | | |
| $I_{QSD}$ | Quiescent current per amplifier | $V_S$ = 2.7 V to 40 V, all amplifiers disabled, $\overline{SHDN}$ = V– + 2 V | | | 30 | 45 | µA |
| $Z_{SHDN}$ | Output impedance during shutdown | $V_S$ = 2.7 V to 40 V, amplifier disabled, SHDN = V- + 2V | | | 320 ‖ 2 | | MΩ ‖ pF |
| $V_{IH}$ | Logic high threshold voltage (amplifier disabled) | For valid input high, the SHDN pin voltage should be greater than the maximum threshold but less than or equal to (V–) + 20 V | | (V–) + 0.8 | | (V–) + 1.1 | V |
| $V_{IL}$ | Logic low threshold voltage (amplifier enabled) | For valid input low, the SHDN pin voltage should be less than the minimum threshold but greater than or equal to V– | | (V–) + 0.2 | | (V–) + 0.8 | V |
| $t_{ON}$ | Amplifier enable time (full shutdown) [2] | G = +1, $V_{CM}$ = V-, $V_O$ = 0.1 × $V_S$/2 | G = +1, $V_{CM}$ = V-, $V_O$ = 0.1 × $V_S$/2 | | 8 | | µs |
| $t_{OFF}$ | Amplifier disable time [2] | $V_{CM}$ = V-, $V_O$ = $V_S$/2 | | | 3 | | µs |
| | $\overline{SHDN}$ pin input bias current (per pin) | $V_S$ = 2.7 V to 40 V, (V-) +20 V ≥ $\overline{SHDN}$ ≥ (V–) + 0.9 V | | | 500 | | nA |
| | | $V_S$ = 2.7 V to 40 V, (V–) ≤ $\overline{SHDN}$ ≤ (V–) + 0.7 V | | | 150 | | |

(1)  Third-order filter; bandwidth = 80 kHz at –3 dB.
(2)  Disable time ($t_{OFF}$) and enable time ($t_{ON}$) are defined as the time interval between the 50% point of the signal applied to the $\overline{SHDN}$ pin and the point at which the output voltage reaches the 10% (disable) or 90% (enable) level.
(3)  Specified by characterization only.

## 5.8 Typical Characteristics

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)
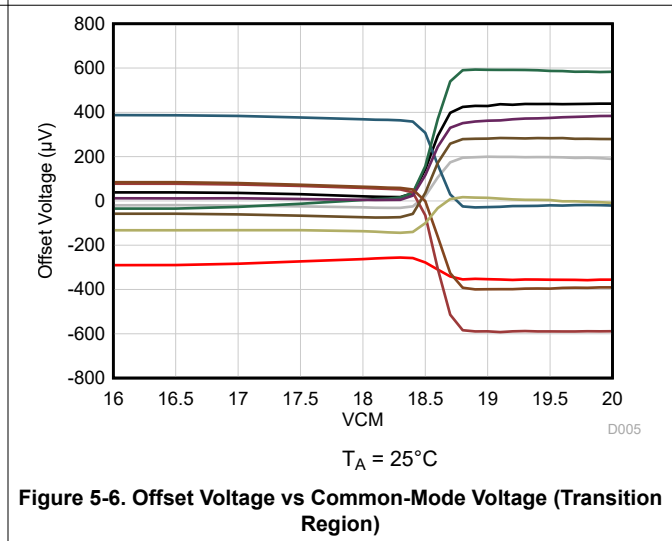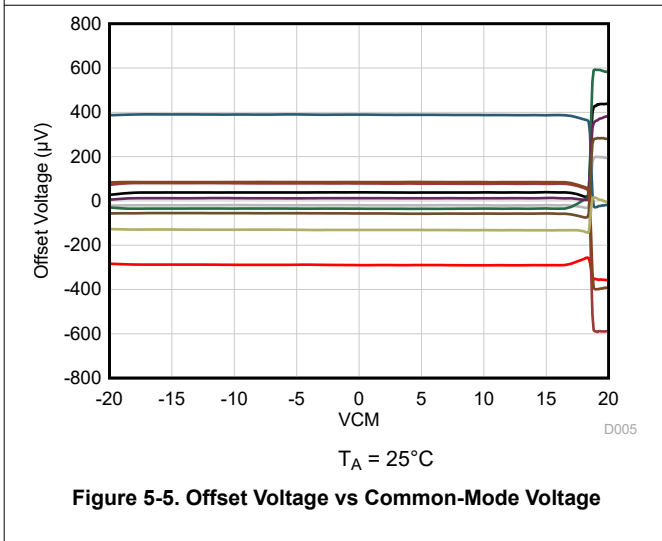


Distribution from 15462 amplifiers, $T_A$ = 25°C

**Figure 5-1. Offset Voltage Production Distribution**



Distribution from 60 amplifiers

**Figure 5-2. Offset Voltage Drift Distribution**



$V_{CM}$ = V+

**Figure 5-3. Offset Voltage vs Temperature**



$V_{CM}$ = V–

**Figure 5-4. Offset Voltage vs Temperature**



$T_A$ = 25°C

**Figure 5-5. Offset Voltage vs Common-Mode Voltage**



$T_A$ = 25°C

**Figure 5-6. Offset Voltage vs Common-Mode Voltage (Transition Region)**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)



$T_A$ = 125°C
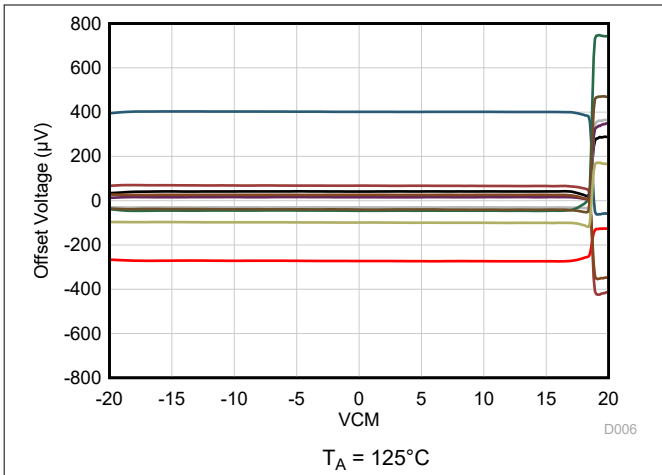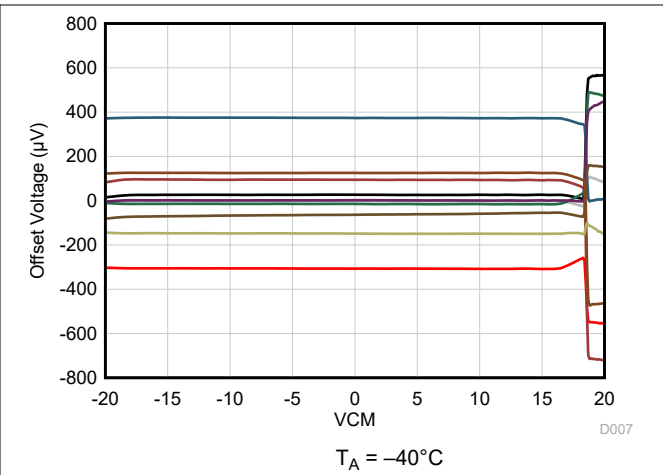
**Figure 5-7. Offset Voltage vs Common-Mode Voltage**



$T_A$ = –40°C

**Figure 5-8. Offset Voltage vs Common-Mode Voltage**
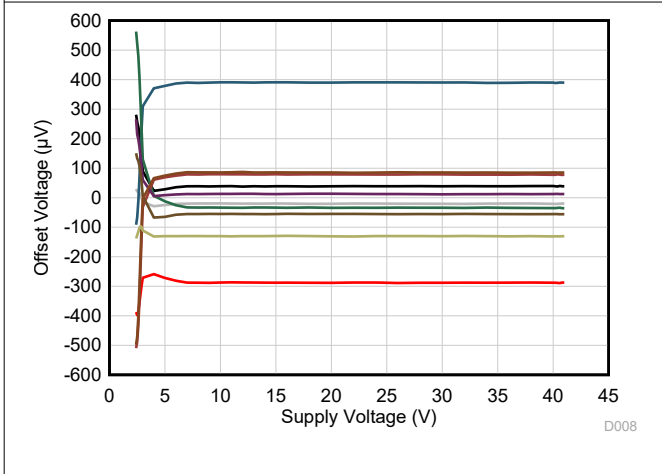


**Figure 5-9. Offset Voltage vs Power Supply**
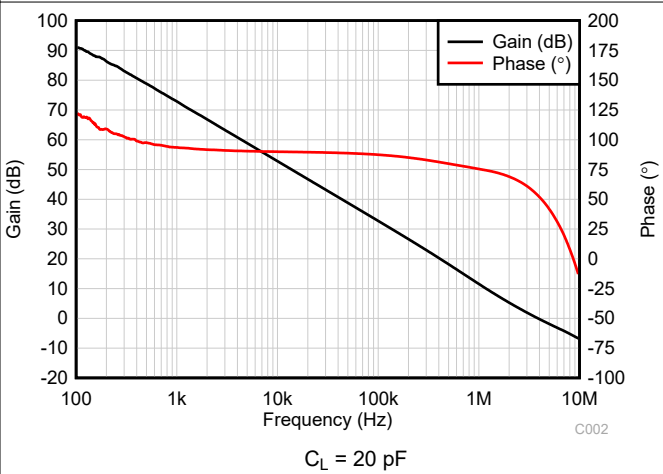


$C_L$ = 20 pF

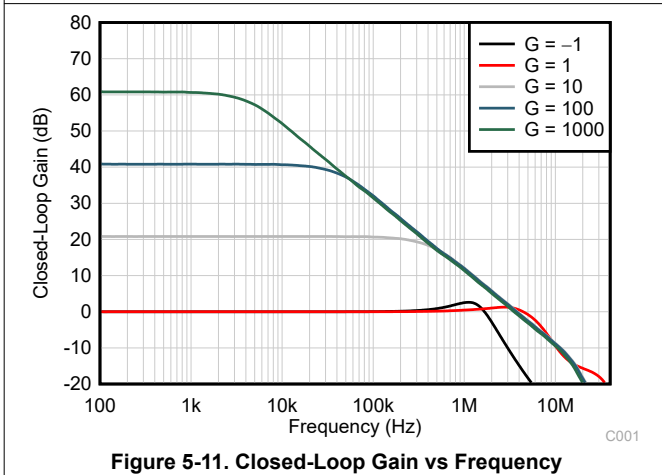**Figure 5-10. Open-Loop Gain and Phase vs Frequency**



**Figure 5-11. Closed-Loop Gain vs Frequency**
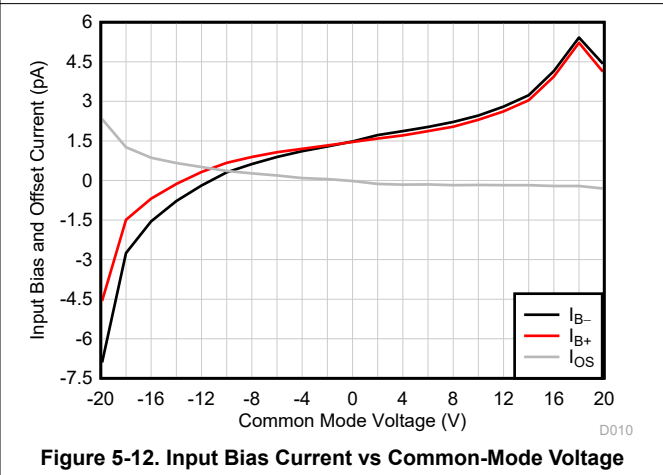


**Figure 5-12. Input Bias Current vs Common-Mode Voltage**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)



**Figure 5-13. Input Bias Current vs Temperature**
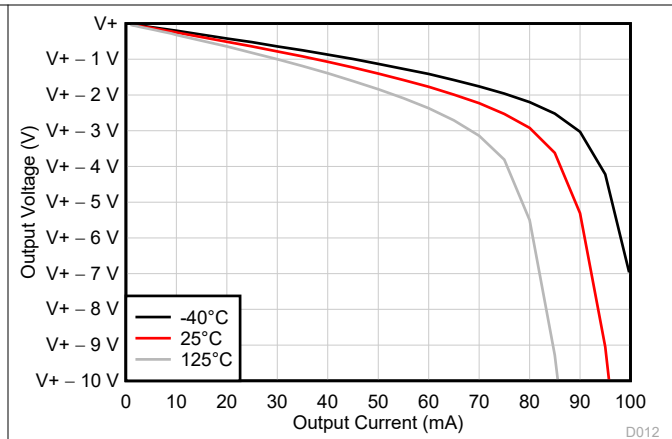


**Figure 5-14. Output Voltage Swing vs Output Current (Sourcing)**
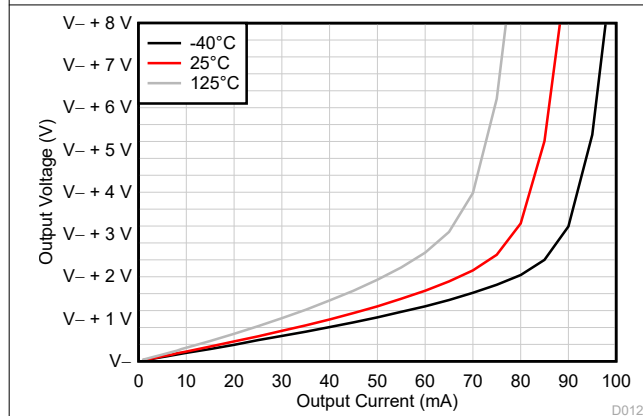


**Figure 5-15. Output Voltage Swing vs Output Current (Sinking)**
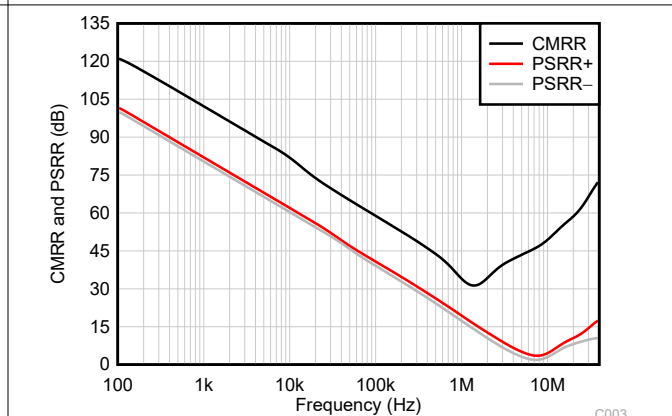


**Figure 5-16. CMRR and PSRR vs Frequency**



f = 0 Hz
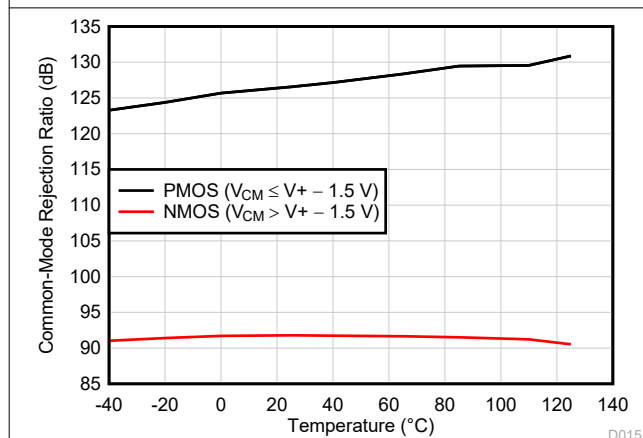
**Figure 5-17. CMRR vs Temperature (dB)**



f = 0 Hz
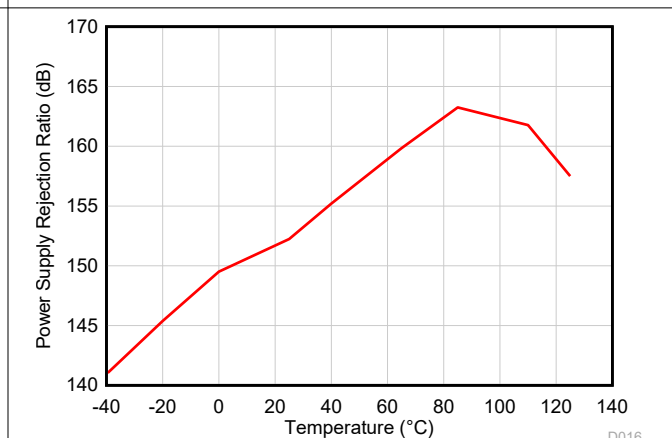
**Figure 5-18. PSRR vs Temperature (dB)**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.8 Typical Characteristics (continued)
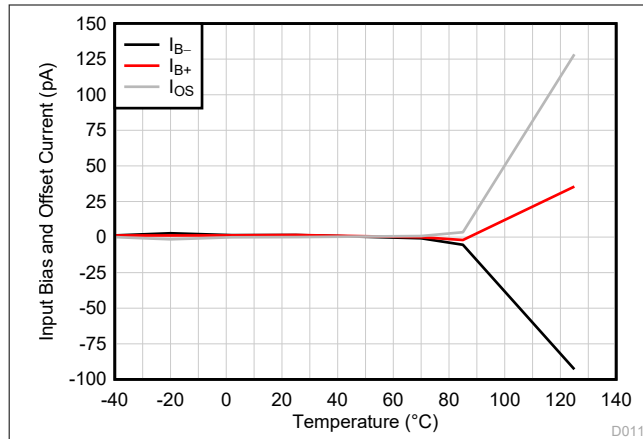
at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)
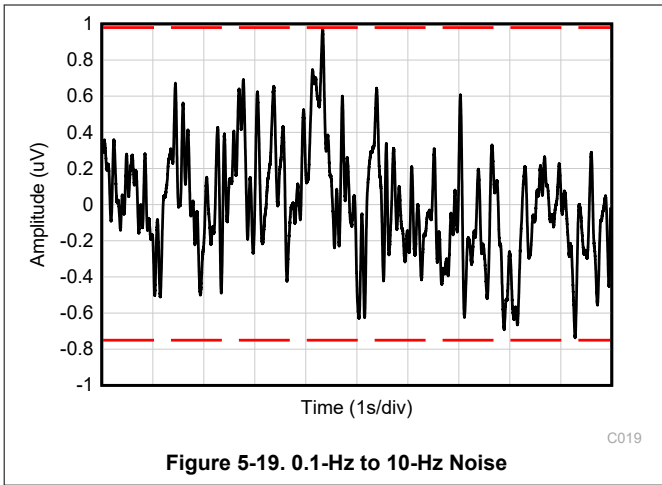


**Figure 5-19. 0.1-Hz to 10-Hz Noise**
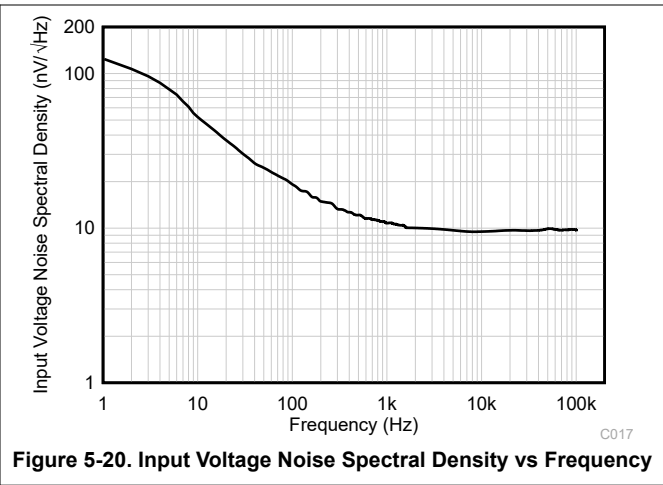


**Figure 5-20. Input Voltage Noise Spectral Density vs Frequency**



BW = 80 kHz, $V_{OUT}$ = 1 $V_{RMS}$
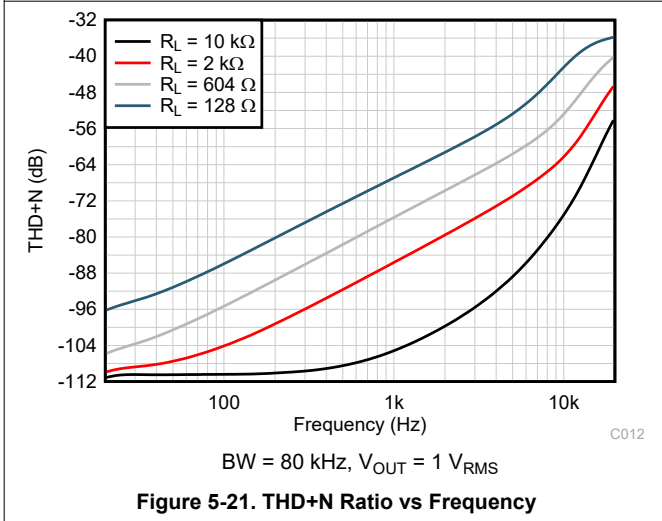
**Figure 5-21. THD+N Ratio vs Frequency**



BW = 80 kHz, f = 1 kHz
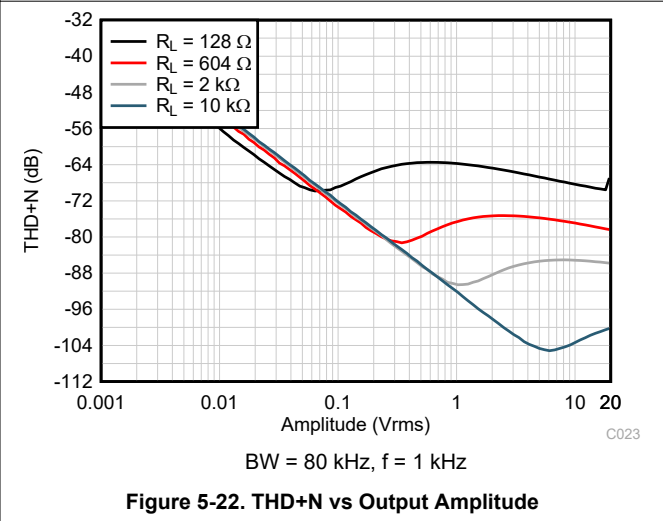
**Figure 5-22. THD+N vs Output Amplitude**
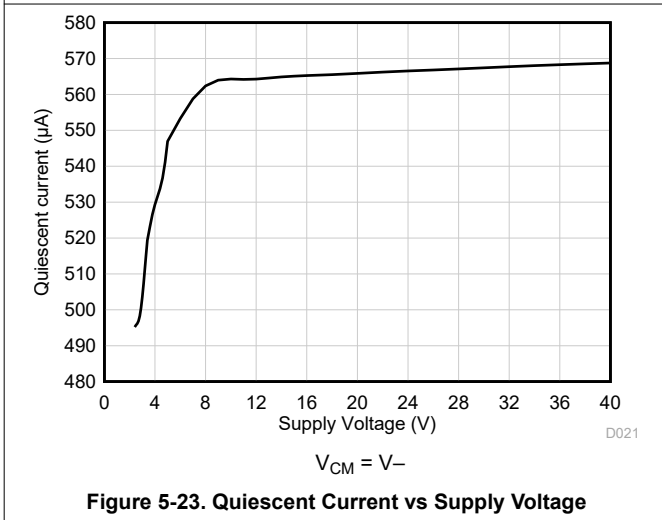


$V_{CM}$ = V−

**Figure 5-23. Quiescent Current vs Supply Voltage**
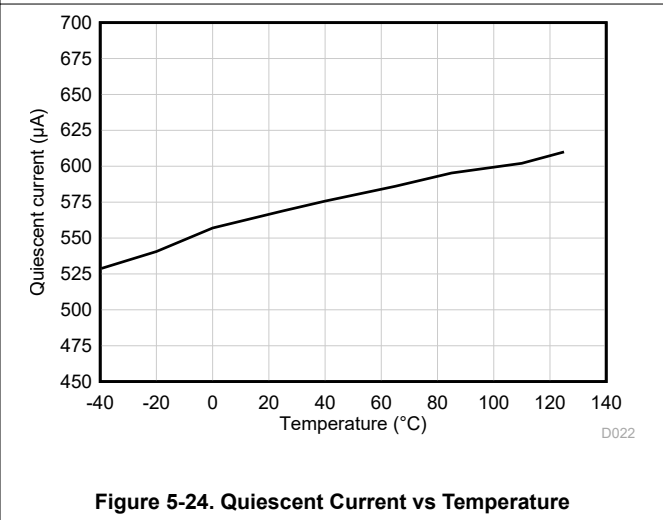


**Figure 5-24. Quiescent Current vs Temperature**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)
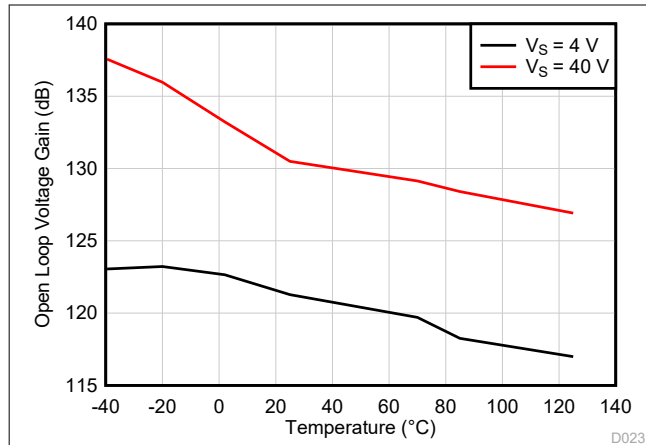


**Figure 5-25. Open-Loop Voltage Gain vs Temperature (dB)**
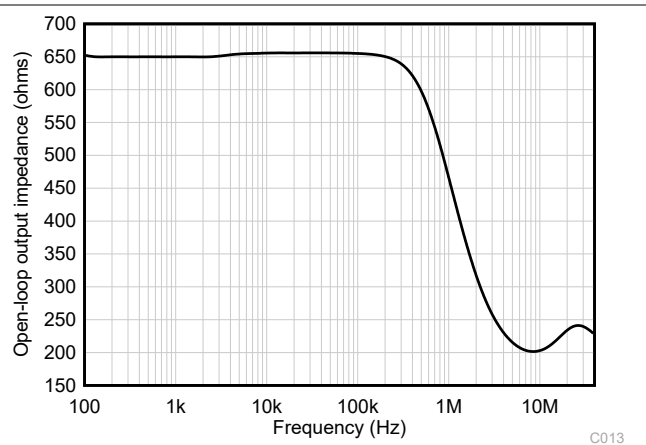


**Figure 5-26. Open-Loop Output Impedance vs Frequency**
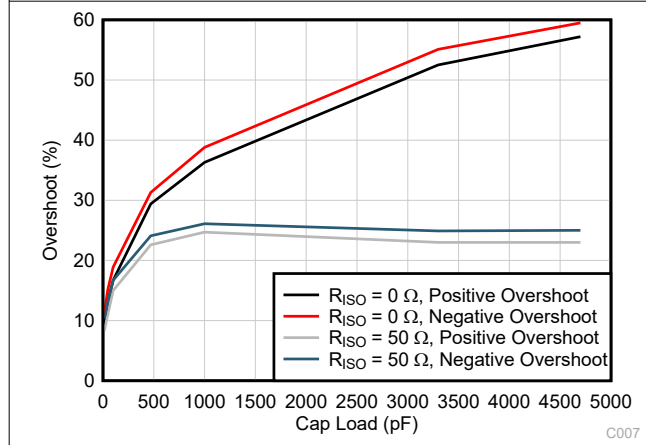


G = –1, 10-mV output step

**Figure 5-27. Small-Signal Overshoot vs Capacitive Load**
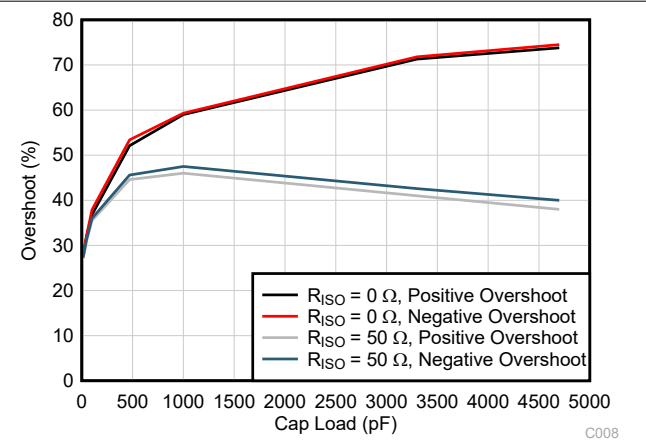


G = 1, 10-mV output step

**Figure 5-28. Small-Signal Overshoot vs Capacitive Load**
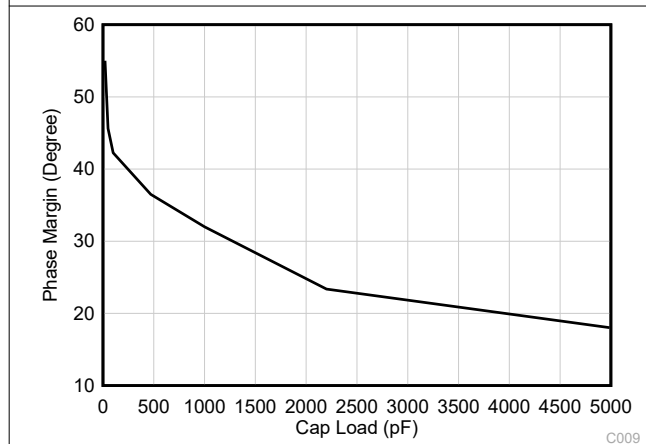


**Figure 5-29. Phase Margin vs Capacitive Load**
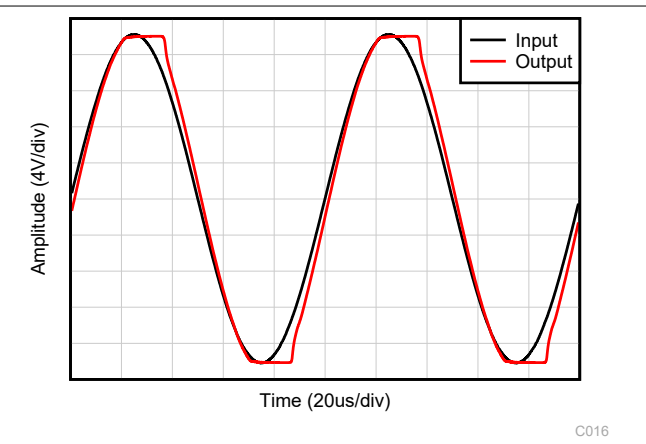


$V_{IN}$ = ±20 V; $V_S$ = $V_{OUT}$ = ±17 V

**Figure 5-30. No Phase Reversal**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 5.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)



G = –10
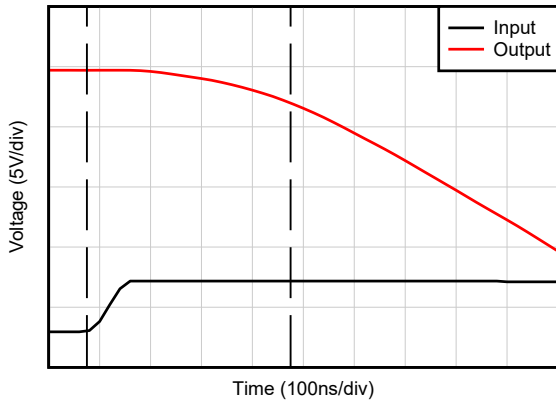
**Figure 5-31. Positive Overload Recovery**



G = –10
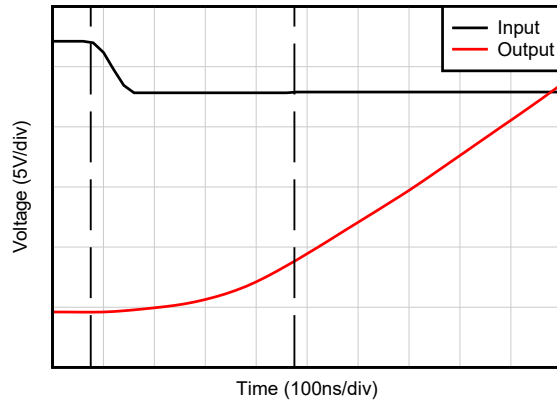
**Figure 5-32. Negative Overload Recovery**
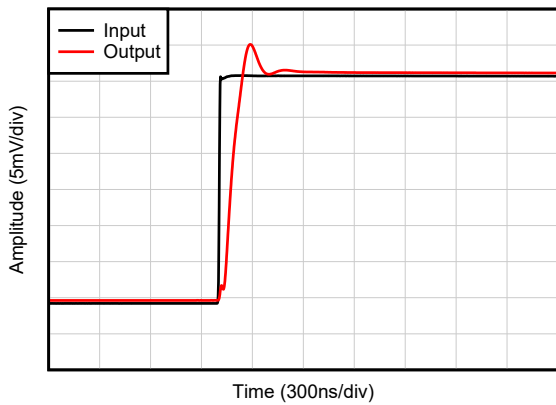


$C_L$ = 20 pF, G = 1, 20-mV step response

**Figure 5-33. Small-Signal Step Response, Rising**
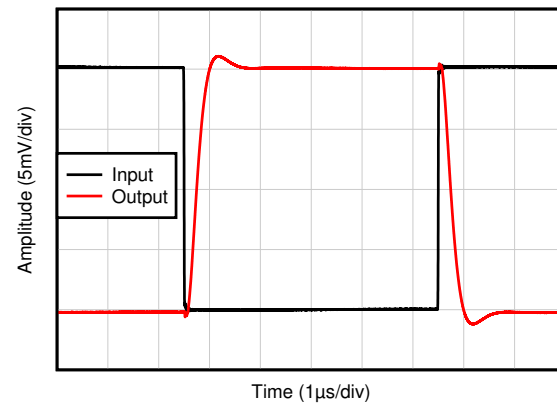


$C_L$ = 20 pF, G = -1, 20-mV step response

**Figure 5-34. Small-Signal Step Response**
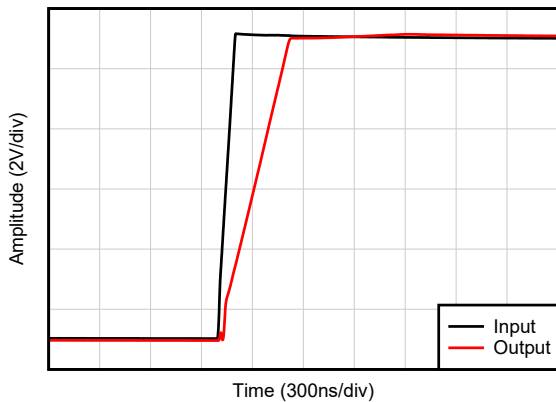


$C_L$ = 20 pF, G = 1

**Figure 5-35. Large-Signal Step Response (Rising)**
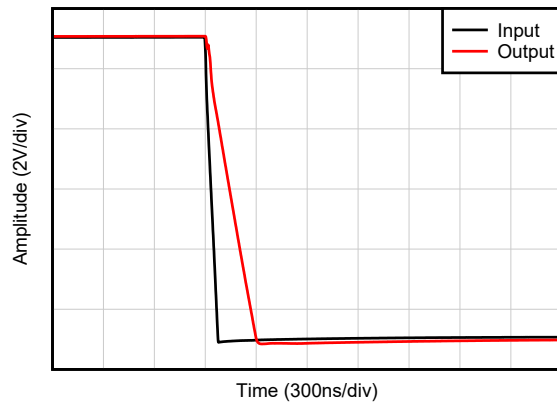


$C_L$ = 20 pF, G = 1

**Figure 5-36. Large-Signal Step Response (Falling)**

## 5.8 Typical Characteristics (continued)

at $T_A$ = 25°C, $V_S$ = ±20 V, $V_{CM}$ = $V_S$ / 2, $R_{LOAD}$ = 10 kΩ connected to $V_S$ / 2, and $C_L$ = 10 pF (unless otherwise noted)



$C_L$ = 20 pF, G = −1

**Figure 5-37. Large-Signal Step Response**



**Figure 5-38. Short-Circuit Current vs Temperature**



**Figure 5-39. Maximum Output Voltage vs Frequency**



**Figure 5-40. Channel Separation vs Frequency**



**Figure 5-41. EMIRR (Electromagnetic Interference Rejection Ratio) at Inputs vs Frequency**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*
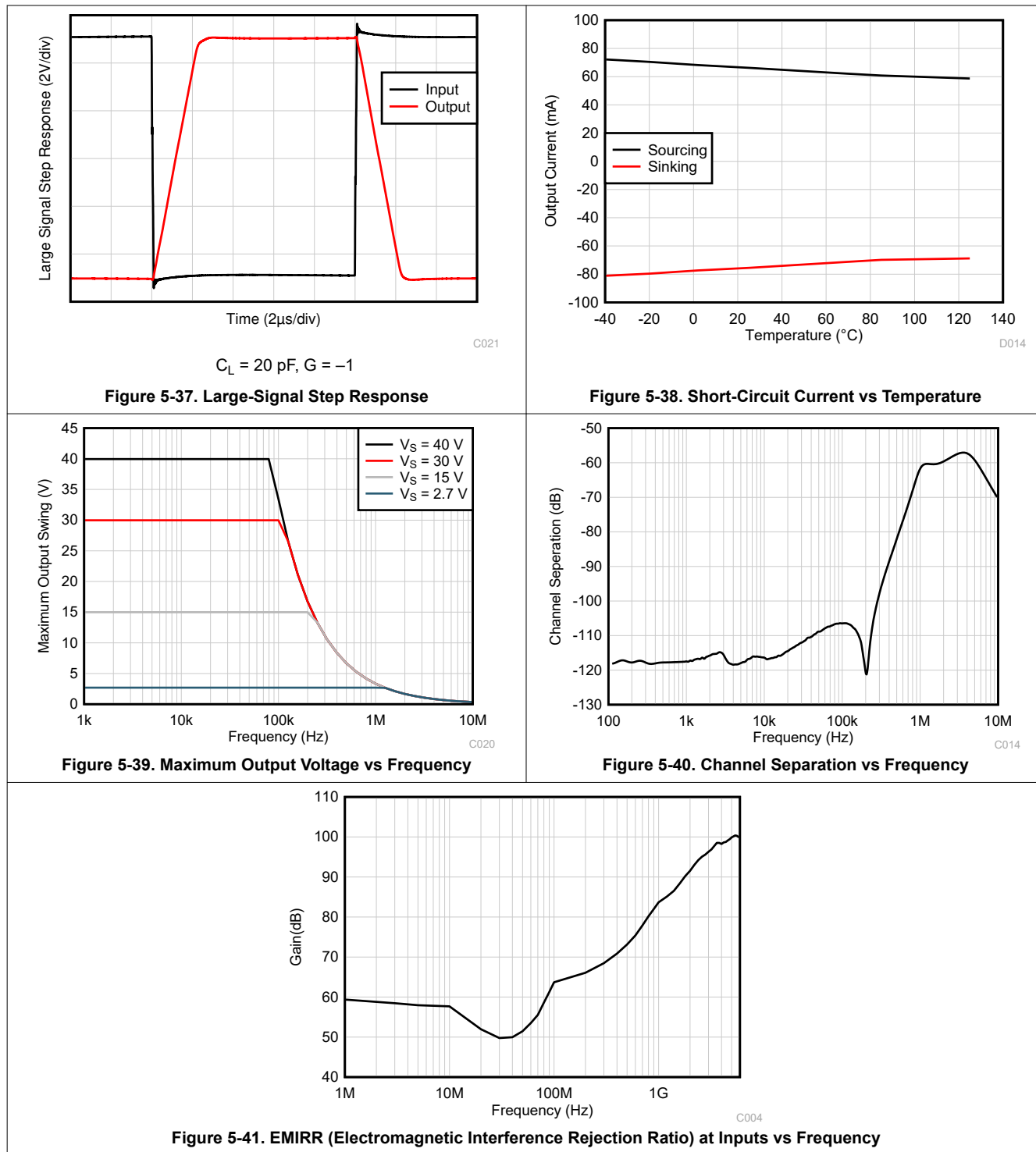
# 6 Detailed Description

## 6.1 Overview

The OPAx991-Q1 family (OPA991-Q1, OPA2991-Q1, and OPA4991-Q1) is a new generation of 40-V general purpose operational amplifiers.

These devices offer excellent DC precision and AC performance, including rail-to-rail input or output, low offset (±125 µV, typical), low offset drift (±0.3 µV/°C, typical), and 4.5-MHz bandwidth.

Unique features such as differential and common-mode input-voltage range to the supply rail, high output current (±75 mA), high slew rate (21 V/µs), and shutdown functionality make the OPAx991-Q1 a robust, high-performance operational amplifier for high-voltage automotive applications.

## 6.2 Functional Block Diagram

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*
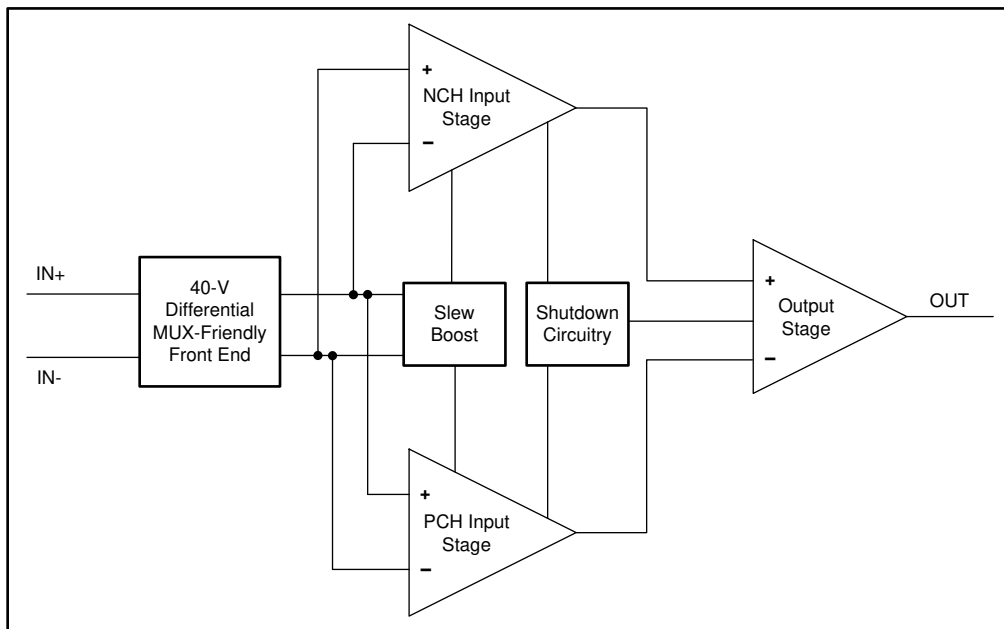
## 6.3 Feature Description

### 6.3.1 Input Protection Circuitry

The OPAx991-Q1 uses a unique input architecture to eliminate the requirement for input protection diodes but still provides robust input protection under transient conditions. Figure 6-1 shows conventional input diode protection schemes that are activated by fast transient step responses and introduce signal distortion and settling time delays because of alternate current paths, as shown in Figure 6-2. For low-gain circuits, these fast-ramping input signals forward-bias back-to-back diodes, causing an increase in input current and resulting in extended settling time.



OPAx991-Q1 Provides Full 40-V Differential Input Range

Conventional Input Protection Limits Differential Input Range
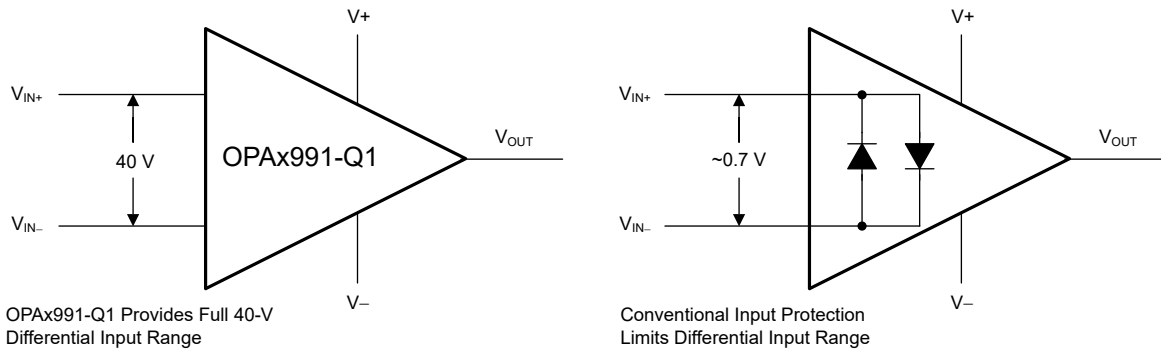
**Figure 6-1. OPAx991-Q1 Input Protection Does Not Limit Differential Input Capability**



*Input Low-Pass Filter*     *Simplified Mux Model*     *Buffer Amplifier*
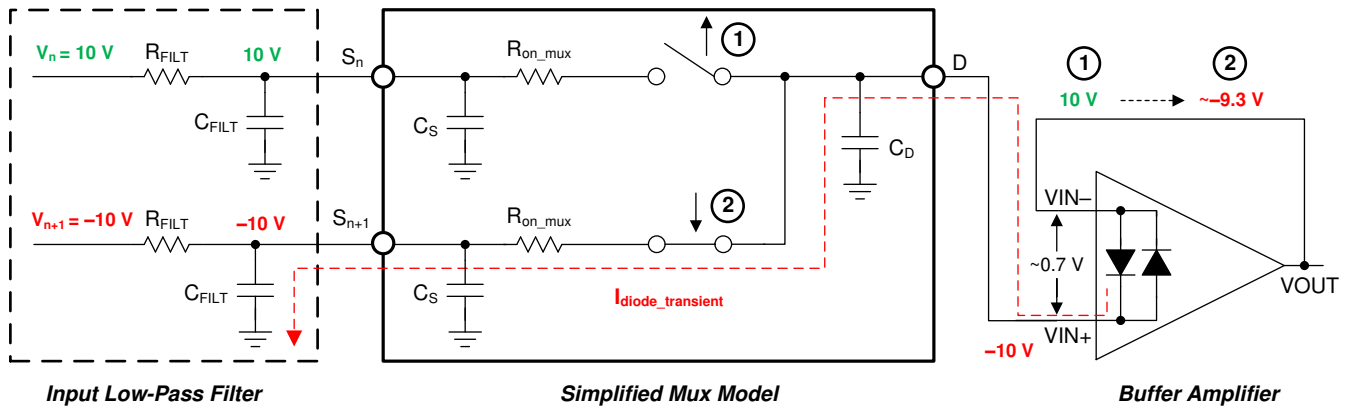
**Figure 6-2. Back-to-Back Diodes Create Settling Issues**

The OPAx991-Q1 family of operational amplifiers provides a true high-impedance differential input capability for high-voltage applications using a patented input protection architecture that does not introduce additional signal distortion or delayed settling time, making the device an optimal op amp for multichannel, high-switched, input applications. The OPAx991-Q1 tolerates a maximum differential swing (voltage between inverting and non-inverting pins of the op amp) of up to 40 V, making the device suitable for use as a comparator or in applications with fast-ramping input signals such as data-acquisition systems; see the TI TechNote *MUX-Friendly Precision Operational Amplifiers* for more information.

### 6.3.2 EMI Rejection

The OPAx991-Q1 uses integrated electromagnetic interference (EMI) filtering to reduce the effects of EMI from sources such as wireless communications and densely-populated boards with a mix of analog signal chain and digital components. EMI immunity can be improved with circuit design techniques; the OPAx991-Q1 benefits from these design improvements. Texas Instruments has developed the ability to accurately measure and quantify the immunity of an operational amplifier over a broad frequency spectrum extending from 10 MHz to 6 GHz. Figure 6-3 shows the results of this testing on the OPAx991-Q1. Table 6-1 lists the EMIRR IN+ values for the OPAx991-Q1 at particular frequencies commonly encountered in real-world applications.

The *EMI Rejection Ratio of Operational Amplifiers* application report contains detailed information on the topic of EMIRR performance as it relates to op amps and is available for download from www.ti.com.
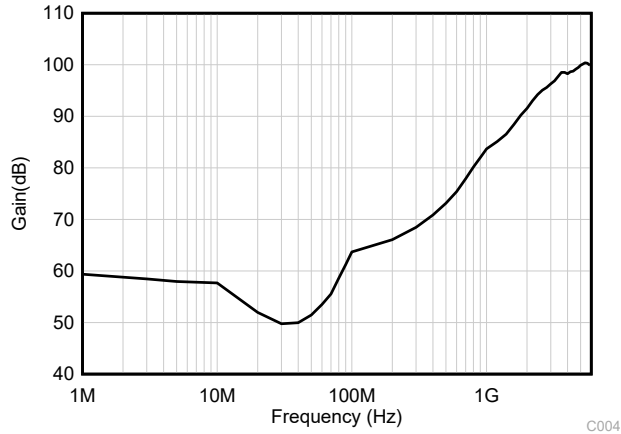


**Figure 6-3. EMIRR Testing**

**Table 6-1. OPAx991-Q1 EMIRR IN+ for Frequencies of Interest**

| FREQUENCY | APPLICATION OR ALLOCATION | EMIRR IN+ |
|---|---|---|
| 400 MHz | Mobile radio, mobile satellite, space operation, weather, radar, ultra-high frequency (UHF) applications | 73.2 dB |
| 900 MHz | Global system for mobile communications (GSM) applications, radio communication, navigation, GPS (to 1.6 GHz), GSM, aeronautical mobile, UHF applications | 82.5 dB |
| 1.8 GHz | GSM applications, mobile personal communications, broadband, satellite, L-band (1 GHz to 2 GHz) | 89.7 dB |
| 2.4 GHz | 802.11b, 802.11g, 802.11n, Bluetooth®, mobile personal communications, industrial, scientific and medical (ISM) radio band, amateur radio and satellite, S-band (2 GHz to 4 GHz) | 93.9 dB |
| 3.6 GHz | Radiolocation, aero communication and navigation, satellite, mobile, S-band | 95.7 dB |
| 5 GHz | 802.11a, 802.11n, aero communication and navigation, mobile communication, space and satellite operation, C-band (4 GHz to 8 GHz) | 98.0 dB |

### 6.3.3 Thermal Protection

The internal power dissipation of any amplifier causes its internal (junction) temperature to rise. This phenomenon is called *self heating*. The absolute maximum junction temperature of the OPAx991-Q1 is 150°C. Exceeding this temperature causes damage to the device. The OPAx991-Q1 has a thermal protection feature that reduces damage from self heating. The protection works by monitoring the temperature of the device and turning off the op amp output drive for temperatures above 170°C. Figure 6-4 shows an application example for the OPAx991-Q1 that has significant self heating because of its power dissipation (0.81 W). Thermal calculations indicate that for an ambient temperature of 65°C, the device junction temperature will reach 177°C. The actual device, however, turns off the output drive to recover towards a safe junction temperature. Figure 6-4 shows how the circuit behaves during thermal protection. During normal operation, the device acts as a buffer so the output is 3 V. When self heating causes the device junction temperature to increase above the internal limit, the thermal protection forces the output to a high-impedance state and the output is pulled to ground through resistor $R_L$. If the condition that caused excessive power dissipation is not removed, the amplifier will oscillate between a shutdown and enabled state until the output fault is corrected.
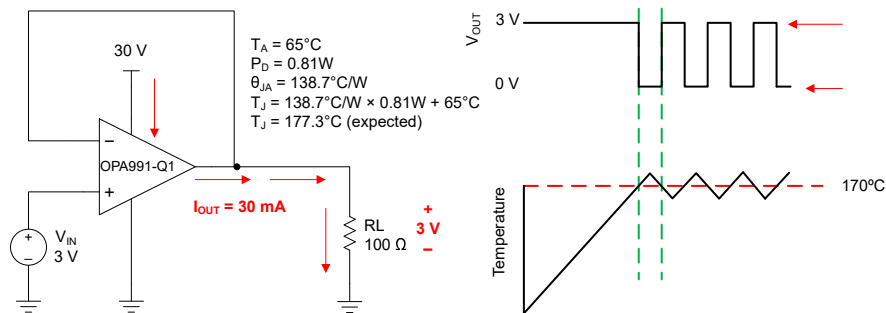


**Figure 6-4. Thermal Protection**

If the device continues to operate at high junction temperatures with high output power over a long period of time, regardless if the device is or is not entering thermal shutdown, the thermal dissipation of the device can slowly degrade performance of the device and eventually cause catastrophic destruction. Designers should be careful to limit output power of the device at high temperatures, or control ambient and junction temperatures under high output power conditions.

### 6.3.4 Capacitive Load and Stability

The OPAx991-Q1 features a resistive output stage capable of driving moderate capacitive loads, and by leveraging an isolation resistor, the device can easily be configured to drive large capacitive loads. Increasing the gain enhances the ability of the amplifier to drive greater capacitive loads; see Figure 6-5 and Figure 6-6. The particular op amp circuit configuration, layout, gain, and output loading are some of the factors to consider when establishing whether an amplifier will be stable in operation.

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

**Figure 6-5. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = 1)**



**Figure 6-6. Small-Signal Overshoot vs Capacitive Load (10-mV Output Step, G = –1)**
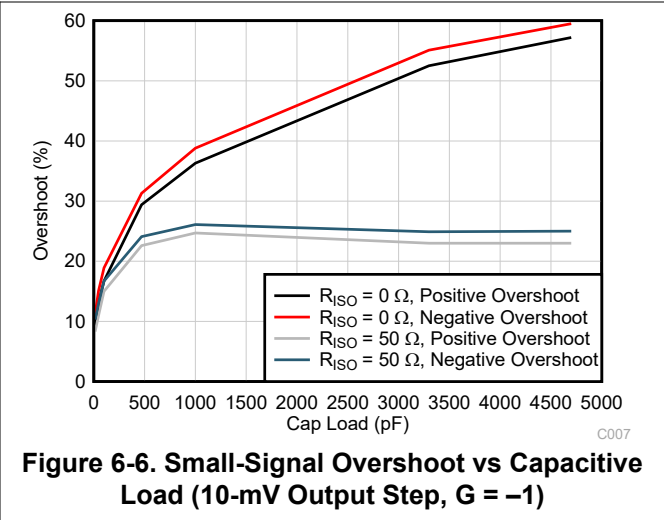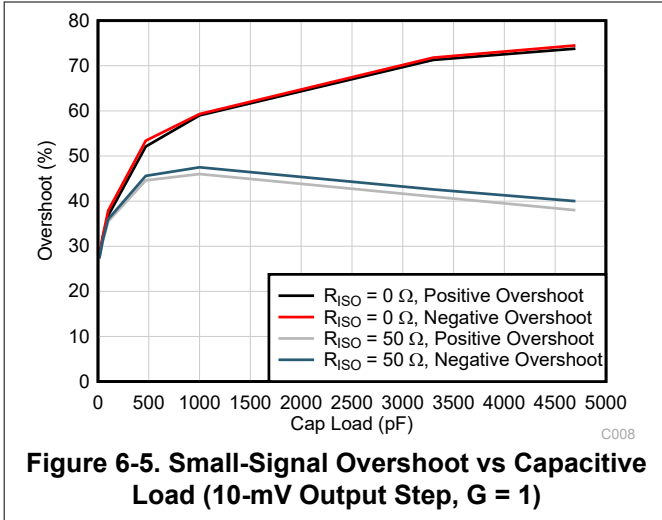
For additional drive capability in unity-gain configurations, improve capacitive load drive by inserting a small resistor, $R_{ISO}$, in series with the output, as shown in Figure 6-7. This resistor significantly reduces ringing and maintains DC performance for purely capacitive loads. However, if a resistive load is in parallel with the capacitive load, then a voltage divider is created, thus introducing a gain error at the output and slightly reducing the output swing. The error introduced is proportional to the ratio $R_{ISO}$ / $R_L$, and is generally negligible at low output levels. A high capacitive load drive makes the OPAx991-Q1 well suited for applications such as reference buffers, MOSFET gate drives, and cable-shield drives. The circuit shown in Figure 6-7 uses an isolation resistor, $R_{ISO}$, to stabilize the output of an op amp. $R_{ISO}$ modifies the open-loop gain of the system for increased phase margin.
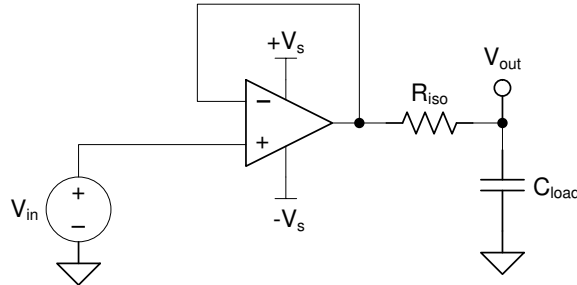


**Figure 6-7. Extending Capacitive Load Drive With the OPAx991-Q1**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

### 6.3.5 Common-Mode Voltage Range

The OPAx991-Q1 is a 40-V, true rail-to-rail input operational amplifier with an input common-mode range that extends 100 mV beyond either supply rail. This wide range is achieved with paralleled complementary N-channel and P-channel differential input pairs, as shown in Figure 6-8. The N-channel pair is active for input voltages close to the positive rail, typically (V+) – 1 V to 100 mV above the positive supply. The P-channel pair is active for inputs from 100 mV below the negative supply to approximately (V+) – 2 V. There is a small transition region, typically (V+) – 2 V to (V+) – 1 V in which both input pairs are on. This transition region can vary modestly with process variation, and within this region PSRR, CMRR, offset voltage, offset drift, noise, and THD performance may be degraded compared to operation outside this region.

Figure 5-5 shows this transition region for a typical device in terms of input voltage offset in more detail.

For more information on common-mode voltage range and PMOS/NMOS pair interaction, see *Op Amps With Complementary-Pair Input Stages* application note.
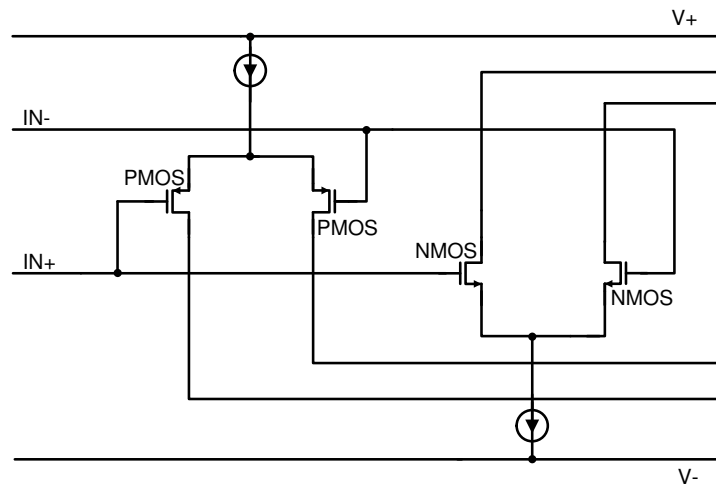


**Figure 6-8. Rail-to-Rail Input Stage**

### 6.3.6 Phase Reversal Protection

The OPAx991-Q1 family has internal phase-reversal protection. Many op amps exhibit phase reversal when the input is driven beyond its linear common-mode range. This condition is most often encountered in non-inverting circuits when the input is driven beyond the specified common-mode voltage range, causing the output to reverse into the opposite rail. The OPAx991-Q1 is a rail-to-rail input op amp; therefore, the common-mode range can extend beyond the rails. Input signals beyond the rails do not cause phase reversal; instead, the output limits into the appropriate rail. This performance is shown in Figure 6-9. For more information on phase reversal, see *Op Amps With Complementary-Pair Input Stages* application note.

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*
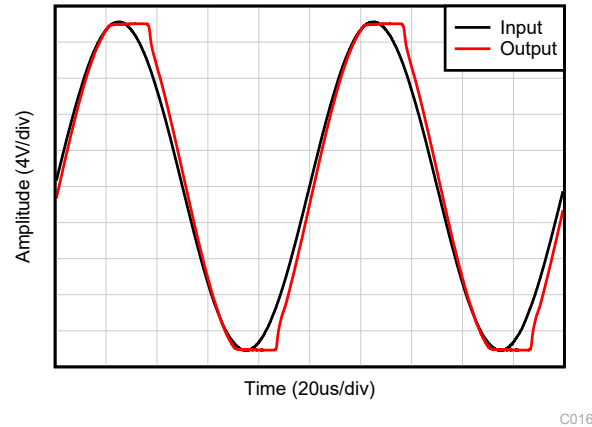
**Figure 6-9. No Phase Reversal**

### 6.3.7 Electrical Overstress

Designers often ask questions about the capability of an operational amplifier to withstand electrical overstress (EOS). These questions tend to focus on the device inputs, but may involve the supply voltage pins or even the output pin. Each of these different pin functions have electrical stress limits determined by the voltage breakdown characteristics of the particular semiconductor fabrication process and specific circuits connected to the pin. Additionally, internal electrostatic discharge (ESD) protection is built into these circuits to protect them from accidental ESD events both before and during product assembly.

Having a good understanding of this basic ESD circuitry and its relevance to an electrical overstress event is helpful. Figure 6-10 shows an illustration of the ESD circuits contained in the OPAx991-Q1 (indicated by the dashed line area). The ESD protection circuitry involves several current-steering diodes connected from the input and output pins and routed back to the internal power-supply lines, where the diodes meet at an absorption device or the power-supply ESD cell, internal to the operational amplifier. This protection circuitry is intended to remain inactive during normal circuit operation.
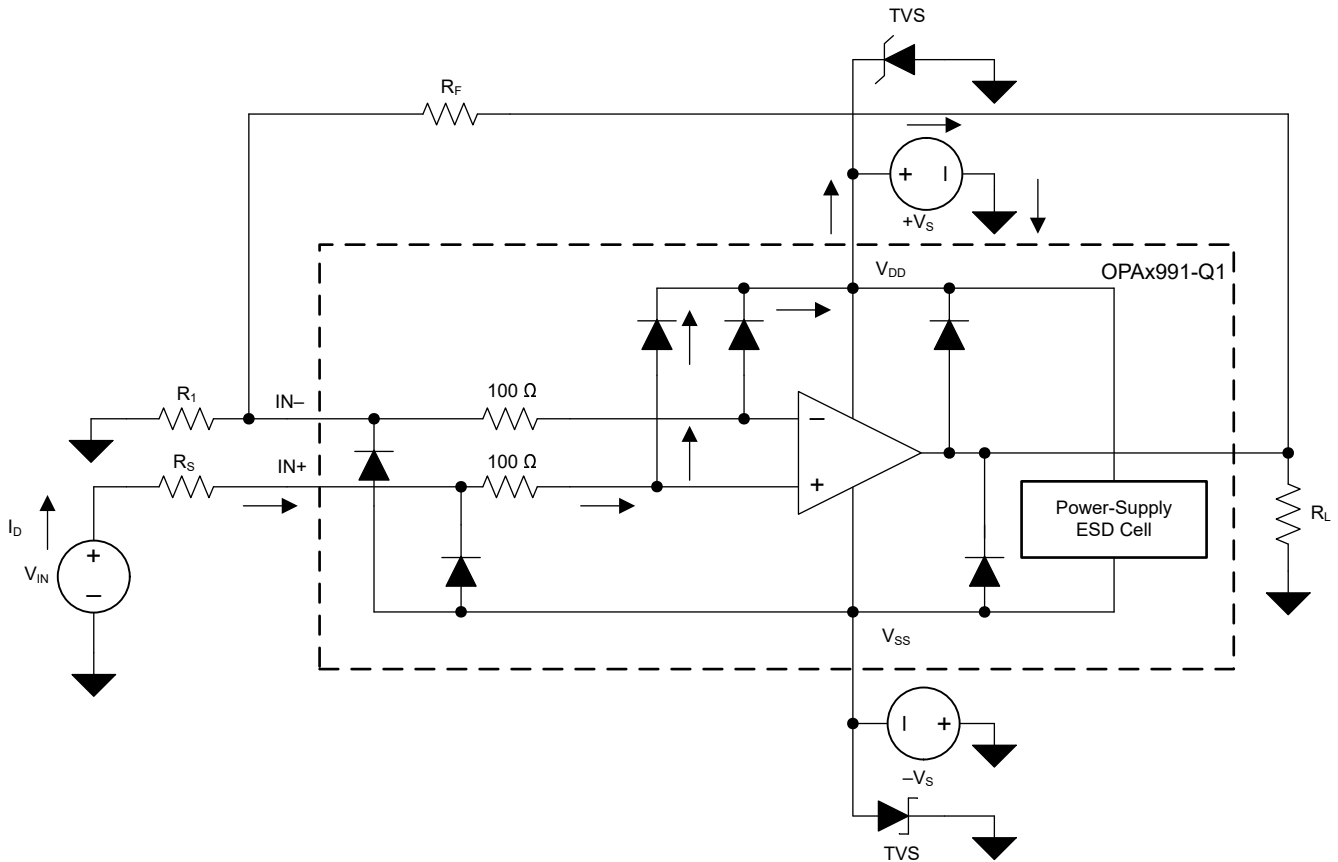
**Figure 6-10. Equivalent Internal ESD Circuitry Relative to a Typical Circuit Application**

An ESD event is very short in duration and very high voltage (for example; 1 kV, 100 ns), whereas an EOS event is long duration and lower voltage (for example; 50 V, 100 ms). The ESD diodes are designed for out-of-circuit ESD protection (that is, during assembly, test, and storage of the device before being soldered to the PCB). During an ESD event, the ESD signal is passed through the ESD steering diodes to an absorption circuit (labeled ESD power-supply circuit). The ESD absorption circuit clamps the supplies to a safe level.

Although this behavior is necessary for out-of-circuit protection, excessive current and damage is caused if activated in-circuit. A transient voltage suppressors (TVS) can be used to prevent against damage caused by turning on the ESD absorption circuit during an in-circuit ESD event. Using the appropriate current limiting resistors and TVS diodes allows for the use of device ESD diodes to protect against EOS events.

### 6.3.8 Overload Recovery

Overload recovery is defined as the time required for the op amp output to recover from a saturated state to a linear state. The output devices of the op amp enter a saturation region when the output voltage exceeds the rated operating voltage, either due to the high input voltage or the high gain. After the device enters the saturation region, the charge carriers in the output devices require time to return back to the linear state. After the charge carriers return back to the linear state, the device begins to slew at the specified slew rate. Thus, the propagation delay in case of an overload condition is the sum of the overload recovery time and the slew time. The overload recovery time for the OPAx991-Q1 is approximately 400 ns.

### 6.3.9 Typical Specifications and Distributions

Designers often have questions about a typical specification of an amplifier to design a more robust circuit. Due to natural variation in process technology and manufacturing procedures, every specification of an amplifier will exhibit some amount of deviation from the ideal value, like an amplifier's input offset voltage. These deviations often follow *Gaussian* (*bell curve*), or *normal* distributions, and circuit designers can leverage this information to guard band their system, even when there is not a minimum or maximum specification in the *Electrical Characteristics* table.
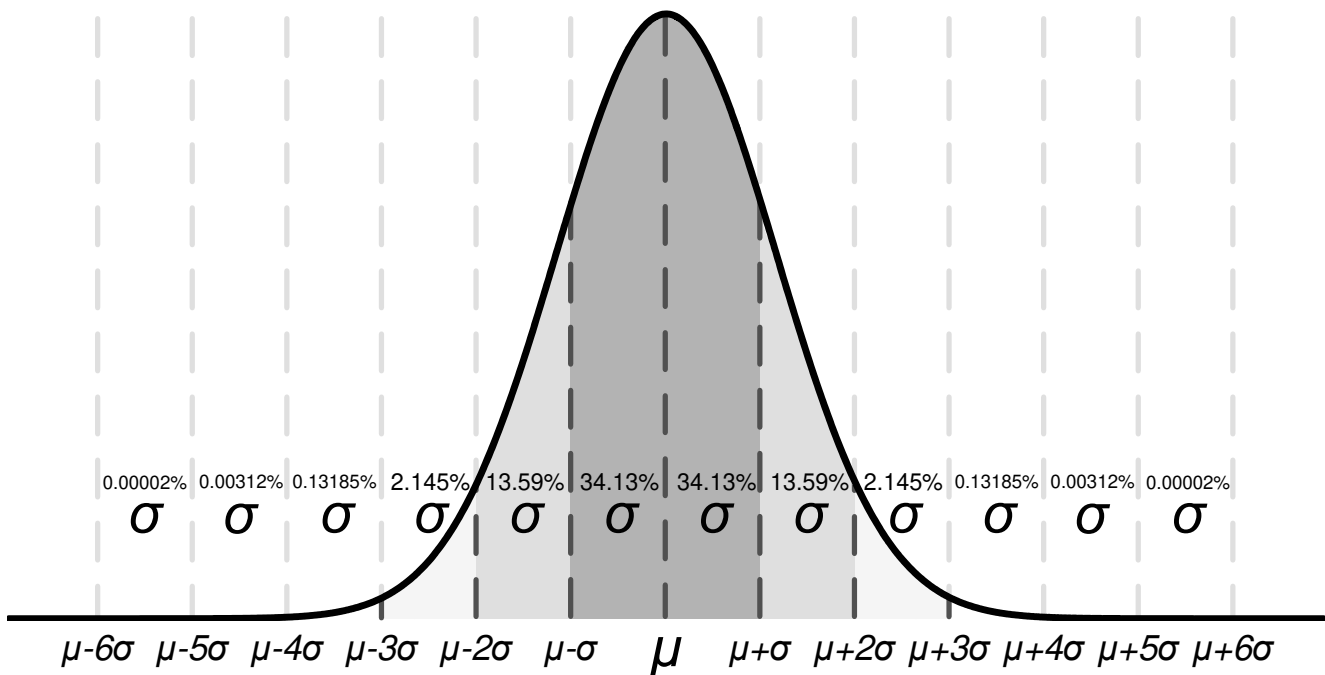


**Figure 6-11. Ideal Gaussian Distribution**

Figure 6-11 shows an example distribution, where $\mu$, or *mu*, is the mean of the distribution, and where $\sigma$, or *sigma*, is the standard deviation of a system. For a specification that exhibits this kind of distribution, approximately two-thirds (68.26%) of all units can be expected to have a value within one standard deviation, or one sigma, of the mean (from $\mu - \sigma$ to $\mu + \sigma$).

Depending on the specification, values listed in the *typical* column of the *Electrical Characteristics* table are represented in different ways. As a general rule, if a specification naturally has a nonzero mean (for example, like gain bandwidth), then the typical value is equal to the mean ($\mu$). However, if a specification naturally has a mean near zero (like input offset voltage), then the typical value is equal to the mean plus one standard deviation ($\mu + \sigma$) to most accurately represent the typical value.

This chart can be used to calculate the approximate probability of a specification in a unit; for example, for OPAx991-Q1, the typical input voltage offset is 125 µV, so 68.2% of all OPAx991-Q1 devices are expected to have an offset from –125 µV to 125 µV. At 4 $\sigma$ (±500 µV), 99.9937% of the distribution has an offset voltage less than ±500 µV, which means 0.0063% of the population is outside of these limits, which corresponds to about 1 in 15,873 units.

Specifications with a value in the minimum or maximum column are assured by TI, and units outside these limits will be removed from production material. For example, the OPAx991-Q1 family has a maximum offset voltage of 895 µV at 25°C, and even though this corresponds to more than 5 σ (≈1 in 1.7 million units), which is extremely unlikely, TI assures that any unit with larger offset than 895 µV will be removed from production material.

For specifications with no value in the minimum or maximum column, consider selecting a sigma value of sufficient guard band for the application, and design worst-case conditions using this value. For example, the 6-σ value corresponds to about 1 in 500 million units, which is an extremely unlikely chance, and could be an option as a wide guard band to design a system around. In this case, the OPAx991-Q1 family does not have a maximum or minimum for offset voltage drift, but based on Figure 5-2 and the typical value of 0.3 µV/°C in the *Electrical Characteristics* table, it can be calculated that the 6-σ value for offset voltage drift is about 1.8 µV/°C. When designing for worst-case system conditions, this value can be used to estimate the worst possible offset across temperature without having an actual minimum or maximum value.

However, process variation and adjustments over time can shift typical means and standard deviations, and unless there is a value in the minimum or maximum specification column, TI cannot assure the performance of a device. This information should be used only to estimate the performance of a device.

### 6.3.10 Shutdown

The OPAx991S-Q1 devices feature one or more shutdown pins (SHDN) that disable the op amp, placing it into a low-power standby mode. In this mode, the op amp typically consumes about 30 µA. The SHDN pins are active high, meaning that shutdown mode is enabled when the input to the SHDN pin is a valid logic high. The amplifier is enabled when the input to the SHDN pin is a valid logic low.

The SHDN pins are referenced to the negative supply rail of the op amp. The threshold of the shutdown feature lies around 800 mV (typical) and does not change with respect to the supply voltage. Hysteresis has been included in the switching threshold for smooth switching characteristics. For optimal shutdown behavior, the SHDN pins should be driven with valid logic signals. A valid logic low is defined as a voltage between V– and V– + 0.2 V. A valid logic high is defined as a voltage between V– + 1.1 V and V– + 20 V or V+, whichever is lower. The shutdown pin circuitry includes a pull-down resistor, which will inherently pull the voltage of the pin to the negative supply rail if not driven. Thus, to enable the amplifier, the SHDN pins should either be left floating or driven to a valid logic low. To disable the amplifier, the SHDN pins must be driven to a valid logic high. The maximum voltage allowed at the SHDN pins is V– + 20 V. Exceeding V– + 20 V or V+, whichever is lower, will damage the device.

The SHDN pins are high-impedance CMOS inputs. Channels of single and dual op amp packages are independently controlled, and channels of quad op amp packages are controlled in pairs. For battery-operated applications, this feature may be used to greatly reduce the average current and extend battery life. The typical enable time out of shutdown is 8 µs; disable time is 3 µs. When disabled, the output assumes a high-impedance state. This architecture allows the OPAx991S-Q1 family to operate as a gated amplifier, multiplexer, or programmable-gain amplifier. Shutdown time ($t_{OFF}$) depends on loading conditions and increases as load resistance increases. For shutdown (disable) within a specific shutdown time, the specified 10-kΩ load to midsupply ($V_S$ / 2) is required. If using the OPAx991S-Q1 without a load, the resulting turnoff time significantly increases.

### 6.4 Device Functional Modes

The OPAx991-Q1 has a single functional mode and is operational when the power-supply voltage is greater than 2.7 V (±1.35 V). The maximum power supply voltage for the OPAx991-Q1 is 40 V (±20 V).

The OPAx991S-Q1 devices feature a shutdown pin, which can be used to place the op amp into a low-power mode. See *Shutdown* section for more information.

# 7 Application and Implementation

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**Note**

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes, as well as validating and testing their design implementation to confirm system functionality.

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## 7.1 Application Information

The OPAx991-Q1 family offers excellent DC precision and AC performance. These devices operate up to 40-V supply rails and offer true rail-to-rail input/output, low offset voltage and offset voltage drift, as well as 4.5-MHz bandwidth and high output drive. These features make the OPAx991-Q1 a robust, high-performance operational amplifier for high-voltage industrial applications.

## 7.2 Typical Applications

### 7.2.1 Low-Side Current Measurement

Figure 7-1 shows the OPAx991-Q1 configured in a low-side current sensing application. For a full analysis of the circuit shown in Figure 7-1 including theory, calculations, simulations, and measured data, see TI Precision Design TIPD129, *0-A to 1-A Single-Supply Low-Side Current-Sensing Solution*.
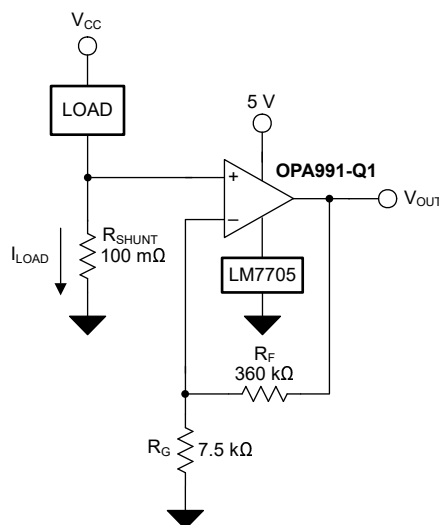


**Figure 7-1. OPAx991-Q1 in a Low-Side, Current-Sensing Application**

#### 7.2.1.1 Design Requirements

The design requirements for this design are:

- Load current: 0 A to 1 A
- Output voltage: 4.9 V
- Maximum shunt voltage: 100 mV

### 7.2.1.2 Detailed Design Procedure

The transfer function of the circuit in Figure 7-1 is given in Equation 1.

$$V_{OUT} = I_{LOAD} \times R_{SHUNT} \times Gain \tag{1}$$

The load current ($I_{LOAD}$) produces a voltage drop across the shunt resistor ($R_{SHUNT}$). The load current is set from 0 A to 1 A. To keep the shunt voltage below 100 mV at maximum load current, the largest shunt resistor is defined using Equation 2.

$$R_{SHUNT} = \frac{V_{SHUNT\_MAX}}{I_{LOAD\_MAX}} = \frac{100\,mV}{1\,A} = 100\,m\Omega \tag{2}$$

Using Equation 2, $R_{SHUNT}$ is calculated to be 100 mΩ. The voltage drop produced by $I_{LOAD}$ and $R_{SHUNT}$ is amplified by the OPA991-Q1 to produce an output voltage of 0 V to 4.9 V. The gain needed by the OPA991-Q1 to produce the necessary output voltage is calculated using Equation 3.

$$Gain = \frac{(V_{OUT\_MAX} - V_{OUT\_MIN})}{(V_{IN\_MAX} - V_{IN\_MIN})} \tag{3}$$

Using Equation 3, the required gain is calculated to be 49 V/V, which is set with resistors $R_F$ and $R_G$. Equation 4 is used to size the resistors, $R_F$ and $R_G$, to set the gain of the OPA991-Q1 to 49 V/V.

$$Gain = 1 + \frac{(R_F)}{(R_G)} \tag{4}$$

Choosing $R_F$ as 360 kΩ, $R_G$ is calculated to be 7.5 kΩ. $R_F$ and $R_G$ were chosen as 360 kΩ and 7.5 kΩ because they are standard value resistors that create a 49:1 ratio. Other resistors that create a 49:1 ratio can also be used. Figure 7-2 shows the measured transfer function of the circuit shown in Figure 7-1.

### 7.2.1.3 Application Curve
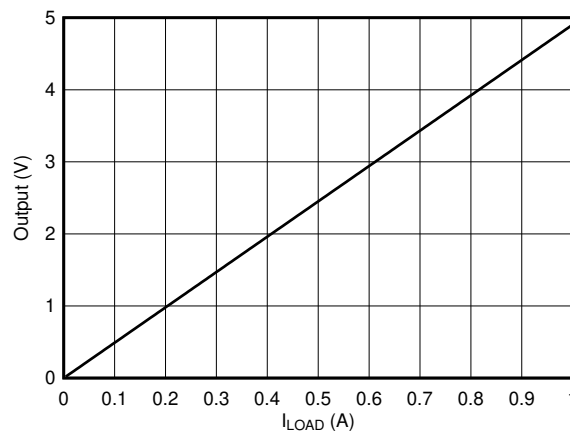


**Figure 7-2. Low-Side, Current-Sense, Transfer Function**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*

## 7.3 Power Supply Recommendations

The OPAx991-Q1 is specified for operation from 2.7 V to 40 V (±1.35 V to ±40 V); many specifications apply from –40°C to 125°C. Parameters that can exhibit significant variance with regard to operating voltage or temperature are presented in *Typical Characteristics*.

<div style="border:1px solid black; padding:10px;">

**CAUTION**

Supply voltages larger than 40 V can permanently damage the device; see the *Absolute Maximum Ratings*.

</div>

Place 0.1-µF bypass capacitors close to the power-supply pins to reduce errors coupling in from noisy or high-impedance power supplies. For more detailed information on bypass capacitor placement, refer to *Layout*.

## 7.4 Layout

### 7.4.1 Layout Guidelines

For best operational performance of the device, use good PCB layout practices, including:

- Noise can propagate into analog circuitry through the power pins of the circuit as a whole and op amp itself. Bypass capacitors are used to reduce the coupled noise by providing low-impedance power sources local to the analog circuitry.
  - Connect low-ESR, 0.1-µF ceramic bypass capacitors between each supply pin and ground, placed as close to the device as possible. A single bypass capacitor from V+ to ground is applicable for single-supply applications.
- Separate grounding for analog and digital portions of circuitry is one of the simplest and most-effective methods of noise suppression. One or more layers on multilayer PCBs are usually devoted to ground planes. A ground plane helps distribute heat and reduces EMI noise pickup. Make sure to physically separate digital and analog grounds paying attention to the flow of the ground current.
- To reduce parasitic coupling, run the input traces as far away from the supply or output traces as possible. If these traces cannot be kept separate, crossing the sensitive trace perpendicular is much better as opposed to in parallel with the noisy trace.
- Place the external components as close to the device as possible. As shown in Figure 7-4, keeping RF and RG close to the inverting input minimizes parasitic capacitance.
- Keep the length of input traces as short as possible. Always remember that the input traces are the most sensitive part of the circuit.
- Consider a driven, low-impedance guard ring around the critical traces. A guard ring can significantly reduce leakage currents from nearby traces that are at different potentials.
- Cleaning the PCB following board assembly is recommended for best performance.
- Any precision integrated circuit may experience performance shifts due to moisture ingress into the plastic package. Following any aqueous PCB cleaning process, baking the PCB assembly is recommended to remove moisture introduced into the device packaging during the cleaning process. A low temperature, post cleaning bake at 85°C for 30 minutes is sufficient for most circumstances.

### 7.4.2 Layout Example
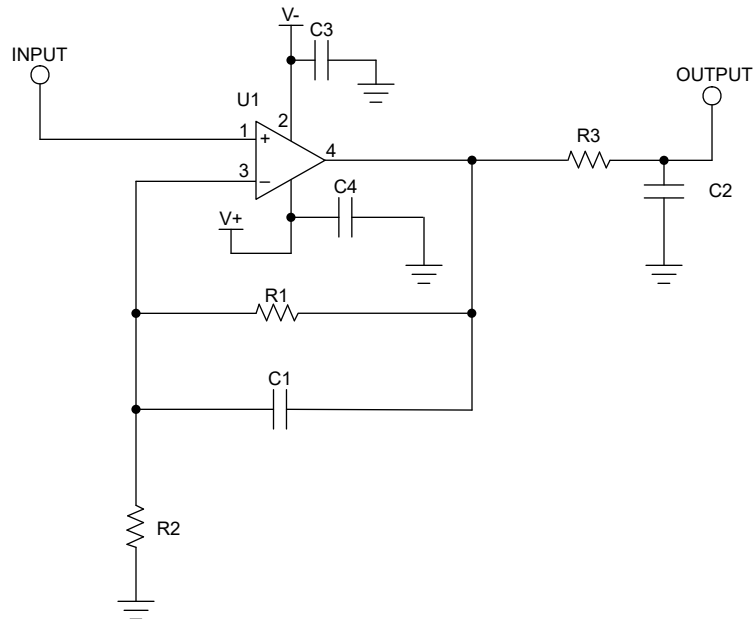


**Figure 7-3. Schematic for Noninverting Configuration Layout Example**
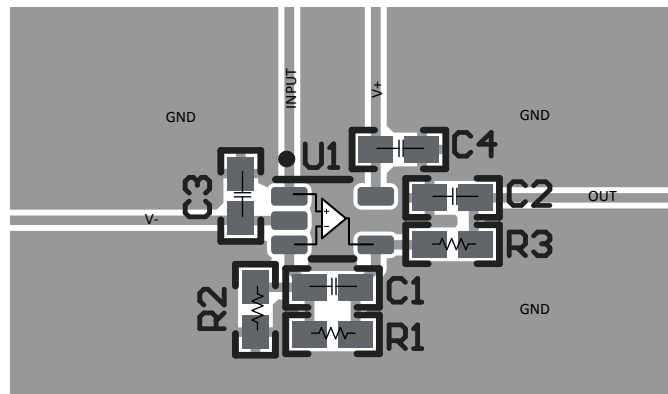


**Figure 7-4. Example Layout for SC70 (DCK) Package**

Product Folder Links: *OPA991-Q1 OPA2991-Q1 OPA4991-Q1*
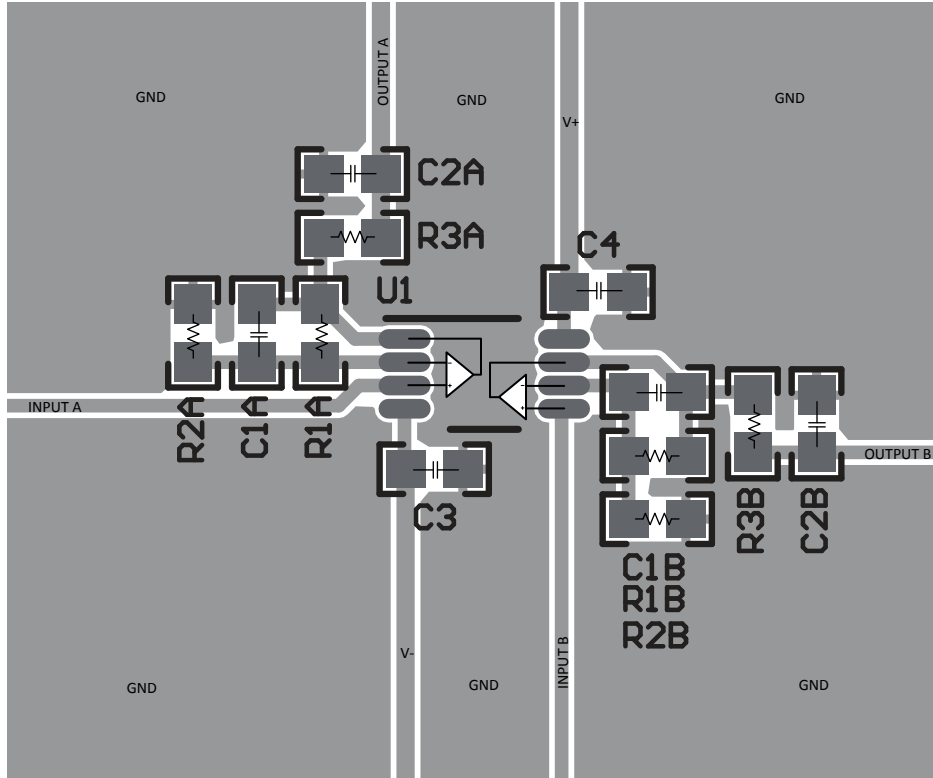
**Figure 7-5. Example Layout for VSSOP-8 (DGK) Package**

# 8 Device and Documentation Support

## 8.1 Device Support

### 8.1.1 Development Support

#### 8.1.1.1 TINA-TI™ (Free Software Download)

TINA™ is a simple, powerful, and easy-to-use circuit simulation program based on a SPICE engine. TINA-TI is a free, fully-functional version of the TINA software, preloaded with a library of macro models in addition to a range of both passive and active models. TINA-TI provides all the conventional dc, transient, and frequency domain analysis of SPICE, as well as additional design capabilities.

Available as a free download from the Analog eLab Design Center, TINA-TI offers extensive post-processing capability that allows users to format results in a variety of ways. Virtual instruments offer the ability to select input waveforms and probe circuit nodes, voltages, and waveforms, creating a dynamic quick-start tool.

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**Note**

These files require that either the TINA software (from DesignSoft™) or TINA-TI software be installed. Download the free TINA-TI software from the TINA-TI folder.

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#### 8.1.1.2 TI Precision Designs

The OPAx991 is featured in several TI Precision Designs, available online at http://www.ti.com/ww/en/analog/precision-designs/. TI Precision Designs are analog solutions created by TI's precision analog applications experts and offer the theory of operation, component selection, simulation, complete PCB schematic and layout, bill of materials, and measured performance of many useful circuits.

## 8.2 Documentation Support

### 8.2.1 Related Documentation

For related documentation, see the following:

*   Texas Instruments, *Analog Engineer's Circuit Cookbook: Amplifiers* solution guide
*   Texas Instruments, *AN31 Amplifier Circuit Collection* application note
*   Texas Instruments, *MUX-Friendly Precision Operational Amplifiers* application brief
*   Texas Instruments, *EMI Rejection Ratio of Operational Amplifiers* application report
*   Texas Instruments, *Op Amps With Complementary-Pair Input Stages* application note

## 8.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. Click on *Notifications* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

## 8.4 Support Resources

TI E2E™ support forums are an engineer's go-to source for fast, verified answers and design help — straight from the experts. Search existing answers or ask your own question to get the quick design help you need.

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## 8.5 Trademarks

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TI E2E™ is a trademark of Texas Instruments.
Bluetooth® is a registered trademark of Bluetooth SIG, Inc.
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## 8.6 Electrostatic Discharge Caution

This integrated circuit can be damaged by ESD. Texas Instruments recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage.

ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because very small parametric changes could cause the device not to meet its published specifications.

## 8.7 Glossary

TI Glossary            This glossary lists and explains terms, acronyms, and definitions.

## 9 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision G (October 2023) to Revision H (March 2024)**       **Page**
- Deleted preview note from 5-pin SC70 (DCK) and 6-pin SOT-23 (DBV) packages...........................................1
- Added HBM ESD rating for OPA991SQDBVRQ1.............................................................................................6
- Changed the schematic and VSSOP-8 (DGK) layout in the *Layout Example* section...................................30
- Added the SC70 (DCK) layout to the *Layout Example* section.......................................................................30

**Changes from Revision F (June 2023) to Revision G (October 2023)**       **Page**
- Added 5-pin SC70 (DCK) and 6-pin SOT-23 (DBV) information throughout data sheet...................................1

**Changes from Revision E (April 2023) to Revision F (June 2023)**       **Page**
- Changed the status of the TSSOP (8) package from: *preview* to: *active* .........................................................1
- Updated the format of the *Device Information* table.......................................................................................1

**Changes from Revision D (September 2021) to Revision E (April 2023)**       **Page**
- Added the TSSOP (8) package in *Package Information* table...........................................................................1

**Changes from Revision C (May 2021) to Revision D (September 2021)**       **Page**
- Deleted preview note from SOIC (14) package in *Device Information* table.....................................................1
- Deleted preview note from SOT-23 (14) package in *Device Information* table.................................................1
- Deleted preview note from SOIC (8) package in *Device Information* table.......................................................1
- Deleted preview note from SOT-23 (5) package in *Device Information* table....................................................1

**Changes from Revision B (March 2021) to Revision C (May 2021)**       **Page**
- Deleted preview note from TSSOP (14) package in *Device Information* table...................................................1

**Changes from Revision A (December 2020) to Revision B (March 2021)**       **Page**
- Changed data sheet status from "Advance Information" to "Production Data"....................................................1

## 10 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2991QDGKRQ1 | ACTIVE | VSSOP | DGK | 8 | 2500 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 27BT | Samples |
| OPA2991QDRQ1 | ACTIVE | SOIC | D | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O2991Q | Samples |
| OPA2991QPWRQ1 | ACTIVE | TSSOP | PW | 8 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OPA291 | Samples |
| OPA4991QDRQ1 | ACTIVE | SOIC | D | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OP4991QD | Samples |
| OPA4991QDYYRQ1 | ACTIVE | SOT-23-THIN | DYY | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | OPA4991Q | Samples |
| OPA4991QPWRQ1 | ACTIVE | TSSOP | PW | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O4991Q | Samples |
| OPA4991TQPWRQ1 | ACTIVE | TSSOP | PW | 14 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | O4991T | Samples |
| OPA991QDBVRQ1 | ACTIVE | SOT-23 | DBV | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 2JAF | Samples |
| OPA991QDCKRQ1 | ACTIVE | SC70 | DCK | 5 | 3000 | RoHS & Green | NIPDAU | Level-1-260C-UNLIM | -40 to 125 | 1MR | Samples |
| OPA991SQDBVRQ1 | ACTIVE | SOT-23 | DBV | 6 | 3000 | RoHS & Green | SN | Level-1-260C-UNLIM | -40 to 125 | 3BFH | Samples |

**(1)** The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

**(2)** **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

**(3)** MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

**(4)** There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

**(5)** Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

**(6)** Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF OPA2991-Q1, OPA4991-Q1, OPA991-Q1 :**

- Catalog : OPA2991, OPA4991, OPA991

- Enhanced Product : OPA4991-EP

NOTE: Qualified Version Definitions:

- Catalog - TI's standard catalog product

- Enhanced Product - Supports Defense, Aerospace and Medical Applications

# PACKAGE MATERIALS INFORMATION

## TAPE AND REEL INFORMATION

**REEL DIMENSIONS**

**TAPE DIMENSIONS**



| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| OPA2991QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 330.0 | 12.4 | 5.3 | 3.4 | 1.4 | 8.0 | 12.0 | Q1 |
| OPA2991QDRQ1 | SOIC | D | 8 | 3000 | 330.0 | 12.4 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |
| OPA2991QPWRQ1 | TSSOP | PW | 8 | 3000 | 330.0 | 12.4 | 7.0 | 3.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA4991QDRQ1 | SOIC | D | 14 | 3000 | 330.0 | 16.4 | 6.5 | 9.0 | 2.1 | 8.0 | 16.0 | Q1 |
| OPA4991QDYYRQ1 | SOT-23-THIN | DYY | 14 | 3000 | 330.0 | 12.4 | 4.8 | 3.6 | 1.6 | 8.0 | 12.0 | Q3 |
| OPA4991QPWRQ1 | TSSOP | PW | 14 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA4991TQPWRQ1 | TSSOP | PW | 14 | 3000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| OPA991QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA991QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |
| OPA991QDCKRQ1 | SC70 | DCK | 5 | 3000 | 178.0 | 9.0 | 2.4 | 2.5 | 1.2 | 4.0 | 8.0 | Q3 |
| OPA991SQDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 180.0 | 8.4 | 3.2 | 3.2 | 1.4 | 4.0 | 8.0 | Q3 |

**TAPE AND REEL BOX DIMENSIONS**



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| OPA2991QDGKRQ1 | VSSOP | DGK | 8 | 2500 | 366.0 | 364.0 | 50.0 |
| OPA2991QDRQ1 | SOIC | D | 8 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA2991QPWRQ1 | TSSOP | PW | 8 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA4991QDRQ1 | SOIC | D | 14 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA4991QDYYRQ1 | SOT-23-THIN | DYY | 14 | 3000 | 336.6 | 336.6 | 31.8 |
| OPA4991QPWRQ1 | TSSOP | PW | 14 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA4991TQPWRQ1 | TSSOP | PW | 14 | 3000 | 356.0 | 356.0 | 35.0 |
| OPA991QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA991QDBVRQ1 | SOT-23 | DBV | 5 | 3000 | 210.0 | 185.0 | 35.0 |
| OPA991QDCKRQ1 | SC70 | DCK | 5 | 3000 | 180.0 | 180.0 | 18.0 |
| OPA991SQDBVRQ1 | SOT-23 | DBV | 6 | 3000 | 210.0 | 185.0 | 35.0 |

3.0
2.6

1.75
1.45

B

A

PIN 1
INDEX AREA

1

5

2X 0.95

(0.1)

1.9

3.05
2.75

2

1.9

(0.15)

5X 0.5
0.3

3

4

⊕ 0.2Ⓜ C A B

NOTE 5

4X 0°-15°

C

◠ 0.1 C

0.15
0.00 TYP

(1.1)

1.45
0.90

4X 4°-15°

0.25
GAGE PLANE

0.22
0.08 TYP

8° TYP
0°

0.6
0.3 TYP

SEATING PLANE

4214839/K   08/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25 mm per side.
5. Support pin may differ or may not be present.

PKG

5X (1.1)

1

5X (0.6)

5

SYMM

2

(1.9)

2X (0.95)

3

4

(R0.05) TYP

(2.6)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

**SOLDER MASK DETAILS**

4214839/K 08/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214839/K   08/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

PIN 1
INDEX AREA

2.4
1.8

1.4
1.1

B

A

C

0.1 C

1.1 MAX

1

5

2X 0.65

2

NOTE 4

(0.15)

(0.1)

1.3

1.3

2.15
1.85

3

4

5X 0.33
0.15

0.1 M C A B

NOTE 5

(0.9)

0.1
0.0 TYP

0.15

GAGE PLANE

8°
0° TYP

0.46
0.26 TYP

0.22
0.08 TYP

SEATING PLANE

ALTERNATIVE PACKAGE
SINGULATION VIEW

4214834/E   06/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-203.
4. Support pin may differ or may not be present.
5. Lead width does not comply with JEDEC.
6. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.25mm per side

## DCK0005A

5X (0.95)

PKG

1

5X (0.4)

5

SYMM

(1.3)

2

2X (0.65)

3

4

(R0.05) TYP

(2.2)

### LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:18X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

### SOLDER MASK DETAILS

4214834/E   06/2024

NOTES: (continued)

7. Publication IPC-7351 may have alternate designs.
8. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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## DCK0005A

PKG

5X (0.95)

5X (0.4)

1

2X(0.65)

2

3

(R0.05) TYP

5

SYMM

(1.3)

4

(2.2)

SOLDER PASTE EXAMPLE
BASED ON 0.125 THICK STENCIL
SCALE:18X

4214834/E  06/2024

NOTES: (continued)

9. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
10. Board assembly site may have different recommendations for stencil design.

A

5.05 / 4.75 TYP

PIN 1 INDEX AREA

C

0.1 C

SEATING PLANE

1

8

6X 0.65

3.1 / 2.9
NOTE 3

2X 1.95

4

5

B

3.1 / 2.9
NOTE 4

8X 0.38 / 0.25

0.13 (M) C A B

SEE DETAIL A

0.23 / 0.13

0.25
GAGE PLANE

1.1 MAX

0°-8°

0.7 / 0.4

0.15 / 0.05

DETAIL A
TYPICAL

4214862/A   04/2023

PowerPAD is a trademark of Texas Instruments.

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-187.

SYMM

8X (1.4)

8X (0.45)    1

(R0.05) TYP

8

SYMM

6X (0.65)

4

5

SEE DETAILS

(4.4)

**LAND PATTERN EXAMPLE**
EXPOSED METAL SHOWN
SCALE: 15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.05 MAX
ALL AROUND

**NON-SOLDER MASK
DEFINED
(PREFERRED)**

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.05 MIN
ALL AROUND

**SOLDER MASK
DEFINED**

**SOLDER MASK DETAILS**

4214862/A   04/2023

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.
8. Vias are optional depending on application, refer to device data sheet. If any vias are implemented, refer to their locations shown on this view. It is recommended that vias under paste be filled, plugged or tented.
9. Size of metal pad may vary due to creepage requirement.

SYMM

8X (1.4)

(R0.05) TYP

8X (0.45)  1

8

SYMM

6X (0.65)

4

5

(4.4)

SOLDER PASTE EXAMPLE
SCALE: 15X

4214862/A   04/2023

NOTES: (continued)

11. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
12. Board assembly site may have different recommendations for stencil design.

PIN 1 INDEX AREA

SEATING PLANE

3.36 / 3.16

A

1

4.3 / 4.1 NOTE 3

7

14

12X 0.5

2X 3

8

14X 0.3 / 0.11

⊕ 0.1 Ⓜ C A B

△ 0.1 C

1.1 MAX

△ 0.1 C

B

2.1 / 1.9

C

ALTERNATIVE PACKAGE SINGULATION VIEW

SEE DETAIL A

0.2 / 0.08 TYP

0.25 GAUGE PLANE

0°- 8°

0.63 / 0.33

0.1 / 0.0

DETAIL A
TYP

4224643/C  04/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.50 per side.
5. Reference JEDEC Registration MO-345, Variation AB

SYMM
℄

14X (1.05)

1

14

14X (0.3)

SYMM
℄

12X (0.5)

7

8

(R0.05) TYP

(3)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 20X

SOLDER MASK
OPENING

METAL

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

NON- SOLDER MASK
DEFINED
(PREFERRED)

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4224643/C   04/2024

NOTES: (continued)

6.  Publication IPC-7351 may have alternate designs.
7.  Solder mask tolerances between and around signal pads can vary based on board fabrication site.

SYMM

14X (1.05)

1

14X (0.3)

14

12X (0.5)

7

8

(R0.05) TYP

SYMM

(3)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 20X

4224643/C   04/2024

NOTES: (continued)
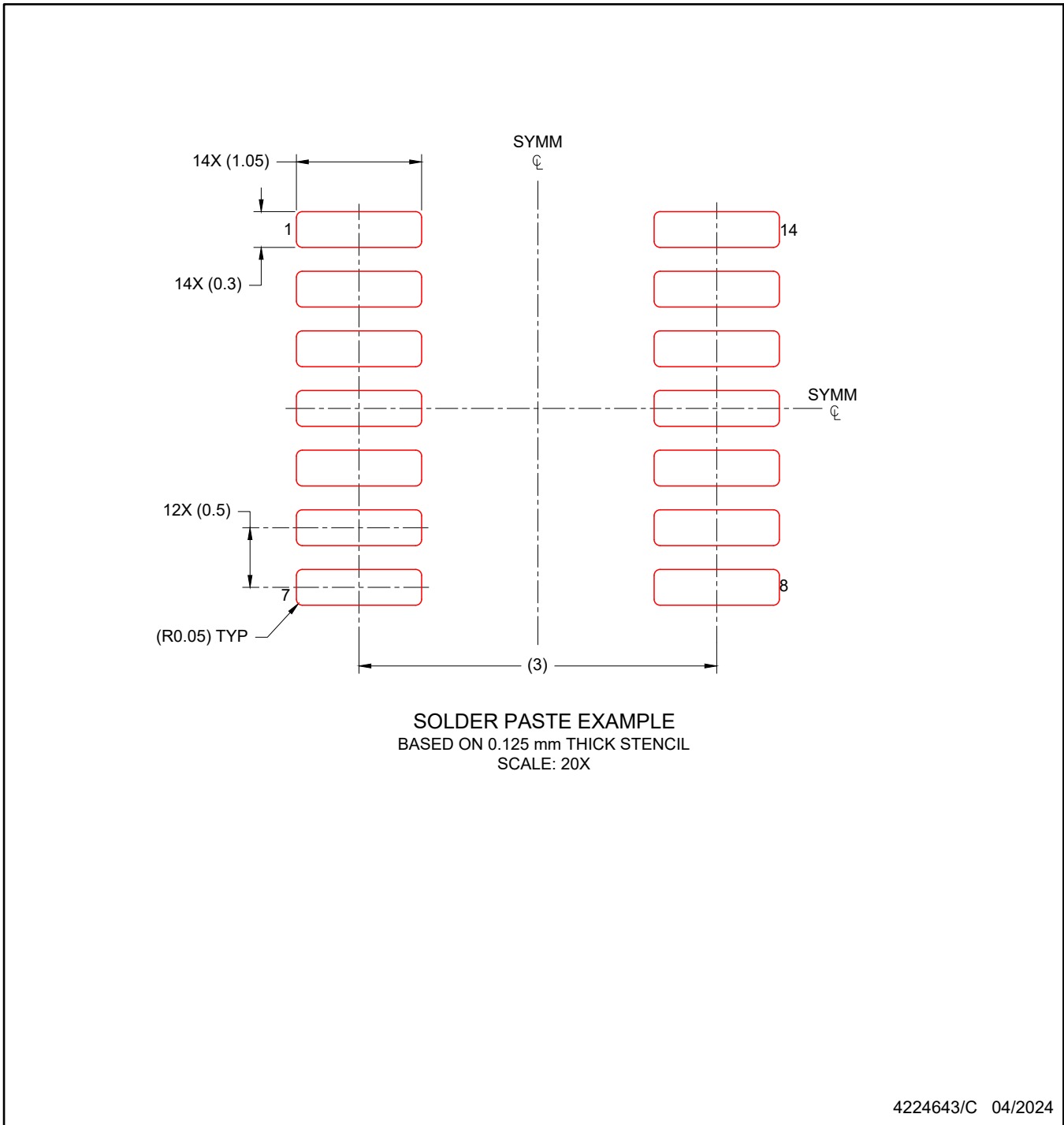
8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

D (R−PDSO−G14)                                        PLASTIC SMALL OUTLINE



0.344 (8,75)
0.337 (8,55)
△C

14                                              8

0.244 (6,20)
0.228 (5,80)

0.157 (4,00)
0.150 (3,80)  △D

1                                               7

Pin 1
Index Area

0.050 (1,27)          0.020 (0,51)
                       0.012 (0,31)
                      ⊕ 0.010 (0,25) Ⓜ

0.069 (1,75) Max                              0.010 (0,25)
                                              0.004 (0,10)

0.010 (0,25)
0.005 (0,13)

Gauge Plane                                   0.004 (0,10)

                                              Seating Plane

0.010 (0,25)        0°−8°

0.050 (1,27)
0.016 (0,40)

4040047−5/M   06/11

NOTES:   A.  All linear dimensions are in inches (millimeters).
         B.  This drawing is subject to change without notice.
       △C.  Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0.006 (0,15) each side.
       △D.  Body width does not include interlead flash.  Interlead flash shall not exceed 0.017 (0,43) each side.
         E.  Reference JEDEC MS−012 variation AB.

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PW (R−PDSO−G14)                                          PLASTIC SMALL OUTLINE

0,65

0,30
0,19

⊕ | 0,10 Ⓜ

14                    8

△D    4,50
      4,30

6,60
6,20

1                     7

5,10
4,90

△C

0,15 NOM

Gage Plane

0°−8°

0,25

0,75
0,50

1,20 MAX

0,15
0,05

Seating Plane

⌂ | 0,10

4040064−3/G  02/11

NOTES:   A.   All linear dimensions are in millimeters.  Dimensioning and tolerancing per ASME Y14.5M−1994.
         B.   This drawing is subject to change without notice.
        △C.   Body length does not include mold flash, protrusions, or gate burrs.  Mold flash, protrusions, or gate burrs shall
              not exceed 0,15 each side.
        △D.   Body width does not include interlead flash.  Interlead flash shall not exceed 0,25 each side.
         E.   Falls within JEDEC MO−153

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.228-.244  TYP
[5.80-6.19]

A

PIN 1 ID AREA

.189-.197
[4.81-5.00]
NOTE 3

1

4

8

5

6X .050
[1.27]

2X
.150
[3.81]

8X .012-.020
[0.31-0.51]

⊕ .010 [0.25] Ⓜ C A B

B

.150-.157
[3.81-3.98]
NOTE 4

C

SEATING PLANE

◯ .004 [0.1] C

4X (0°-15°)

.069 MAX
[1.75]

SEE DETAIL A

4X (0°-15°)

.005-.010  TYP
[0.13-0.25]

.010
[0.25]

0° - 8°

.016-.050
[0.41-1.27]

(.041)
[1.04]

.004-.010
[0.11-0.25]

DETAIL A
TYPICAL

4214825/C   02/2019

NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.

8X (.061 )
[1.55]

SYMM
₵

SEE
DETAILS

1

8X (.024)
[0.6]

SYMM
₵

8

6X (.050 )
[1.27]

4

(R.002 ) TYP
[0.05]

5

(.213)
[5.4]

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X

METAL

SOLDER MASK
OPENING

SOLDER MASK
OPENING

METAL UNDER
SOLDER MASK

EXPOSED
METAL

EXPOSED
METAL

.0028 MAX
[0.07]
ALL AROUND

.0028 MIN
[0.07]
ALL AROUND

NON SOLDER MASK
DEFINED

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214825/C   02/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

8X (.061 )
[1.55]

1

8X (.024)
[0.6]

SYMM
₵

SYMM
₵

8

(R.002 ) TYP
[0.05]

6X (.050 )
[1.27]

4

5

(.213)
[5.4]

SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C  02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
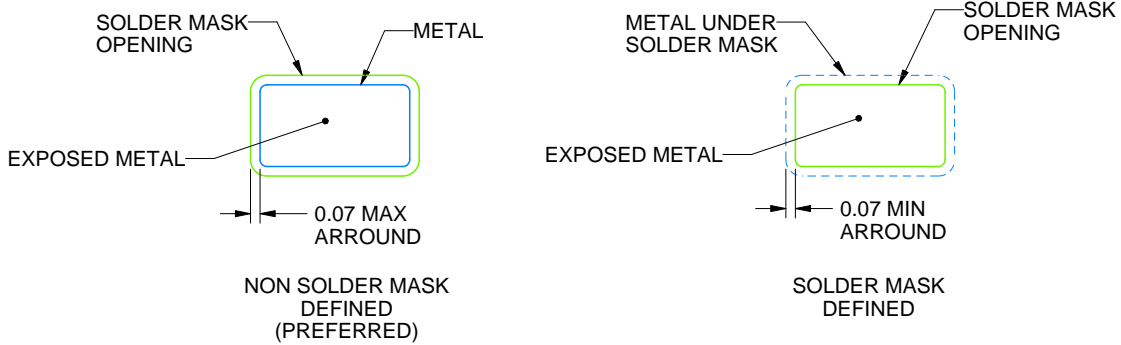9. Board assembly site may have different recommendations for stencil design.

3.0
2.6

1.75
1.45

B

A

PIN 1
INDEX AREA

1

2X | 0.95 |

1.9

2

6X | 0.50 |
| 0.25 |

⊕ | 0.2Ⓜ | C | A | B |

3

6

3.05
2.75

5

4

C

| ⌒ | 0.1 | C |

(1.1)

1.45
0.90

0.15 TYP
0.00

| 0.25 |

GAGE PLANE

8° TYP
0°

0.6 TYP
0.3

SEATING PLANE

0.22 TYP
0.08

ALTERNATIVE PACKAGE SINGULATION VIEW

4214840/F   05/2024

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing
   per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.25 per side.
4. Leads 1,2,3 may be wider than leads 4,5,6 for package orientation.
5. Refernce JEDEC MO-178.

## DBV0006A

PKG

6X (1.1)

1

6X (0.6)

6

2

SYMM

5

2X (0.95)

3

4

(R0.05) TYP

(2.6)

LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X

SOLDER MASK
OPENING

METAL

EXPOSED METAL

0.07 MAX
ARROUND

NON SOLDER MASK
DEFINED
(PREFERRED)

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

EXPOSED METAL

0.07 MIN
ARROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS

4214840/F   05/2024

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

PKG

6X (1.1)

1

6X (0.6)

6

2

SYMM

5

2X(0.95)

3

4

(R0.05) TYP

(2.6)

SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

4214840/F   05/2024

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate
   design recommendations.
9. Board assembly site may have different recommendations for stencil design.

SEATING PLANE

C

0.1 C

6X 0.65

2X 1.95

8X 0.30
0.19

⊕ 0.1 Ⓜ C AⓈ BⓈ

1.2 MAX

6.6
6.2 TYP

PIN 1 ID
AREA

A

1

8

3.1
2.9
NOTE 3

4

5

B

4.5
4.3
NOTE 4

SEE DETAIL A

(0.15) TYP

0.25

GAGE PLANE

0° - 8°

0.75
0.50

0.15
0.05

**DETAIL A**
TYPICAL

4221848/A   02/2015

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153, variation AA.

8X (1.5)

8X (0.45)

1

SYMM

(R0.05)
TYP

8

SYMM

6X (0.65)

4

5

(5.8)

LAND PATTERN EXAMPLE
SCALE:10X

SOLDER MASK
OPENING

METAL

0.05 MAX
ALL AROUND

NON SOLDER MASK
DEFINED

METAL UNDER
SOLDER MASK

SOLDER MASK
OPENING

0.05 MIN
ALL AROUND

SOLDER MASK
DEFINED

SOLDER MASK DETAILS
NOT TO SCALE

4221848/A  02/2015

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

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## PW0008A

8X (0.45)

8X (1.5)

1

SYMM

(R0.05) TYP

8

SYMM

6X (0.65)

4

5

(5.8)

**SOLDER PASTE EXAMPLE**
BASED ON 0.125 mm THICK STENCIL
SCALE:10X

4221848/A   02/2015

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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