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## SAMA5D2 System in Package (SiP) MPU with up to 1 Gbit DDR2 SDRAM or 2 Gbit LPDDR2 SDRAM

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### Scope

This document is an overview of the main features of the SAMA5D2 SIP. The sole reference documents for product information on the SAMA5D2 and the LPDDR2/DDR2-SDRAM memories are listed in the table below.

### Introduction

The SAMA5D2 System-In-Package (SIP) integrates the Arm<sup>®</sup> Cortex<sup>®</sup>-A5 processor-based SAMA5D2 MPU with up to 1 Gbit DDR2-SDRAM or up to 2 Gbit LPDDR2-SDRAM in a single package.

By combining the high-performance, ultra-low power SAMA5D2 with LPDDR2/DDR2-SDRAM in a single package, PCB routing complexity, area and number of layers is reduced in the majority of cases. This makes board design easier and more robust by facilitating design for EMI, ESD and signal integrity.

DDR2-SDRAM memory sizes and package options available

- 128 Mbit, TFBGA196
- 512 Mbit and 1 Gbit, TFBGA289

LPDDR2-SDRAM memory sizes and package options available

- 1 Gbit and 2 Gbit, TFBGA361

While the smallest option targets applications with a small OS or bare metal, the larger options are suitable for applications using Linux<sup>®</sup>.

### Reference Documents

| Type       | Document Title  | Available  | Ref. No.   |
|------------|---|--|------------|
| Data sheet | SAMA5D2 Series  | <a href="http://www.microchip.com">www.microchip.com</a> | DS60001476 |
| Data sheet | 2 Mwords × 4 Banks × 16 bits<br>DDR2 SDRAM (128 Mbit) | <a href="http://www.winbond.com">www.winbond.com</a>     | W9712G6KB  |
| Data sheet | 8 Mwords × 4 Banks × 16 bits<br>DDR2 SDRAM (512 Mbit) | <a href="http://www.winbond.com">www.winbond.com</a>     | W9751G6KB  |
| Data sheet | 8 Mwords × 8 Banks × 16 bits<br>DDR2 SDRAM (1 Gbit)   | <a href="http://www.winbond.com">www.winbond.com</a>     | W971GG6SB  |
| Data sheet | 4 Mwords × 8 Banks × 32 bits<br>LPDDR2-SDRAM (1 Gbit) | <a href="http://www.apmemory.com">www.apmemory.com</a>   | AD2100XXX- |

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| Type       | Document Title  | Available  | Ref. No.   |
|------------|---|--|------------|
| Data sheet | 8 Mwords × 8 Banks × 32 bits<br>LPDDR2-SDRAM (2 Gbit) | <a href="http://www.apmemory.com">www.apmemory.com</a> | AD2200XXX- |

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## 1. Features

- Arm Cortex-A5 core
  - ARMv7-A architecture
  - Arm TrustZone®
  - NEON™ Media Processing Engine
  - Up to 500 MHz
  - ETM/ETB 8 Kbytes
- Memory Architecture
  - Memory Management Unit
  - 32-Kbyte L1 data cache, 32-Kbyte L1 instruction cache
  - 128-Kbyte L2 cache configurable to be used as an internal SRAM
  - DDR2-SDRAM memory up to 1 Gb
  - LPDDR2-SDRAM memory up to 2 Gb
  - One 128-Kbyte scrambled internal SRAM
  - One 160-Kbyte internal ROM
    - 64-Kbyte scrambled and maskable ROM embedding bootloader/Secure bootloader
    - 96-Kbyte unscrambled, unmaskable ROM for NAND Flash BCH ECC table
  - High-bandwidth scramblable 16-bit Double Data Rate (DDR) multiport dynamic RAM controller supporting Winbond DDR2-SDRAM up to 1 Gb, including “on-the-fly” encryption/decryption path
  - High-bandwidth scramblable 32-bit Double Data Rate (DDR) multiport dynamic RAM controller supporting AP memory LPDDR2-SDRAM up to 2 Gb , including “on-the-fly” encryption/decryption path
  - 8-bit SLC/MLC NAND controller, with up to 32-bit Error Correcting Code (PMECC)
- System Running up to 166 MHz
  - Reset controller, shutdown controller, periodic interval timer, independent watchdog timer and secure Real-Time Clock (RTC) with clock calibration
  - One 600 to 1200 MHz PLL for the system and one 480 MHz PLL optimized for USB high speed
  - Digital fractional PLL for audio (11.2896 MHz and 12.288 MHz)
  - Internal low-power 12 MHz RC and 32 KHz typical RC
  - Selectable 32.768-Hz low-power oscillator and 8 to 24 MHz oscillator
  - 51 DMA Channels including two 16-channel 64-bit Central DMA Controllers
  - 64-bit Advanced Interrupt Controller (AIC)
  - 64-bit Secure Advanced Interrupt Controller (SAIC)
  - Three programmable external clock signals
- Low-Power Modes
  - Ultra-Low-Power mode with fast wake-up capability
  - Low-Power Backup mode with 5-Kbyte SRAM and SleepWalking™ features
    - Wake-up from up to nine wake-up pins, UART reception, analog comparison
    - Fast wake-up capability
    - Extended Backup mode with LPDDR2/DDR2-SDRAM in Self-Refresh mode

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- Peripherals
    - LCD TFT controller up to 1024x768, with four overlays, rotation, post-processing and alpha blending, 24-bit parallel RGB
    - ITU-R BT. 601/656/1120 Image Sensor Controller (ISC) supporting up to 5 M-pixel sensors with a parallel 12-bit interface for Raw Bayer, YCbCr, Monochrome and JPEG-compressed sensor interface
    - Two Synchronous Serial Controllers (SSC), two Inter-IC Sound Controllers (I2SC), and one Stereo Class D amplifier
    - One Peripheral Touch Controller (PTC) with up to 8 X-lines and 8 Y-lines (64-channel capacitive touch)
    - One Pulse Density Modulation Interface Controller (PDMIC)
    - One USB high-speed device port (UDPHS) and one USB high-speed host port or two USB high-speed host ports (UHPHS)
    - One USB high-speed host port with a High-Speed Inter-Chip (HSIC) interface
    - One 10/100 Ethernet MAC (GMAC)
      - Energy efficiency support (IEEE 802.3az standard)
      - Ethernet AVB support with IEEE802.1AS time stamping
      - IEEE®802.1Qav credit-based traffic-shaping hardware support
      - IEEE1588 Precision Time Protocol (PTP)
    - Two high-speed memory card hosts:
      - SDMMC0: SD 3.0, eMMC 4.51, 8 bits
      - SDMMC1: SD 2.0, eMMC 4.41, 4 bits only
    - Two master/slave Serial Peripheral Interfaces (SPI)
    - Two Quad Serial Peripheral Interfaces (QSPI)
    - Five FLEXCOMs (USART, SPI and TWI)
    - Five UARTs
    - Two master CAN-FD (MCAN) controllers with SRAM-based mailboxes, and time- and event-triggered transmission
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-  **WARNING** MCAN implements the non-ISO CAN FD frame format and therefore does not pass the CAN FD Conformance Test according to ISO 16845-1:2016.
- 
- One Rx only UART in backup area (RXLP)
  - One analog comparator (ACC) in backup area
  - Two 2-wire interfaces (TWIHS) up to 400 Kbits/s supporting the I<sup>2</sup>C protocol and SMBUS (TWIHS)
  - Two 3-channel 32-bit Timer/Counters (TC), supporting basic PWM modes
  - One full-featured 4-channel 16-bit Pulse Width Modulation (PWM) controller
  - One 12-channel, 12-bit, Analog-to-Digital Converter (ADC) with Resistive TouchScreen capability
- Safety
    - Zero-power Power-On Reset (POR) cells
    - Main crystal clock failure detector
    - Write-protected registers

- Integrity Check Monitor (ICM) based on SHA256
- Memory Management Unit
- Independent watchdog
- Security
  - 5 Kbytes of internal scrambled SRAM:
    - 1 Kbyte non-erasable on tamper detection
    - 4 Kbytes erasable on tamper detection
  - 256 bits of scrambled and erasable registers
  - Up to eight tamper pins for static or dynamic intrusion detections<sup>(1)</sup>
  - Environmental monitors on specific versions: temperature, voltage, frequency and active die shield<sup>(2)</sup>
  - Secure Boot Loader<sup>(3)</sup>
  - On-the-fly AES encryption/decryption on LPDDR2/DDR2-SDRAM and QSPI memories (AESB)
  - RTC including time-stamping on security intrusions
  - Programmable fuse box with 544 fuse bits (including JTAG protection and BMS)
- Hardware cryptography
  - SHA (SHA1, SHA224, SHA256, SHA384, SHA512): compliant with FIPS PUB 180-2
  - AES: 256-, 192-, 128-bit key algorithm, compliant with FIPS PUB 197
  - TDES: two-key or three-key algorithms, compliant with FIPS PUB 46-3
  - True Random Number Generator (TRNG) compliant with NIST Special Publication 800-22 Test Suite and FIPS PUBs 140-2 and 140-3
- Up to 128 I/Os
  - Fully programmable through set/clear registers
  - Multiplexing of up to eight peripheral functions per I/O line
  - Each I/O line can be assigned to a peripheral or used as a general purpose I/O
  - PIO controller features a synchronous output providing up to 32 bits of data output in one write operation

**Note:**

1. For information specific to dynamic tamper protection (PIOBU), refer to the document *SAMA5D2 External Tamper Protections* (document no. 44095).
2. For environmental monitors, refer to the document *SAMA5D23 and SAMA5D28 Environmental Monitors* (document no. 44036), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.
3. For secure boot strategies, refer to the document *SAMA5D2 Series Secure Boot Strategy* (document no. 44040), available under Non-Disclosure Agreement (NDA). Contact a Microchip sales representative for details.

## **2. DDR2-SDRAM Features**

- Power Supply: DDRM\_VDD, DDRM\_VDDL, DDRM\_VDDQ = 1.8 V  $\pm$ 0.1 V
- Double Data Rate Architecture: Two Data Transfers per Clock Cycle
- CAS Latency: 3
- Burst Length: 8
- Bi-Directional, Differential Data Strokes (DQS and DQSN) are Transmitted/Received with Data
- Edge-Aligned with Read Data and Center-Aligned with Write Data
- DLL Aligns DQ and DQS Transitions with Clock
- Differential Clock Inputs (CLK and CLKN)
- Data Masks (DM) for Write Data
- Commands Entered on Each Positive CLK Edge, Data and Data Mask are Referenced to Both Edges of DQS
- Auto-Refresh and Self-Refresh Modes
- Precharged Power-Down and Active Power-Down
- Write Data Mask
- Write Latency = Read Latency - 1 (WL = RL - 1)
- Interface: SSTL\_18



### 3. LPDDR2-SDRAM Features

- Power Supply: DDRM\_VDD18 = 1.7 to 1.9V
- Power Supply: DDRM\_VDD12 = 1.14 to 1.3V
- Double Data Rate Architecture: Two Data Transfers per Clock Cycle
- Burst Length (BL): 4, 8, 16
- Write Latency (WL): 1, 2, 3, 4
- Read Latency (RL): 3, 4, 5, 6, 7, 8
- Bi-Directional, Differential Data Strokes (DQS and DQSN) are Transmitted/Received with Data
- Edge-Aligned with Read Data and Center-Aligned with Write Data
- Differential Clock Inputs (CLK and CLKN)
- Data Masks (DM) for Write Data
- Commands Entered on each Positive CLK Edge, Data and Data Mask are Referenced to Both Edges of DQS
- Interface: HSUL\_12
- Auto-Refresh and Self-Refresh Modes
- Low Power Consumption
- JEDEC LPDDR2-S4B Compliance
- Partial Array Self-Refresh (PASR)
- Auto Temperature Compensated Self-Refresh (ATCSR) by Built-in Temperature Sensor
- Deep Power-Down Mode

### 4. Configuration Summary

**Table 4-1. Configuration Summary**

| Feature                            | SAMA5D225                         | SAMA5D27  |      |          |      | SAMA5D28 |          |      |
|------------------------------------|-----------------------------------|---|------|----------|------|----------|----------|------|
| Package                            | TFBGA196                          | TFBGA289  |      | TFBGA361 |      | TFBGA289 | TFBGA361 |      |
| DDR2-SDRAM                         | 128 Mb                            | 512 Mb  | 1 Gb | –        | –    | 1 Gb     | –        | –    |
| LPDDR2-SDRAM                       | –                                 | –   | –    | 1 Gb     | 2 Gb | –        | 1 Gb     | 2 Gb |
| SMC                                | Up to 16-bit                      |   |      |          |      |          |          |      |
| Internal Memory Bus Width          | 16-bit                            |   |      | 32-bit   |      | 16-bit   | 32-bit   |      |
| PIOs                               | 90                                | 128   |      |          |      |          |          |      |
| SRAM                               | 128 Kbytes                        |   |      |          |      |          |          |      |
| QSPI                               | 2                                 |   |      |          |      |          |          |      |
| LCD                                | 24-bit RGB                        |   |      |          |      |          |          |      |
| Camera Interface (ISC)             | 1                                 |   |      |          |      |          |          |      |
| EMAC                               | 1                                 |   |      |          |      |          |          |      |
| PTC                                | 4 X-lines x 8 Y-lines             | 8 X-lines x 8 Y-lines                           |      |          |      |          |          |      |
| CAN                                | 1                                 | 2   |      |          |      |          |          |      |
| USB                                | 2<br>(2 Hosts or 1 Host/1 Device) | 3<br>(2 Hosts/1 HSIC or 1 Host/1 Device/1 HSIC) |      |          |      |          |          |      |
| UART/SPI/I <sup>2</sup> C          | 9 / 7 / 7                         | 10 / 7 / 7                                      |      |          |      |          |          |      |
| SDIO/SD/MMC                        | 2                                 |   |      |          |      |          |          |      |
| I <sup>2</sup> S/SSC/Class D/PDM   | 2 / 2 / 1 / 1                     |   |      |          |      |          |          |      |
| ADC Inputs                         | 5                                 | 12  |      |          |      |          |          |      |
| Timers                             | 5                                 | 6   |      |          |      |          |          |      |
| PWM                                | 4 (PWM) + 5 (TC)                  | 4 (PWM) + 6 (TC)                                |      |          |      |          |          |      |
| Tamper Pins                        | 6                                 | 8   |      |          |      |          |          |      |
| AESB                               | Yes                               |   |      |          |      |          |          |      |
| Environmental Monitors, Die Shield | –                                 | –   | –    | –        | –    | –        | –        | Yes  |

## 5. Chip Identifier

Table 5-1. SAMA5D2 SIP Chip ID Registers

| Chip Name      | CHIPID_CIDR | CHIPID_EXID |
|----------------|-------------|-------------|
| SAMA5D225C-D1M | 0x8A5C08C2  | 0x00000053  |
| SAMA5D27C-D5M  |             | 0x00000032  |
| SAMA5D27C-D1G  |             | 0x00000033  |
| SAMA5D27C-LD1G |             | 0x00000061  |
| SAMA5D27C-LD2G |             | 0x00000062  |
| SAMA5D28C-D1G  |             | 0x00000013  |
| SAMA5D28C-LD1G |             | 0x00000071  |
| SAMA5D28C-LD2G |             | 0x00000072  |

## 6. Package and Ballout

The SAMA5D2 SIP is available in the packages listed below.



**Important:** SAMA5D2 DDR2 SIP devices are not pin-to-pin compatible with SAMA5D2 devices.

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**Table 6-1. Packages**

| Package Name            | Ball Count | Ball Pitch | Package Size |
|-------------------------|------------|------------|--------------|
| TFBGA196                | 196        | 0.75 mm    | 11 x 11 (mm) |
| TFBGA289 <sup>(1)</sup> | 289        | 0.8 mm     | 14 x 14 (mm) |
| TFBGA361 <sup>(2)</sup> | 361        | 0.8 mm     | 16 x 16 (mm) |

**Note:**

1. 512 Mbit and 1 Gbit DDR2 in TFBGA289 have the same ballout.
2. 1 Gbit and 2 Gbit LPDDR2 in TFBGA361 have the same ballout.

Table 6-2. Ball Description

| 361-ball<br>BGA | 289-ball<br>BGA | 196-ball<br>BGA | Power Rail | I/O<br>Type | Primary |     | Alternate |     | PIO Peripheral |              |     |           | Reset State<br>(Signal, Dir,<br>PU, PD,<br>HiZ, ST) <sup>(1)</sup> |
|-----------------|-----------------|-----------------|------------|-------------|---------|-----|-----------|-----|----------------|--------------|-----|-----------|--|
|                 |                 |                 |            |             | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO<br>Set |  |
| W11             | U13             | M8              | VDDSDMMC   | GPIO_EMMC   | PA0     | I/O | -         | -   | A              | SDMMC0_CK    | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPIO_SCK    | O   | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D0           | I/O | 2         |  |
| R9              | N7              | F7              | VDDSDMMC   | GPIO_EMMC   | PA1     | I/O | -         | -   | A              | SDMMC0_CMD   | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPIO_CS     | O   | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D1           | I/O | 2         |  |
| W12             | U14             | L8              | VDDSDMMC   | GPIO_EMMC   | PA2     | I/O | -         | -   | A              | SDMMC0_DAT0  | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPIO_IO0    | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D2           | I/O | 2         |  |
| V11             | T13             | G8              | VDDSDMMC   | GPIO_EMMC   | PA3     | I/O | -         | -   | A              | SDMMC0_DAT1  | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPIO_IO1    | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D3           | I/O | 2         |  |
| W14             | U15             | K8              | VDDSDMMC   | GPIO_EMMC   | PA4     | I/O | -         | -   | A              | SDMMC0_DAT2  | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPIO_IO2    | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D4           | I/O | 2         |  |
| V10             | U16             | P9              | VDDSDMMC   | GGPIO_EMMC  | PA5     | I/O | -         | -   | A              | SDMMC0_DAT3  | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPIO_IO3    | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D5           | I/O | 2         |  |
| W15             | U17             | P10             | VDDSDMMC   | GPIO_EMMC   | PA6     | I/O | -         | -   | A              | SDMMC0_DAT4  | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPI1_SCK    | O   | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | D              | TIOA5        | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | E              | FLEXCOM2_IO0 | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D6           | I/O | 2         |  |
| W16             | R11             | P11             | VDDSDMMC   | GPIO_EMMC   | PA7     | I/O | -         | -   | A              | SDMMC0_DAT5  | I/O | 1         | PIO, I, PU, ST   |
|                 |                 |                 |            |             |         |     |           |     | B              | QSPI1_IO0    | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | D              | TIOB5        | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | E              | FLEXCOM2_IO1 | I/O | 1         |  |
|                 |                 |                 |            |             |         |     |           |     | F              | D7           | I/O | 2         |  |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type  | Primary |     | Alternate |     | PIO Peripheral |               |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|-----------|---------|-----|-----------|-----|----------------|---------------|-----|--------|---|
|              |              |              |            |           | Signal  | Dir | Signal    | Dir | Func           | Signal        | Dir | IO Set |   |
| V12          | R9           | K9           | VDDSDMMC   | GPIO_EMMC | PA8     | I/O | -         | -   | A              | SDMMC0_DAT6   | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | QSPI1_IO1     | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | D              | TCLK5         | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | FLEXCOM2_IO2  | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | NWE/NANDWE    | O   | 2      |   |
| V16          | P8           | J9           | VDDSDMMC   | GPIO_EMMC | PA9     | I/O | -         | -   | A              | SDMMC0_DAT7   | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | QSPI1_IO2     | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | D              | TIOA4         | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | FLEXCOM2_IO3  | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | NCS3          | O   | 2      |   |
| V14          | R10          | N14          | VDDSDMMC   | GPIO_EMMC | PA10    | I/O | -         | -   | A              | SDMMC0_RSTN   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | QSPI1_IO3     | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | D              | TIOB4         | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | FLEXCOM2_IO4  | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | A21/NANDALE   | O   | 2      |   |
| L18          | P15          | N13          | VDDIOP1    | GPIO      | PA11    | I/O | -         | -   | A              | SDMMC0_1V8SEL | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | QSPI1_CS      | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | D              | TCLK4         | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | A22/NANDCLE   | O   | 2      |   |
| T16          | N17          | L12          | VDDIOP1    | GPIO      | PA12    | I/O | -         | -   | A              | SDMMC0_WP     | I   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | IRQ           | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | NRD/NANDOE    | O   | 2      |   |
| K18          | P16          | M14          | VDDIOP1    | GPIO      | PA13    | I/O | -         | -   | A              | SDMMC0_CD     | I   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | E              | FLEXCOM3_IO1  | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | D8            | I/O | 2      |   |
| R19          | M17          | J10          | VDDIOP1    | GPIO_QSPI | PA14    | I/O | -         | -   | A              | SPI0_SPCK     | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | TK1           | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | QSPI0_SCK     | O   | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | I2SC1_MCK     | O   | 2      |   |
|              |              |              |            |           |         |     |           |     | E              | FLEXCOM3_IO2  | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | D9            | I/O | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| L17          | N16          | L14          | VDDIOP1    | GPIO     | PA15    | I/O | -         | -   | A              | SPI0_MOSI    | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | TF1          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | QSPIO_CS     | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | I2SC1_CK     | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO0 | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | D10          | I/O | 2      |   |
| N19          | M11          | H14          | VDDIOP1    | GPIO_IO  | PA16    | I/O | -         | -   | A              | SPI0_MISO    | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | TD1          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | QSPIO_IO0    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | I2SC1_WS     | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO3 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | D11          | I/O | 2      |   |
| M16          | N14          | K14          | VDDIOP1    | GPIO_IO  | PA17    | I/O | -         | -   | A              | SPI0_NPCS0   | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | RD1          | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | QSPIO_IO1    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | I2SC1_DI0    | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO4 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | D12          | I/O | 2      |   |
| V19          | T16          | L9           | VDDIOP1    | GPIO_IO  | PA18    | I/O | -         | -   | A              | SPI0_NPCS1   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | RK1          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | QSPIO_IO2    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | I2SC1_DO0    | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | SDMMC1_DAT0  | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | D13          | I/O | 2      |   |
| V15          | T15          | P12          | VDDIOP1    | GPIO_IO  | PA19    | I/O | -         | -   | A              | SPI0_NPCS2   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | RF1          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | QSPIO_IO3    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOA0        | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | SDMMC1_DAT1  | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | D14          | I/O | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type  | Primary |     | Alternate |     | Func | PIO Peripheral |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|-----------|---------|-----|-----------|-----|------|----------------|-----|--------|---|
|              |              |              |            |           | Signal  | Dir | Signal    | Dir |      | Signal         | Dir | IO Set |   |
| T10          | P9           | H9           | VDDIOP1    | GPIO_IO   | PA20    | I/O | -         | -   | A    | SPI0_NPCS3     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | D    | TIOB0          | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | E    | SDMMC1_DAT2    | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | F    | D15            | I/O | 2      |   |
| U19          | P10          | G9           | VDDIOP1    | GPIO_IO   | PA21    | I/O | -         | -   | A    | IRQ            | I   | 2      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B    | PCK2           | O   | 3      |   |
|              |              |              |            |           |         |     |           |     | D    | TCLK0          | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | E    | SDMMC1_DAT3    | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | F    | NANDRDY        | I   | 2      |   |
| V17          | T17          | K10          | VDDIOP1    | GPIO_QSPI | PA22    | I/O | -         | -   | A    | FLEXCOM1_IO2   | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B    | D0             | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C    | TCK            | I   | 4      |   |
|              |              |              |            |           |         |     |           |     | D    | SPI1_SPCK      | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | E    | SDMMC1_CK      | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | F    | QSPI0_SCK      | O   | 3      |   |
| U18          | T14          | G10          | VDDIOP1    | GPIO      | PA23    | I/O | -         | -   | A    | FLEXCOM1_IO1   | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B    | D1             | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C    | TDI            | I   | 4      |   |
|              |              |              |            |           |         |     |           |     | D    | SPI1_MOSI      | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | F    | QSPI0_CS       | O   | 3      |   |
| W17          | R17          | P13          | VDDIOP1    | GPIO_IO   | PA24    | I/O | -         | -   | A    | FLEXCOM1_IO0   | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B    | D2             | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C    | TDO            | O   | 4      |   |
|              |              |              |            |           |         |     |           |     | D    | SPI1_MISO      | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | F    | QSPI0_IO0      | I/O | 3      |   |
| W18          | R16          | H10          | VDDIOP1    | GPIO_IO   | PA25    | I/O | -         | -   | A    | FLEXCOM1_IO3   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B    | D3             | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C    | TMS            | I   | 4      |   |
|              |              |              |            |           |         |     |           |     | D    | SPI1_NPCS0     | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | F    | QSPI0_IO1      | I/O | 3      |   |



| .....continued |              |              |            |          |         |     |           |     |                |              |     |        |   |
|----------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
| 361-ball BGA   | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|                |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| U14            | P17          | L10          | VDDIOP1    | GPIO_IO  | PA26    | I/O | -         | -   | A              | FLEXCOM1_IO4 | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D4           | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | NTRST        | I   | 4      |   |
|                |              |              |            |          |         |     |           |     | D              | SPI1_NPCS1   | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | QSPI0_IO2    | I/O | 3      |   |
| M18            | R15          | P14          | VDDIOP1    | GPIO_IO  | PA27    | I/O | -         | -   | A              | TIOA1        | I/O | 2      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D5           | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | SPI0_NPCS2   | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | D              | SPI1_NPCS2   | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | E              | SDMMC1_RSTN  | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | QSPI0_IO3    | I/O | 3      |   |
| U13            | R14          | N12          | VDDIOP1    | GPIO     | PA28    | I/O | -         | -   | A              | TIOB1        | I/O | 2      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D6           | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | SPI0_NPCS3   | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | D              | SPI1_NPCS3   | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | E              | SDMMC1_CMD   | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | CLASSD_L0    | O   | 1      |   |
| U16            | P14          | M12          | VDDIOP1    | GPIO     | PA29    | I/O | -         | -   | A              | TCLK1        | I   | 2      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D7           | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | SPI0_NPCS1   | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | E              | SDMMC1_WP    | I   | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | CLASSD_L1    | O   | 1      |   |
| U12            | R13          | N11          | VDDIOP1    | GPIO     | PA30    | I/O | -         | -   | B              | NWE/NANDWE   | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | C              | SPI0_NPCS0   | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | D              | PWMH0        | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | E              | SDMMC1_CD    | I   | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | CLASSD_L2    | O   | 1      |   |
| U17            | P13          | M11          | VDDIOP1    | GPIO     | PA31    | I/O | -         | -   | B              | NCS3         | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | C              | SPI0_MISO    | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | D              | PWML0        | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | CLASSD_L3    | O   | 1      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type  | Primary |     | Alternate |     | PIO Peripheral |             |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|-----------|---------|-----|-----------|-----|----------------|-------------|-----|--------|---|
|              |              |              |            |           | Signal  | Dir | Signal    | Dir | Func           | Signal      | Dir | IO Set |   |
| C7           | F5           | E6           | VDDIOP0    | GPIO      | PB0     | I/O | -         | -   | B              | A21/NANDALE | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | C              | SPI0_MOSI   | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | PWMH1       | O   | 1      |   |
| A9           | C8           | D6           | VDDIOP0    | GPIO      | PB1     | I/O | -         | -   | B              | A22/NANDCLE | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | C              | SPI0_SPCK   | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | PWML1       | O   | 1      |   |
| A10          | C7           | C6           | VDDIOP0    | GPIO      | PB2     | I/O | -         | -   | B              | NRD/NANDOE  | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | D              | PWMFIO      | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | CLASSD_R0   | O   | 1      |   |
| A11          | B8           | C5           | VDDIOP0    | GPIO      | PB3     | I/O | -         | -   | A              | URXD4       | I   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | D8          | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | IRQ         | I   | 3      |   |
|              |              |              |            |           |         |     |           |     | D              | PWMEXTRG1   | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | F              | CLASSD_R2   | O   | 1      |   |
| A12          | B7           | D5           | VDDIOP0    | GPIO      | PB4     | I/O | -         | -   | A              | UTXD4       | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | D9          | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | FIQ         | I   | 4      |   |
|              |              |              |            |           |         |     |           |     | F              | CLASSD_R3   | O   | 1      |   |
| A7           | A10          | D7           | VDDIOP0    | GPIO_QSPI | PB5     | I/O | -         | -   | A              | TCLK2       | I   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | D10         | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | PWMH2       | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | D              | QSPI1_SCK   | O   | 2      |   |
| B7           | A9           | C8           | VDDIOP0    | GPIO      | PB6     | I/O | -         | -   | A              | TIOA2       | I/O | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | D11         | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | PWML2       | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | D              | QSPI1_CS    | O   | 2      |   |
|              |              |              |            |           |         |     |           |     | F              | GTXER       | O   | 3      |   |

| .....continued |              |              |            |          |         |     |           |     |                |           |     |        |   |
|----------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|-----------|-----|--------|---|
| 361-ball BGA   | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |           |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|                |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal    | Dir | IO Set |   |
| C5             | D5           | D9           | VDDIOP0    | GPIO_IO  | PB7     | I/O | -         | -   | A              | TIOB2     | I/O | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D12       | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | PWMH3     | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | QSPI1_IO0 | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | GRXCK     | I   | 3      |   |
| B8             | E5           | C7           | VDDIOP0    | GPIO_IO  | PB8     | I/O | -         | -   | A              | TCLK3     | I   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D13       | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | PWML3     | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | QSPI1_IO1 | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | GCRS      | I   | 3      |   |
| B6             | C6           | C9           | VDDIOP0    | GPIO_IO  | PB9     | I/O | -         | -   | A              | TIOA3     | I/O | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D14       | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | PWMF1     | I   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | QSPI1_IO2 | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | GCOL      | I   | 3      |   |
| G6             | A8           | F6           | VDDIOP0    | GPIO_IO  | PB10    | I/O | -         | -   | A              | TIOB3     | I/O | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | D15       | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | PWMEXTRG2 | I   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | QSPI1_IO3 | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | GRX2      | I   | 3      |   |
| B5             | A7           | B9           | VDDIOP0    | GPIO     | PB11    | I/O | -         | -   | A              | LCDDAT0   | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A0/NBS0   | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | URXD3     | I   | 3      |   |
|                |              |              |            |          |         |     |           |     | D              | PDMIC_DAT |     | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | GRX3      | I   | 3      |   |
| A6             | B6           | B8           | VDDIOP0    | GPIO     | PB12    | I/O | -         | -   | A              | LCDDAT1   | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A1        | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | UTXD3     | O   | 3      |   |
|                |              |              |            |          |         |     |           |     | D              | PDMIC_CLK |     | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | GTX2      | O   | 3      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type  | Primary |     | Alternate |     | PIO Peripheral |           |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|-----------|---------|-----|-----------|-----|----------------|-----------|-----|--------|---|
|              |              |              |            |           | Signal  | Dir | Signal    | Dir | Func           | Signal    | Dir | IO Set |   |
| C4           | C5           | B7           | VDDIOP0    | GPIO      | PB13    | I/O | -         | -   | A              | LCDDAT2   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | A2        | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | PCK1      | O   | 3      |   |
|              |              |              |            |           |         |     |           |     | F              | GTX3      | O   | 3      |   |
| G4           | A6           | G6           | VDDIOP0    | GPIO_QSPI | PB14    | I/O | -         | -   | A              | LCDDAT3   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | A3        | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | TK1       | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | I2SC1_MCK | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | QSPI1_SCK | O   | 3      |   |
|              |              |              |            |           |         |     |           |     | F              | GTXCK     | I/O | 3      |   |
| H4           | E4           | B5           | VDDIOP0    | GPIO      | PB15    | I/O | -         | -   | A              | LCDDAT4   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | A4        | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | TF1       | I/O | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | I2SC1_CK  | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | QSPI1_CS  | O   | 3      |   |
|              |              |              |            |           |         |     |           |     | F              | GTXEN     | O   | 3      |   |
| A4           | B5           | C4           | VDDIOP0    | GPIO_IO   | PB16    | I/O | -         | -   | A              | LCDDAT5   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | A5        | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | TD1       | O   | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | I2SC1_WS  | I/O | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | QSPI1_IO0 | I/O | 3      |   |
|              |              |              |            |           |         |     |           |     | F              | GRXDV     | I   | 3      |   |
| B3           | C4           | A5           | VDDIOP0    | GPIO_IO   | PB17    | I/O | -         | -   | A              | LCDDAT6   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |           |         |     |           |     | B              | A6        | O   | 1      |   |
|              |              |              |            |           |         |     |           |     | C              | RD1       | I   | 2      |   |
|              |              |              |            |           |         |     |           |     | D              | I2SC1_DI0 | I   | 1      |   |
|              |              |              |            |           |         |     |           |     | E              | QSPI1_IO1 | I/O | 3      |   |
|              |              |              |            |           |         |     |           |     | F              | GRXER     | I   | 3      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| D3           | A5           | B4           | VDDIOP0    | GPIO_IO  | PB18    | I/O | -         | -   | A              | LCDDAT7      | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A7           | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | RK1          | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | I2SC1_DO0    | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | QSPI1_IO2    | I/O | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | GRX0         | I   | 3      |   |
| F4           | B4           | A6           | VDDIOP0    | GPIO_IO  | PB19    | I/O | -         | -   | A              | LCDDAT8      | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A8           | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | RF1          | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOA3        | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | QSPI1_IO3    | I/O | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | GRX1         | I   | 3      |   |
| F2           | A4           | A4           | VDDIOP0    | GPIO     | PB20    | I/O | -         | -   | A              | LCDDAT9      | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A9           | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TK0          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOB3        | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | PCK1         | O   | 4      |   |
|              |              |              |            |          |         |     |           |     | F              | GTX0         | O   | 3      |   |
| F3           | D3           | A3           | VDDIOP0    | GPIO     | PB21    | I/O | -         | -   | A              | LCDDAT10     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A10          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TF0          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TCLK3        | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO2 | I/O | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | GTX1         | O   | 3      |   |
| E4           | C3           | D3           | VDDIOP0    | GPIO     | PB22    | I/O | -         | -   | A              | LCDDAT11     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A11          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TD0          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOA2        | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO1 | I/O | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | GMDC         | O   | 3      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| H2           | B3           | B2           | VDDIOP0    | GPIO     | PB23    | I/O | -         | -   | A              | LCDDAT12     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A12          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | RD0          | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOB2        | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO0 | I/O | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | GMDIO        | I/O | 3      |   |
| A3           | E2           | E3           | VDDIOP0    | GPIO     | PB24    | I/O | -         | -   | A              | LCDDAT13     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A13          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | RK0          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TCLK2        | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO3 | O   | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D10      | I   | 3      |   |
| H1           | A3           | E2           | VDDIOP0    | GPIO     | PB25    | I/O | -         | -   | A              | LCDDAT14     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A14          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | RF0          | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO4 | O   | 3      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D11      | I   | 3      |   |
| G2           | G3           | D4           | VDDIOP0    | GPIO     | PB26    | I/O | -         | -   | A              | LCDDAT15     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A15          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | URXD0        | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | PDMIC_DAT    |     | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D0       | I   | 3      |   |
| H5           | F4           | C3           | VDDIOP0    | GPIO     | PB27    | I/O | -         | -   | A              | LCDDAT16     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A16          | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | UTXD0        | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | PDMIC_CLK    |     | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D1       | I   | 3      |   |

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|----------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
| 361-ball BGA   | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|                |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| J2             | D2           | D2           | VDDIOP0    | GPIO     | PB28    | I/O | -         | -   | A              | LCDDAT17     | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A17          | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | FLEXCOM0_IO0 | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | TIOA5        | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D2       | I   | 3      |   |
| J3             | G8           | B3           | VDDIOP0    | GPIO     | PB29    | I/O | -         | -   | A              | LCDDAT18     | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A18          | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | FLEXCOM0_IO1 | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | TIOB5        | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D3       | I   | 3      |   |
| A2             | C2           | F3           | VDDIOP0    | GPIO     | PB30    | I/O | -         | -   | A              | LCDDAT19     | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A19          | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | FLEXCOM0_IO2 | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | TCLK5        | I   | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D4       | I   | 3      |   |
| J4             | G7           | A2           | VDDIOP0    | GPIO     | PB31    | I/O | -         | -   | A              | LCDDAT20     | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A20          | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | FLEXCOM0_IO3 | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | TWD0         | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D5       | I   | 3      |   |
| T14            | N10          | L13          | VDDIOP1    | GPIO     | PC0     | I/O | -         | -   | A              | LCDDAT21     | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A23          | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | FLEXCOM0_IO4 | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | TWCK0        | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D6       | I   | 3      |   |
| R16            | N11          | H11          | VDDIOP1    | GPIO     | PC1     | I/O | -         | -   | A              | LCDDAT22     | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | A24          | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | C              | CANTX0       | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | SPI1_SPCK    | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | E              | I2SC0_CK     | I/O | 1      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D7       | I   | 3      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |            |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal     | Dir | IO Set |   |
| T15          | N9           | L11          | VDDIOP1    | GPIO     | PC2     | I/O | -         | -   | A              | LCDDAT23   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | A25        | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | CANRX0     | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | SPI1_MOSI  | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | I2SC0_MCK  | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D8     | I   | 3      |   |
| T13          | M10          | F13          | VDDIOP1    | GPIO     | PC3     | I/O | -         | -   | A              | LCDPWM     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | NWAIT      | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TIOA1      | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | SPI1_MISO  | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | I2SC0_WS   | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D9     | I   | 3      |   |
| P16          | N15          | G14          | VDDIOP1    | GPIO     | PC4     | I/O | -         | -   | A              | LCDDISP    | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | NWR1/NBS1  | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TIOB1      | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | SPI1_NPCS0 | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | I2SC0_DI0  | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_PCK    | I   | 3      |   |
| L19          | M16          | J14          | VDDIOP1    | GPIO     | PC5     | I/O | -         | -   | A              | LCDVSYNC   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | NCS0       | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TCLK1      | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | SPI1_NPCS1 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | I2SC0_DO0  | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_VSYNC  | I   | 3      |   |
| R15          | L11          | J13          | VDDIOP1    | GPIO     | PC6     | I/O | -         | -   | A              | LCDHSYNC   | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | NCS1       | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TWD1       | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | SPI1_NPCS2 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_HSYNC  | I   | 3      |   |



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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |            |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal     | Dir | IO Set |   |
| N15          | M15          | F14          | VDDIOP1    | GPIO_CLK | PC7     | I/O | -         | -   | A              | LCDPCK     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | NCS2       | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | TWCK1      | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | SPI1_NPCS3 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | URXD1      | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_MCK    | O   | 3      |   |
| P11          | M13          | K13          | VDDIOP1    | GPIO     | PC8     | I/O | -         | -   | A              | LCDDEN     | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | NANDRDY    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | FIQ        | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | PCK0       | O   | 3      |   |
|              |              |              |            |          |         |     |           |     | E              | UTXD1      | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_FIELD  | I   | 3      |   |
| B2           | B2           | -            | VDDISC     | GPIO     | PC9     | I/O | -         | -   | A              | FIQ        | I   | 3      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTSUCOMP   | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D0     | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOA4      | I/O | 2      |   |
| K5           | G4           | -            | VDDISC     | GPIO     | PC10    | I/O | -         | -   | A              | LCDDAT2    | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTCK       | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D1     | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TIOB4      | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | CANTX0     | O   | 2      |   |
| C2           | A2           | -            | VDDISC     | GPIO     | PC11    | I/O | -         | -   | A              | LCDDAT3    | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTEN       | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D2     | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | TCLK4      | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | CANRX0     | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A0/NBS0    | O   | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |          |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|----------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal   | Dir | IO Set |   |
| D2           | A1           | –            | VDDISC     | GPIO     | PC12    | I/O | –         | –   | A              | LCDDAT4  | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRXDV    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D3   | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | URXD3    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | TK0      | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A1       | O   | 2      |   |
| K2           | B1           | –            | VDDISC     | GPIO     | PC13    | I/O | –         | –   | A              | LCDDAT5  | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRXER    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D4   | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | UTXD3    | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | TF0      | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A2       | O   | 2      |   |
| K6           | G5           | –            | VDDISC     | GPIO     | PC14    | I/O | –         | –   | A              | LCDDAT6  | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRX0     | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D5   | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | TD0      | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A3       | O   | 2      |   |
| B1           | G2           | –            | VDDISC     | GPIO     | PC15    | I/O | –         | –   | A              | LCDDAT7  | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRX1     | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D6   | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | RD0      | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A4       | O   | 2      |   |
| K9           | G6           | –            | VDDISC     | GPIO     | PC16    | I/O | –         | –   | A              | LCDDAT10 | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTX0     | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D7   | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | RK0      | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A5       | O   | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| C1           | C1           | –            | VDDISC     | GPIO     | PC17    | I/O | –         | –   | A              | LCDDAT11     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTX1         | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D8       | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | RF0          | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A6           | O   | 2      |   |
| L9           | G9           | –            | VDDISC     | GPIO     | PC18    | I/O | –         | –   | A              | LCDDAT12     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GMDC         | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D9       | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO2 | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A7           | O   | 2      |   |
| D1           | D1           | –            | VDDISC     | GPIO     | PC19    | I/O | –         | –   | A              | LCDDAT13     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GMDIO        | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D10      | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO1 | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A8           | O   | 2      |   |
| L8           | H4           | –            | VDDISC     | GPIO     | PC20    | I/O | –         | –   | A              | LCDDAT14     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRXCK        | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_D11      | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO0 | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A9           | O   | 2      |   |
| E3           | E1           | –            | VDDISC     | GPIO     | PC21    | I/O | –         | –   | A              | LCDDAT15     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTXER        | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_PCK      | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO3 | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A10          | O   | 2      |   |
| E2           | F1           | –            | VDDISC     | GPIO     | PC22    | I/O | –         | –   | A              | LCDDAT18     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GCRS         | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_VSYNC    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | FLEXCOM3_IO4 | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A11          | O   | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| L7           | H9           | –            | VDDISC     | GPIO     | PC23    | I/O | –         | –   | A              | LCDDAT19     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GCOL         | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_HSYNC    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | A12          | O   | 2      |   |
| E1           | G1           | –            | VDDISC     | GPIO_CLK | PC24    | I/O | –         | –   | A              | LCDDAT20     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRX2         | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_MCK      | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | A13          | O   | 2      |   |
| L4           | H8           | –            | VDDISC     | GPIO     | PC25    | I/O | –         | –   | A              | LCDDAT21     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GRX3         | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | ISC_FIELD    | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | A14          | O   | 2      |   |
| D6           | F7           | –            | VDDIOP2    | GPIO     | PC26    | I/O | –         | –   | A              | LCDDAT22     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTX2         | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | CANTX1       | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | A15          | O   | 2      |   |
| E7           | B10          | –            | VDDIOP2    | GPIO     | PC27    | I/O | –         | –   | A              | LCDDAT23     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | GTX3         | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | PCK1         | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | CANRX1       | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | TWD0         | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A16          | O   | 2      |   |
| J5           | F6           | –            | VDDIOP2    | GPIO     | PC28    | I/O | –         | –   | A              | LCDPWM       | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO0 | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | PCK2         | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | E              | TWCK0        | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A17          | O   | 2      |   |
| C6           | B9           | –            | VDDIOP2    | GPIO     | PC29    | I/O | –         | –   | A              | LCDDISP      | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO1 | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | A18          | O   | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir | IO Set |   |
| D7           | E6           | –            | VDDIOP2    | GPIO     | PC30    | I/O | –         | –   | A              | LCDVSYNC     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO2 | I/O | 1      |   |
|              |              |              |            |          |         |     |           |     | F              | A19          | O   | 2      |   |
| C8           | A11          | –            | VDDIOP2    | GPIO     | PC31    | I/O | –         | –   | A              | LCDHSYNC     | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO3 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | URXD3        | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A20          | O   | 2      |   |
| J7           | E7           | –            | VDDIOP2    | GPIO_CLK | PD0     | I/O | –         | –   | A              | LCDPCK       | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO4 | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | C              | UTXD3        | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | GTSUCOMP     | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A23          | O   | 2      |   |
| D8           | C9           | –            | VDDIOP2    | GPIO     | PD1     | I/O | –         | –   | A              | LCDDEN       | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | D              | GRXCK        | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A24          | O   | 2      |   |
| J6           | D8           | –            | VDDIOP2    | GPIO_CLK | PD2     | I/O | –         | –   | A              | URXD1        | I   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | D              | GTXER        | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_MCK      | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | A25          | O   | 2      |   |
| M3           | J1           | –            | VDDANA     | GPIO_AD  | PD3     | I/O | PTC_X0    | –   | A              | UTXD1        | O   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FIQ          | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | D              | GCRS         | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D11      | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | NWAIT        | I   | 2      |   |
| L6           | H7           | –            | VDDANA     | GPIO_AD  | PD4     | I/O | PTC_X1    | –   | A              | TWD1         | I/O | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | URXD2        | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GCOL         | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D10      | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | NCS0         | O   | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |            |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal     | Dir | IO Set |   |
| L2           | H1           | –            | VDDANA     | GPIO_AD  | PD5     | I/O | PTC_X2    | –   | A              | TWCK1      | I/O | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | UTXD2      | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GRX2       | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D9     | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | NCS1       | O   | 2      |   |
| J1           | J2           | –            | VDDANA     | GPIO_AD  | PD6     | I/O | PTC_X3    | –   | A              | TCK        | I   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | PCK1       | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GRX3       | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D8     | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | NCS2       | O   | 2      |   |
| L5           | H6           | H5           | VDDANA     | GPIO_AD  | PD7     | I/O | PTC_X4    | –   | A              | TDI        | I   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | C              | UTMI_RXVAL | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GTX2       | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D0     | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | NWR1/NBS1  | O   | 2      |   |
| K1           | K3           | J2           | VDDANA     | GPIO_AD  | PD8     | I/O | PTC_X5    | –   | A              | TDO        | O   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | C              | UTMI_RXERR | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GTX3       | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D1     | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | NANDRDY    | I   | 2      |   |
| L3           | J4           | G4           | VDDANA     | GPIO_AD  | PD9     | I/O | PTC_X6    | –   | A              | TMS        | I   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | C              | UTMI_RXACT | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GTXCK      | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D2     | I   | 2      |   |
| L1           | J3           | C2           | VDDANA     | GPIO_AD  | PD10    | I/O | PTC_X7    | –   | A              | NTRST      | I   | 2      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | C              | UTMI_HDIS  | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GTXEN      | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D3     | I   | 2      |   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |                 |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|-----------------|-----|--------|---|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal          | Dir | IO Set |   |
| N3           | K2           | F2           | VDDANA     | GPIO_AD  | PD11    | I/O | PTC_Y0    | -   | A              | TIOA1           | I/O | 3      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | PCK2            | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | C              | UTMI_LS0        | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GRXDV           | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D4          | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_MCK         | O   | 4      |   |
| M7           | K9           | K4           | VDDANA     | GPIO_AD  | PD12    | I/O | PTC_Y1    | -   | A              | TIOB1           | I/O | 3      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO0    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | C              | UTMI_LS1        | O   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GRXER           | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D5          | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D4          | I   | 4      |   |
| N2           | N1           | C1           | VDDANA     | GPIO_AD  | PD13    | I/O | PTC_Y2    | -   | A              | TCLK1           | I   | 3      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO1    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | C              | UTMI_CDRCPSEL0  | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GRX0            | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D6          | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D5          | I   | 4      |   |
| M6           | K5           | H2           | VDDANA     | GPIO_AD  | PD14    | I/O | PTC_Y3    | -   | A              | TCK             | I   | 1      | A, PU, ST   |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO2    | I/O | 2      |   |
|              |              |              |            |          |         |     |           |     | C              | UTMI_CDRCPSEL1  | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GRX1            | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_D7          | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D6          | I   | 4      |   |
| M5           | K8           | G2           | VDDANA     | GPIO_AD  | PD15    | I/O | PTC_Y4    | -   | A              | TDI             | I   | 1      | PIO, I, PU, ST  |
|              |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO3    | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | C              | UTMI_CDRCPDIVEN | I   | 1      |   |
|              |              |              |            |          |         |     |           |     | D              | GTX0            | O   | 2      |   |
|              |              |              |            |          |         |     |           |     | E              | ISC_PCK         | I   | 2      |   |
|              |              |              |            |          |         |     |           |     | F              | ISC_D7          | I   | 4      |   |

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|----------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|-------------------|-----|--------|---|
| 361-ball BGA   | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |                   |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|                |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal            | Dir | IO Set |   |
| M1             | L1           | J1           | VDDANA     | GPIO_AD  | PD16    | I/O | PTC_Y5    | -   | A              | TDO               | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | FLEXCOM4_IO4      | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | C              | UTMI_CDRBISTEN    | I   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | GTX1              | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | E              | ISC_VSYNC         | I   | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D8            | I   | 4      |   |
| M2             | K1           | A1           | VDDANA     | GPIO_AD  | PD17    | I/O | PTC_Y6    | -   | A              | TMS               | I   | 1      | A, PU, ST   |
|                |              |              |            |          |         |     |           |     | C              | UTMI_CDRCPSSELDIV | O   | 1      |   |
|                |              |              |            |          |         |     |           |     | D              | GMDC              | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | E              | ISC_HSYNC         | I   | 2      |   |
| M4             | J7           | G3           | VDDANA     | GPIO_AD  | PD18    | I/O | PTC_Y7    | -   | A              | NTRST             | I   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | D              | GMDIO             | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | E              | ISC_FIELD         | I   | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D10           | I   | 4      |   |
| M8             | L8           | K2           | VDDANA     | GPIO_AD  | PD19    | I/O | AD0       | -   | A              | PCK0              | O   | 1      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | TWD1              | I/O | 3      |   |
|                |              |              |            |          |         |     |           |     | C              | URXD2             | I   | 3      |   |
|                |              |              |            |          |         |     |           |     | E              | I2SC0_CK          | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_D11           | I   | 4      |   |
| N1             | L2           | H1           | VDDANA     | GPIO_AD  | PD20    | I/O | AD1       | -   | A              | TIOA2             | I/O | 3      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | TWCK1             | I/O | 3      |   |
|                |              |              |            |          |         |     |           |     | C              | UTXD2             | O   | 3      |   |
|                |              |              |            |          |         |     |           |     | E              | I2SC0_MCK         | O   | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_PCK           | I   | 4      |   |
| P3             | P1           | G1           | VDDANA     | GPIO_AD  | PD21    | I/O | AD2       | -   | A              | TIOB2             | I/O | 3      | PIO, I, PU, ST  |
|                |              |              |            |          |         |     |           |     | B              | TWD0              | I/O | 4      |   |
|                |              |              |            |          |         |     |           |     | C              | FLEXCOM4_IO0      | I/O | 3      |   |
|                |              |              |            |          |         |     |           |     | E              | I2SC0_WS          | I/O | 2      |   |
|                |              |              |            |          |         |     |           |     | F              | ISC_VSYNC         | I   | 4      |   |



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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail | I/O Type | Primary |     | Alternate |     | PIO Peripheral |              |     | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |                |
|--------------|--------------|--------------|------------|----------|---------|-----|-----------|-----|----------------|--------------|-----|---|----------------|
|              |              |              |            |          | Signal  | Dir | Signal    | Dir | Func           | Signal       | Dir |   | IO Set         |
| N6           | L6           | F1           | VDDANA     | GPIO_AD  | PD22    | I/O | AD3       | -   | A              | TCLK2        | I   | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | B              | TWCK0        | I/O | 4   |                |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM4_IO1 | I/O | 3   |                |
|              |              |              |            |          |         |     |           |     | E              | I2SC0_DI0    | I   | 2   |                |
|              |              |              |            |          |         |     |           |     | F              | ISC_HSYNC    | I   | 4   |                |
| P1           | T1           | E1           | VDDANA     | GPIO_AD  | PD23    | I/O | AD4       | -   | A              | URXD2        | I   | 2   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM4_IO2 | I/O | 3   |                |
|              |              |              |            |          |         |     |           |     | E              | I2SC0_DO0    | O   | 2   |                |
|              |              |              |            |          |         |     |           |     | F              | ISC_FIELD    | I   | 4   |                |
| N8           | L4           | -            | VDDANA     | GPIO_AD  | PD24    | I/O | AD5       | -   | A              | UTXD2        | O   | 2   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM4_IO3 | O   | 3   |                |
| P8           | L5           | -            | VDDANA     | GPIO_AD  | PD25    | I/O | AD6       | -   | A              | SPI1_SPCK    | I/O | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM4_IO4 | O   | 3   |                |
| P2           | R1           | -            | VDDANA     | GPIO_AD  | PD26    | I/O | AD7       | -   | A              | SPI1_MOSI    | I/O | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM2_IO0 | I/O | 2   |                |
| N5           | L7           | -            | VDDANA     | GPIO_AD  | PD27    | I/O | AD8       | -   | A              | SPI1_MISO    | I/O | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | B              | TCK          | I   | 3   |                |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM2_IO1 | I/O | 2   |                |
| N4           | L3           | -            | VDDANA     | GPIO_AD  | PD28    | I/O | AD9       | -   | A              | SPI1_NPCS0   | I/O | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | B              | TDI          | I   | 3   |                |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM2_IO2 | I/O | 2   |                |
| R2           | M2           | -            | VDDANA     | GPIO_AD  | PD29    | I/O | AD10      | -   | A              | SPI1_NPCS1   | O   | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | B              | TDO          | O   | 3   |                |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM2_IO3 | O   | 2   |                |
|              |              |              |            |          |         |     |           |     | D              | TIOA3        | I/O | 3   |                |
|              |              |              |            |          |         |     |           |     | E              | TWD0         | I/O | 3   |                |
| N10          | M9           | -            | VDDANA     | GPIO_AD  | PD30    | I/O | AD11      | -   | A              | SPI1_NPCS2   | O   | 3   | PIO, I, PU, ST |
|              |              |              |            |          |         |     |           |     | B              | TMS          | I   | 3   |                |
|              |              |              |            |          |         |     |           |     | C              | FLEXCOM2_IO4 | O   | 2   |                |
|              |              |              |            |          |         |     |           |     | D              | TIOB3        | I/O | 3   |                |
|              |              |              |            |          |         |     |           |     | E              | TWCK0        | I/O | 3   |                |

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| 361-ball BGA                    | 289-ball BGA                    | 196-ball BGA                              | Power Rail | I/O Type | Primary  |     | Alternate |     | Func | PIO Peripheral |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|---------------------------------|---------------------------------|---|------------|----------|----------|-----|-----------|-----|------|----------------|-----|--------|---|
|                                 |                                 |   |            |          | Signal   | Dir | Signal    | Dir |      | Signal         | Dir | IO Set |   |
| P7                              | M8                              | -   | VDDANA     | GPIO     | PD31     | I/O | -         | -   | A    | ADTRG          | I   | 1      | PIO, I, PU, ST  |
|                                 |                                 |   |            |          |          |     |           |     | B    | NTRST          | I   | 3      |   |
|                                 |                                 |   |            |          |          |     |           |     | C    | IRQ            | I   | 4      |   |
|                                 |                                 |   |            |          |          |     |           |     | D    | TCLK3          | I   | 3      |   |
|                                 |                                 |   |            |          |          |     |           |     | E    | PCK0           | O   | 2      |   |
| M9                              | L9                              | L1  | VDDANA     | -        | ADVREF   | I   | -         | -   | -    | -              | -   | -      | -   |
| G1, H6                          | K4, J5                          | K3, L2                                    | VDDANA     | power    | VDDANA   | I   | -         | -   | -    | -              | -   | -      | -   |
| F1, G5                          | J6, M1                          | L3, K1                                    | GNDANA     | ground   | GNDANA   | I   | -         | -   | -    | -              | -   | -      | -   |
| M12, J10                        | J10, F11                        | K12, F12                                  | VDDIODDR   | DDR      | DDR_VREF | I   | -         | -   | -    | -              | -   | -      | -   |
| C19                             | -                               | -   | VDDIODDR   | DDR      | ZQ       | -   | -         | -   | -    | -              | -   | -      | -   |
| E11, E8, H10, J13, J8, L10, P12 | L10, L14, J8, H10, G12, E11, E8 | F10, E8, E9, E10, G12, H12, J12           | VDDIODDR   | power    | VDDIODDR | I   | -         | -   | -    | -              | -   | -      | -   |
| E10, F8, G10, J9, L11, M13, N12 | K10, M14, J9, G10, H12, E10, F8 | K11, J11, F9, C10, E11, F8, F11, G13, H13 | GNDIODDR   | ground   | GNDIODDR | I   | -         | -   | -    | -              | -   | -      | -   |
| C3, C9, K3, U9, V5, W6, K8      | H2, U3, P7, L12, E9, D7         | G7, H4, D14, E14, L5                      | VDDCORE    | power    | VDDCORE  | I   | -         | -   | -    | -              | -   | -      | -   |
| A1, D9, J11, K4, K7, V9, W1     | E12, F12, J11, K11, K6, K7      | G11, E12, E13, H3, H7, H8, J3             | GNDCORE    | ground   | GNDCORE  | I   | -         | -   | -    | -              | -   | -      | -   |
| B4, D5                          | D4, F3                          | F4, E4                                    | VDDIOP0    | power    | VDDIOP0  | I   | -         | -   | -    | -              | -   | -      | -   |
| A5, D4                          | E3, F2                          | E5, F5                                    | GNDIOP0    | ground   | GNDIOP0  | I   | -         | -   | -    | -              | -   | -      | -   |
| V13, V18                        | N12, P12                        | N9, N10                                   | VDDIOP1    | power    | VDDIOP1  | I   | -         | -   | -    | -              | -   | -      | -   |
| P13, R13, W13, W19              | M12, P11                        | M9, M10                                   | GNDIOP1    | ground   | GNDIOP1  | I   | -         | -   | -    | -              | -   | -      | -   |
| A8                              | D9                              | -   | VDDIOP2    | power    | VDDIOP2  | I   | -         | -   | -    | -              | -   | -      | -   |
| B9                              | D6                              | -   | GNDIOP2    | ground   | GNDIOP2  | I   | -         | -   | -    | -              | -   | -      | -   |
| T7                              | N8                              | J7  | VDDSDMMC   | power    | VDDSDMMC | I   | -         | -   | -    | -              | -   | -      | -   |

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| 361-ball BGA | 289-ball BGA | 196-ball BGA | Power Rail  | I/O Type | Primary     |     | Alternate |     | Func | PIO Peripheral |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--------------|--------------|-------------|----------|-------------|-----|-----------|-----|------|----------------|-----|--------|---|
|              |              |              |             |          | Signal      | Dir | Signal    | Dir |      | Signal         | Dir | IO Set |   |
| T8           | R8           | J8           | GNDSMMMC    | ground   | GNDSMMMC    | I   | -         | -   | -    | -              | -   | -      | -   |
| G3           | H3           | -            | VDDISC      | power    | VDDISC      | I   | -         | -   | -    | -              | -   | -      | -   |
| H3           | H5           | -            | GNDISC      | ground   | GNDISC      | I   | -         | -   | -    | -              | -   | -      | -   |
| U15          | N13          | M13          | VDDFUSE     | power    | VDDFUSE     | I   | -         | -   | -    | -              | -   | -      | -   |
| P9           | R5           | P4           | VDDPLLA     | power    | VDDPLLA     | I   | -         | -   | -    | -              | -   | -      | -   |
| P10          | T5           | L6           | GNDPLLA     | ground   | GNDPLLA     | I   | -         | -   | -    | -              | -   | -      | -   |
| R6           | M4           | K6           | VDDAUDIOPLL | power    | VDDAUDIOPLL | I   | -         | -   | -    | -              | -   | -      | -   |
| N9           | T3           | J6           | GNDDPLL     | ground   | GNDDPLL     | I   | -         | -   | -    | -              | -   | -      | -   |
| P6           | T4           | H6           | GNAUDIOPLL  | ground   | GNAUDIOPLL  | I   | -         | -   | -    | -              | -   | -      | -   |
| W2           | T8           | P1           | VDDAUDIOPLL | -        | CLK_AUDIO   | O   | -         | -   | -    | -              | -   | -      | -   |
| W5           | U9           | N5           | VDDOSC      | -        | XIN         | I   | -         | -   | -    | -              | -   | -      | -   |
| W4           | U8           | P5           | VDDOSC      | -        | XOUT        | O   | -         | -   | -    | -              | -   | -      | -   |
| R10          | N6           | M7           | VDDOSC      | -        | VDDOSC      | I   | -         | -   | -    | -              | -   | -      | -   |
| T11          | P5           | N6           | GNDOSC      | ground   | GNDOSC      | I   | -         | -   | -    | -              | -   | -      | -   |
| R8           | P6           | M6           | VDDUTMII    | power    | VDDUTMII    | I   | -         | -   | -    | -              | -   | -      | -   |
| U7           | R7           | -            | VDDHSIC     | power    | VDDHSIC     | I   | -         | -   | -    | -              | -   | -      | -   |
| R7           | M6           | L7           | GNDUTMII    | ground   | GNDUTMII    | I   | -         | -   | -    | -              | -   | -      | -   |
| W7           | U10          | N7           | VDDUTMII    | -        | HHSDPA      | I/O | -         | -   | -    | -              | -   | -      | -   |
| V7           | T10          | P7           | VDDUTMII    | -        | HHSDMA      | I/O | -         | -   | -    | -              | -   | -      | -   |
| W8           | U11          | N8           | VDDUTMII    | -        | HHSDPB      | I/O | -         | -   | -    | -              | -   | -      | -   |
| V8           | T11          | P8           | VDDUTMII    | -        | HHSDMB      | I/O | -         | -   | -    | -              | -   | -      | -   |
| W9           | T12          | -            | VDDHSIC     | -        | HHSDPDATC   | I/O | -         | -   | -    | -              | -   | -      | -   |
| W10          | U12          | -            | VDDHSIC     | -        | HHSDMSTRC   | I/O | -         | -   | -    | -              | -   | -      | -   |
| T6           | M7           | K7           | VDDUTMIC    | power    | VDDUTMIC    | I   | -         | -   | -    | -              | -   | -      | -   |
| U6           | R6           | G5           | GNDUTMIC    | ground   | GNDUTMIC    | I   | -         | -   | -    | -              | -   | -      | -   |
| V6           | T6           | P6           | VDDUTMIC    | -        | VBG         | I   | -         | -   | -    | -              | -   | -      | -   |
| T2           | R4           | D1           | VDDBU       | -        | TST         | I   | -         | -   | -    | -              | -   | -      | -   |
| W3           | T7           | J5           | VDDBU       | -        | NRST        | I   | -         | -   | -    | -              | -   | -      | -   |
| T3           | R3           | N3           | VDDBU       | -        | JTAGSEL     | I   | -         | -   | -    | -              | -   | -      | -   |
| U2           | R2           | N1           | VDDBU       | -        | WKUP        | I   | -         | -   | -    | -              | -   | -      | -   |
| R1           | N2           | -            | VDDBU       | -        | RXD         | I   | -         | -   | -    | -              | -   | -      | -   |

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| 361-ball BGA | 289-ball BGA                           | 196-ball BGA              | Power Rail               | I/O Type | Primary                  |     | Alternate |     | Func | PIO Peripheral |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--------------|--|---------------------------|--------------------------|----------|--------------------------|-----|-----------|-----|------|----------------|-----|--------|---|
|              |  |                           |                          |          | Signal                   | Dir | Signal    | Dir |      | Signal         | Dir | IO Set |   |
| P4           | T2                                     | B1                        | VDDBU                    | –        | SHDN                     | O   | –         | –   | –    | –              | –   | –      | –   |
| R4           | P3                                     | N4                        | VDDBU                    | –        | PIOBU0                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| R5           | M3                                     | L4                        | VDDBU                    | –        | PIOBU1                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| R3           | P2                                     | M3                        | VDDBU                    | –        | PIOBU2                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| T4           | P4                                     | M4                        | VDDBU                    | –        | PIOBU3                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| U3           | N4                                     | J4                        | VDDBU                    | –        | PIOBU4                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| T5           | M5                                     | M5                        | VDDBU                    | –        | PIOBU5                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| U5           | N5                                     | –                         | VDDBU                    | –        | PIOBU6                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| P5           | N3                                     | –                         | VDDBU                    | –        | PIOBU7                   | I/O | –         | –   | –    | –              | –   | –      | –   |
| V3           | U5                                     | K5                        | VDDBU                    | power    | VDDBU                    | I   | –         | –   | –    | –              | –   | –      | –   |
| U4           | U4                                     | N2                        | GNDBU                    | ground   | GNDBU                    | I   | –         | –   | –    | –              | –   | –      | –   |
| U1           | U2                                     | M1                        | VDDBU                    | –        | XIN32                    | I   | –         | –   | –    | –              | –   | –      | –   |
| T1           | U1                                     | M2                        | VDDBU                    | –        | XOUT32                   | O   | –         | –   | –    | –              | –   | –      | –   |
| V1           | U6                                     | P2                        | VDDBU                    | –        | COMPP                    | I   | –         | –   | –    | –              | –   | –      | –   |
| V2           | U7                                     | P3                        | VDDBU                    | –        | COMPN                    | I   | –         | –   | –    | –              | –   | –      | –   |
| -            | D17                                    | D12                       | DDRM_VDDQ <sup>(2)</sup> | –        | ODT                      | I   | –         | –   | –    | –              | –   | –      | –   |
| -            | A16, B16, C16, D16, E15, G17, J17, L16 | B10, A12, D10, D11        | DDRM_VDD                 | power    | DDRM_VDD                 | I   | –         | –   | –    | –              | –   | –      | –   |
| -            | E16                                    | E7                        | DDRM_VDDL <sup>(2)</sup> | power    | DDRM_VDDL <sup>(2)</sup> | I   | –         | –   | –    | –              | –   | –      | –   |
| -            | F15, G15, H15, J15, K15, L15           | A7, A13, A9, A11, B6, C12 | DDRM_VDDQ <sup>(2)</sup> | power    | DDRM_VDDQ <sup>(2)</sup> | –   | –         | –   | –    | –              | –   | –      | –   |

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| 361-ball BGA   | 289-ball BGA                           | 196-ball BGA                 | Power Rail                | I/O Type | Primary                   |     | Alternate |     | Func | PIO Peripheral |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|--|--|------------------------------|---------------------------|----------|---------------------------|-----|-----------|-----|------|----------------|-----|--------|---|
|  |  |                              |                           |          | Signal                    | Dir | Signal    | Dir |      | Signal         | Dir | IO Set |   |
| A14, A19, B14, B18, C14, C18, D14, D18, E14, E18, F14, F18, G14, G18, H14, H18, N14, N17, N18, P14, P18, R14, R18, T18 | A17, B17, C17, D15, E14, F17, H17, L17 | B14, A8, C11, C14, D8        | DDRM_VSS                  | ground   | DDRM_VSS                  | -   | -         | -   | -    | -              | -   | -      | -   |
| -  | E17                                    | D13                          | DDRM_VSSDL                | ground   | DDRM_VSSDL                | I   | -         | -   | -    | -              | -   | -      | -   |
| -  | F16, G16, H16, J16, K16, K17           | A10, A14, B11, B12, B13, C13 | DDRM_VSSQ                 | ground   | DDRM_VSSQ                 | I   | -         | -   | -    | -              | -   | -      | -   |
| B15, B17, B19, D15, D17, D19, F15, F17, F19, H15, H17, H19, K15, K17, K19, M15, M17, M19, P15, P17, P19, T17, T19      | -                                      | -                            | DDRM_VDD12 <sup>(3)</sup> | power    | DDRM_VDD12 <sup>(3)</sup> | I   | -         | -   | -    | -              | -   | -      | -   |
| B11, B13, D11, D13, K13, K16   | -                                      | -                            | DDRM_VDD18 <sup>(3)</sup> | power    | DDRM_VDD18 <sup>(3)</sup> | I   | -         | -   | -    | -              | -   | -      | -   |

| .....continued   |  |              |            |                   |         |     |           |     |      |                |     |        |   |
|--|--|--------------|------------|-------------------|---------|-----|-----------|-----|------|----------------|-----|--------|---|
| 361-ball BGA   | 289-ball BGA   | 196-ball BGA | Power Rail | I/O Type          | Primary |     | Alternate |     | Func | PIO Peripheral |     |        | Reset State (Signal, Dir, PU, PD, HiZ, ST) <sup>(1)</sup> |
|  |  |              |            |                   | Signal  | Dir | Signal    | Dir |      | Signal         | Dir | IO Set |   |
| A13, A15, A16, A17, A18, B10, B12, B16, C10, C11, C12, C13, C15, C16, C17, D10, D12, D16, E12, E13, E15, E16, E17, E19, E5, E6, E9, F10, F11, F12, F13, F16, F5, F6, F7, F9, G11, G12, G13, G15, G16, G17, G19, G7, G8, G9, H11, H12, H13, H16, H7, H8, H9, J12, J14, J15, J16, J17, J18, J19, K10, K11, K12, K14, L12, L13, L14, L15, L16, M10, M11, M14, N11, N13, N16, N7, R11, R12, R17, T12, T9, U10, U11, U8, V4 | A12, A13, A14, A15, B11, B12, B13, B14, B15, C10, C11, C12, C13, C14, C15, D10, D11, D12, D13, D14, E13, F9, F10, F13, F14, G11, G13, G14, H11, H13, H14, J12, J13, J14, K12, K13, K14, L13, R12, T9 | –            | –          | NC <sup>(4)</sup> | –       | –   | –         | –   | –    | –              | –   | –      | –   |

**Note:**

1. Signal = 'PIO' if GPIO; Dir = Direction; PU = Pull-up; PD = Pull-down; HiZ = High impedance; ST = Schmitt Trigger
2. Refer to the DDR2-SDRAM data sheet for DDRM\_VDDQ and DDRM\_VDDL definitions.  
DDRM\_VDDQ/DDRM\_VDDL = 1.8V ±0.1V.
3. DDRM\_VDD18 stands for VDD1, DDRM\_VDD12 stands for VDD2, refer to the LPDDR2-SDRAM data sheet for VDD1 and VDD2 definitions.
4. These balls are not internally connected, they can be left unconnected, connected to any GND, VDD or to any slowly varying signal to avoid any EMI related issues.

## 7. Memory

The SAMA5D2 SIP is available with 128 Mbits, 512 Mbits or 1 Gbit of DDR2-SDRAM memory, and with 1 Gbit or 2 Gbits of LPDDR2-SDRAM memory. For the features of these memories, see [DDR2-SDRAM Features](#) and [LPDDR2-SDRAM Features](#).

For power consumption, electrical characteristics and timings of these memories, refer to the data sheets referenced below on the manufacturer's website.

**Table 7-1. Memory Data Sheet References**

| Memory Type  | Density  | Manufacturer Packaged PN | Data Sheet Reference Number |
|--------------|----------|--------------------------|-----------------------------|
| DDR2-SDRAM   | 128 Mbit | Winbond W9712G6KB25I     | W9712G6KB                   |
|              | 512 Mbit | Winbond W9751G6KB25I     | W9751G6KB                   |
|              | 1 Gbit   | Winbond W971GG6SB25I     | W971GG6SB                   |
| LPDDR2-SDRAM | 1 Gbit   | apmemory AD2100xxx-      | lpddr2_datasheet_1gb        |
|              | 2 Gbit   | apmemory AD2200xxx-      | lpddr2_datasheet_2gb        |



## 8. Electrical Characteristics

### 8.1 Decoupling

100 nF (min) decoupling capacitors must be added on each power supply pin, as close as possible to the device.

### 8.2 Power Sequences

#### 8.2.1 SAMA5D2 DDR2 SIP

DDRM\_VDD, DDRM\_VDDL and DDRM\_VDDQ power rails must be connected to VDDIODDR (1.8V) on the PCB. Refer to the sections “Power-up Considerations” and “Power-down Considerations” in the *SAMA5D2 Series* data sheet, ref. no. DS60001476, available on [www.microchip.com](http://www.microchip.com).

#### 8.2.2 SAMA5D2 LPDDR2 SIP

The DDRM\_VDD12 power rail must be connected to VDDIODDR (1.2V). The DDRM\_VDD18 power rail must be connected to a 1.8V power supply. For Backup with Self-refresh mode, these power supplies must be maintained.



**Important:** The sections below supersede “Recommended Power-up Sequence”, “Recommended Power-up Sequence”, “Power Supply Sequencing at Backup Mode Entry and Exit” in the *SAMA5D2 Series* data sheet.

---

#### 8.2.2.1 Power-up Considerations

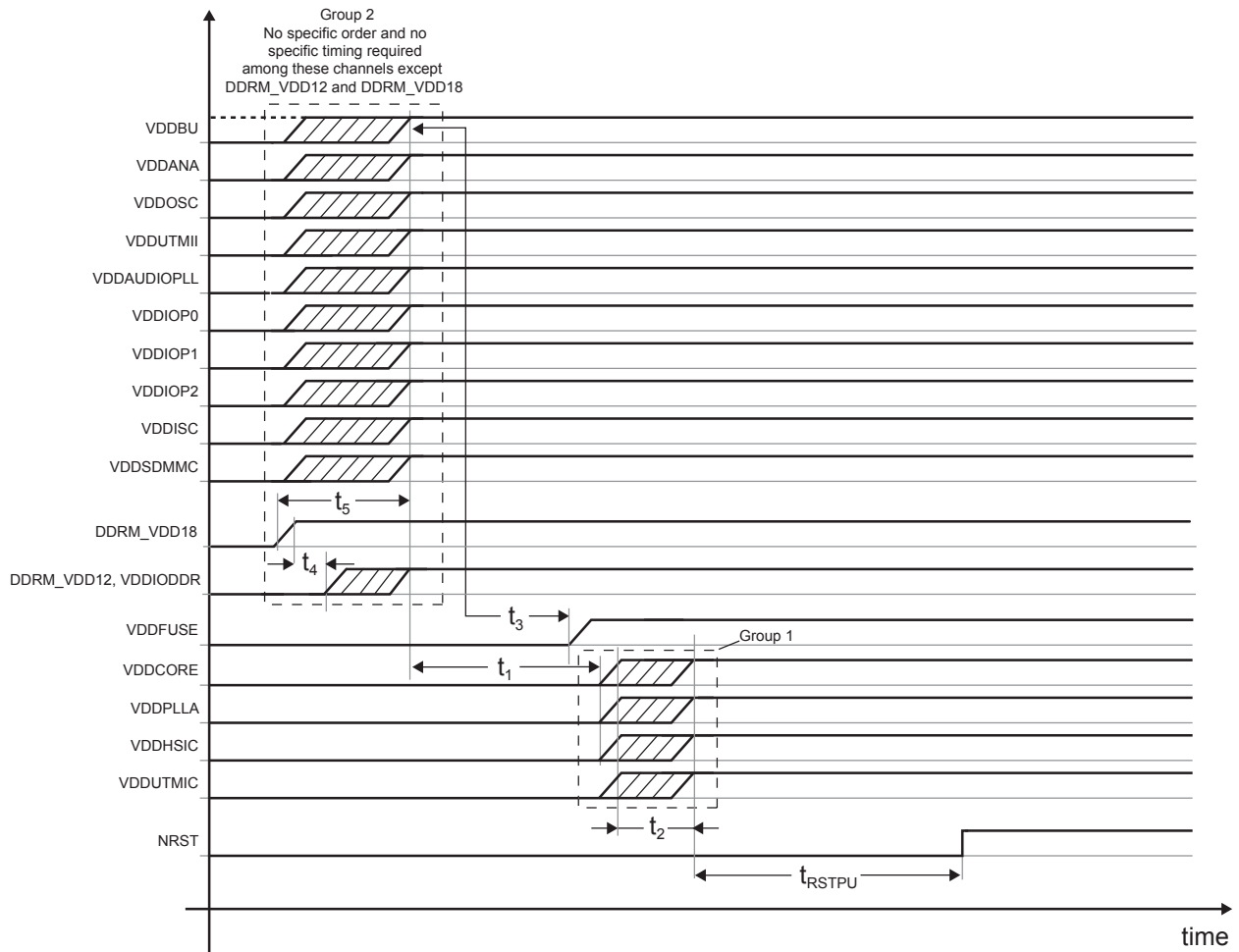
At power-up, from a supply sequencing perspective, the SAMA5D2 LPDDR2 SIP power supply inputs are categorized into two groups:

- Group 1 (core group) contains VDDCORE, VDDUTMIC, VDDHSIC and VDDPLLA.
- Group 2 (periphery group) contains all other power supply inputs except VDDFUSE.

The figure below shows the recommended power-up sequence. Note that:

- VDDBU, when supplied from a battery, is an always-on supply input and is therefore not part of the power supply sequencing. When no backup battery is present in the application, VDDBU is part of Group 2.
- VDDFUSE is the only power supply that may be left unpowered during operation. This is possible if and only if the application does not access the Customer Fuse Matrix in Write mode. It is good practice to turn on VDDFUSE only when the Customer Fuse Matrix is accessed in Write mode, and to turn off VDDFUSE otherwise.

**Figure 8-1. Recommended Power-up Sequence**



**Table 8-1. Power-up Timing Specification**

| Symbol      | Parameter                      | Conditions  | Min | Max | Unit |
|-------------|--------------------------------|---|-----|-----|------|
| $t_1$       | Group 2 to Group 1 delay       | Delay from the last Group 2 established <sup>(1)</sup> supply to the first Group 1 supply turn-on | 0   | –   | ms   |
| $t_2$       | Group 1 delay                  | Delay from the first Group 1 established supply to the last Group 1 established supply            | –   | 1   |      |
| $t_3$       | VDDFUSE to VDDBU delay         | Delay from VDDBU established to VDDFUSE turn-on   | 1   | –   |      |
| $t_4$       | DDRM_VDD18 to DDRM_VDD12 delay | Delay from the DDRM_VDD18 established to DDRM_VDD12 turn-on                                       | 0   | –   |      |
| $t_5$       | LPDDR2 power-on delay          | Delay from DDRM_VDD18 turn-on to DDRM_VDD12 established   | –   | 20  |      |
| $t_{RSTPU}$ | Reset delay at power-up        | From the last established supply to NRST high   | 1   | –   |      |

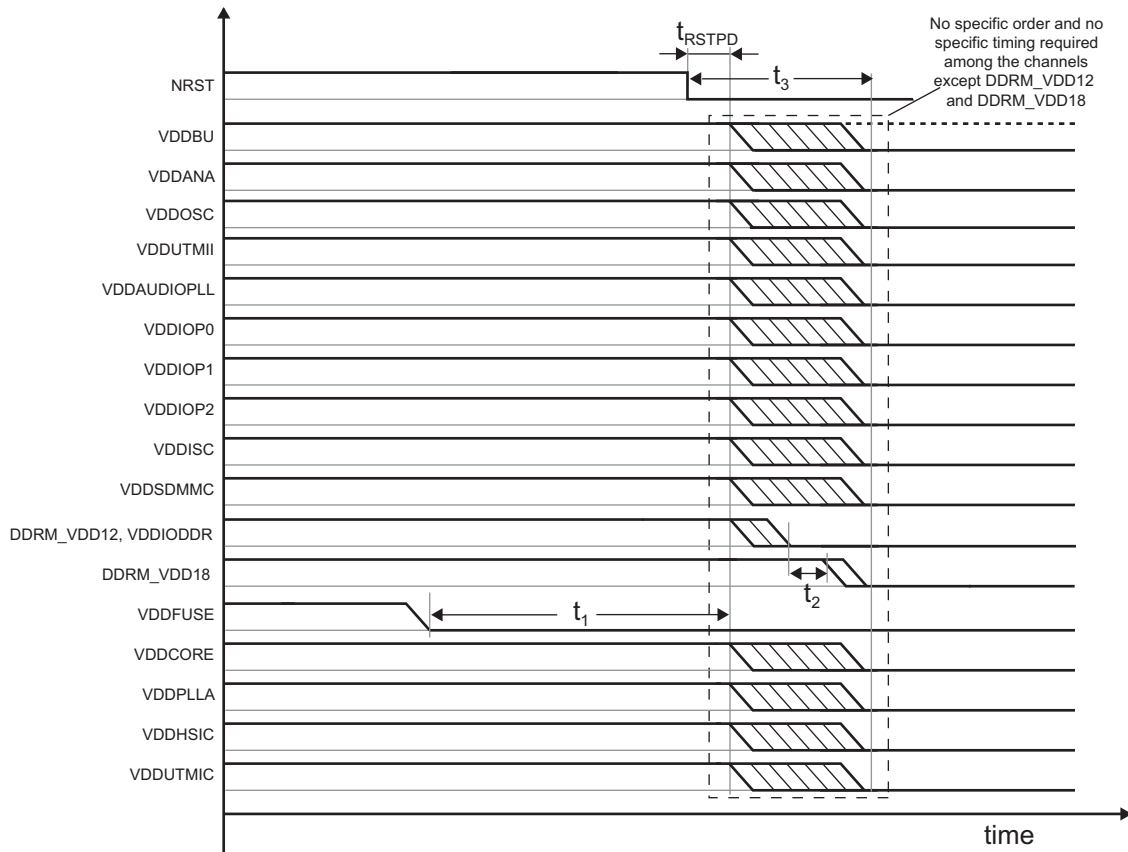
**Note:**

1. An “established” supply refers to a power supply established at 90% of its final value.

### 8.2.2.2 Power-down Considerations

The figure below shows the SAMA5D2 LPDDR2 SIP power-down sequence that starts by asserting the NRST line to 0. Once NRST is asserted, the supply inputs can be immediately shut down without any specific timing or order except for DDRM\_VDD12 and DDRM\_VDD18. VDDDBU may not be shut down if the application uses a backup battery on this supply input. In applications where VDDFUSE is powered, it is mandatory to shut down VDDFUSE prior to removing any other supply. VDDFUSE can be removed before or after asserting the NRST signal.

**Figure 8-2. Recommended Power-down Sequence**



**Table 8-2. Power-down Timing Specification**

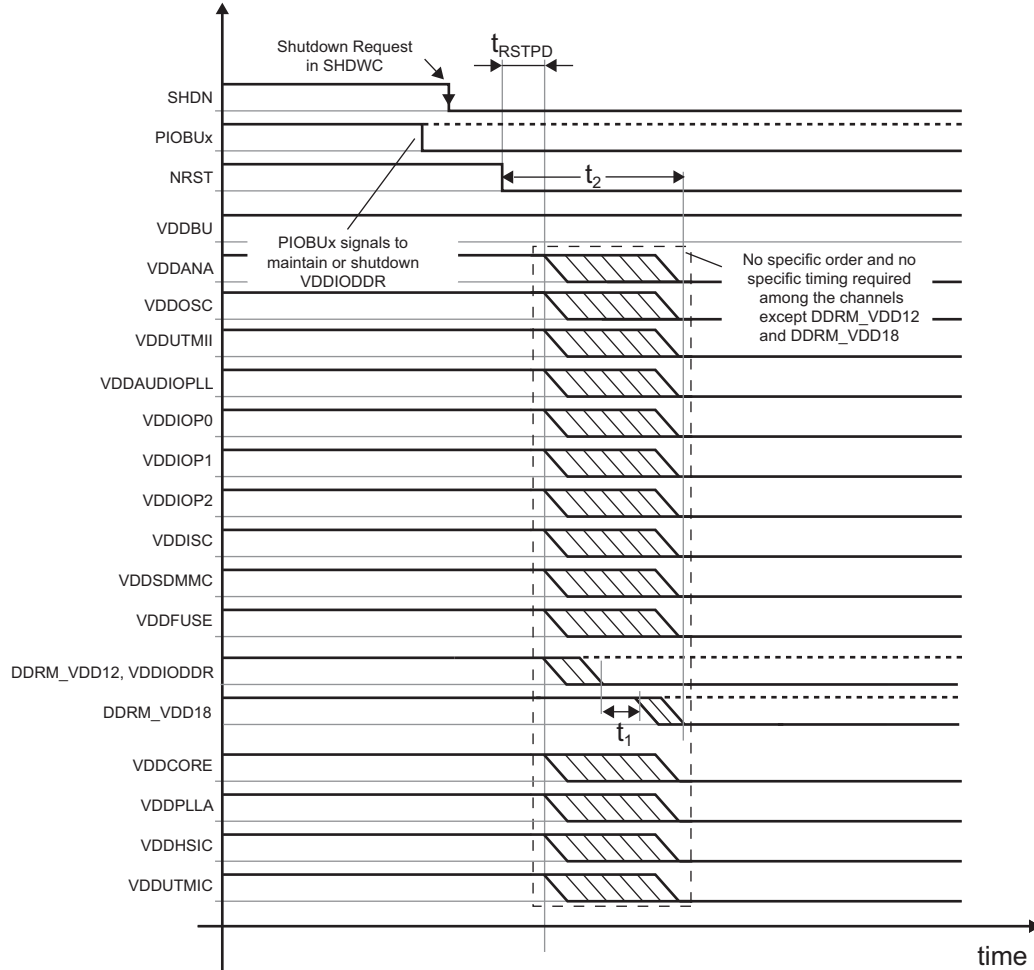
| Symbol      | Parameter                      | Conditions                                     | Min | Max  | Unit |
|-------------|--------------------------------|--|-----|------|------|
| $t_{RSTPD}$ | Reset delay at power-down      | From NRST low to the first supply turn-off     | 0   | –    | ms   |
| $t_1$       | VDDFUSE delay at shut-down     | From VDDFUSE < 1V to the first supply turn-off | 0   | –    |      |
| $t_2$       | DDRM_VDD12 to DDRM_VDD18 delay | From DDRM_VDD12 zeroed to DDRM_VDD18 turn-off  | 0   | –    |      |
| $t_3$       | LPDDR2 power-off delay         | From NRST low to DDRM_VDD18 zeroed             | –   | 2000 |      |

### 8.2.2.3 Backup Mode Entry (Shutdown)

The figure below shows the recommended power-down sequence to place the SAMA5D2 LPDDR2 SIP either in Backup mode or in Backup mode with the LPDDR2 in self-refresh. The SHDN signal, an output of the Shutdown Controller (SHDWC), signals the shutdown request to the power supply. This output is

supplied by VDDBU that is present in Backup mode. Placing the LPDDR2 memory in self-refresh while in Backup mode requires maintaining VDDIODDR, DDRM\_VDD18 and DDRM\_VDD12 as well. One possible way to signal this additional need to the power supply is to position one of the general-purpose I/Os supplied by VDDBU (PIOBUx) in a predefined state.

**Figure 8-3. Recommended Backup Mode Entry (Shutdown)**



**Table 8-3. Shutdown Timing Specification**

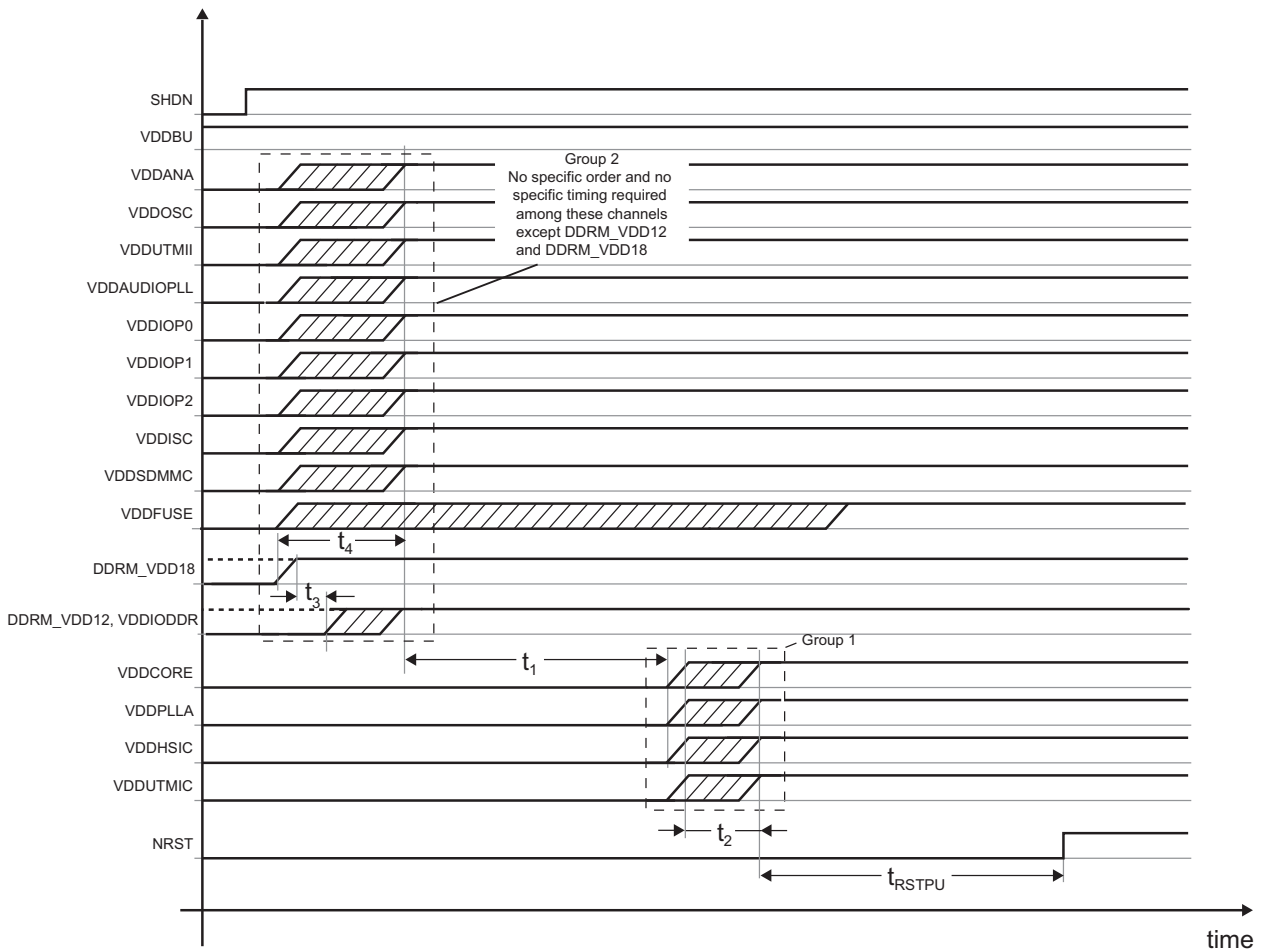
| Symbol      | Parameter                      | Conditions                                    | Min | Max  | Unit |
|-------------|--------------------------------|---|-----|------|------|
| $t_{RSTPD}$ | Reset delay at power-down      | From NRST low to the first supply turn-off    | 0   | –    | ms   |
| $t_1$       | DDRM_VDD12 to DDRM_VDD18 delay | From DDRM_VDD12 zeroed to DDRM_VDD18 turn-off | 0   | –    |      |
| $t_2$       | LPDDR2 power-off delay         | From NRST low to DDRM_VDD18 zeroed            | –   | 2000 |      |

### 8.2.2.4 Backup Mode Exit (Wake-up)

The figure below shows the recommended power-up sequence to wake up the SAMA5D2 LPDDR2 SIP from Backup mode. Upon a wake-up event, the Shutdown Controller toggles its SHDN output back to VDDBU to request the power supply to restart. Except for VDDIODDR, DDRM\_VDD18 and DDRM\_VDD12 which may already be present if the LPDDR2 memory was placed in Self-refresh mode,

this power-up sequence is the same one as presented in the figure “Recommended Power-up Sequence”. In particular, the definitions of Group 1 and Group 2 are the same.

**Figure 8-4. Recommended Backup Mode Exit (Wake-Up)**



**Table 8-4. Wake-up Timing Specification**

| Symbol      | Parameter                      | Conditions  | Min | Max | Unit |
|-------------|--------------------------------|---|-----|-----|------|
| $t_1$       | Group 2 to Group 1 delay       | Delay from the last Group 2 established <sup>(1)</sup> supply to the first Group 1 supply turn-on | 1   | –   | ms   |
| $t_2$       | Group 1 delay                  | Delay from the first Group 1 established supply to the last Group 1 established supply            | –   | 1   |      |
| $t_3$       | DDRM_VDD18 to DDRM_VDD12 delay | Delay from the DDRM_VDD18 established to DDRM_VDD12 turn-on                                       | 0   | –   |      |
| $t_4$       | LPDDR2 power-on delay          | Delay from DDRM_VDD18 turn-on to DDRM_VDD12 established   | –   | 20  |      |
| $t_{RSTPU}$ | Reset delay at power-up        | From the last established supply to NRST high   | 1   | –   |      |

**Note:**

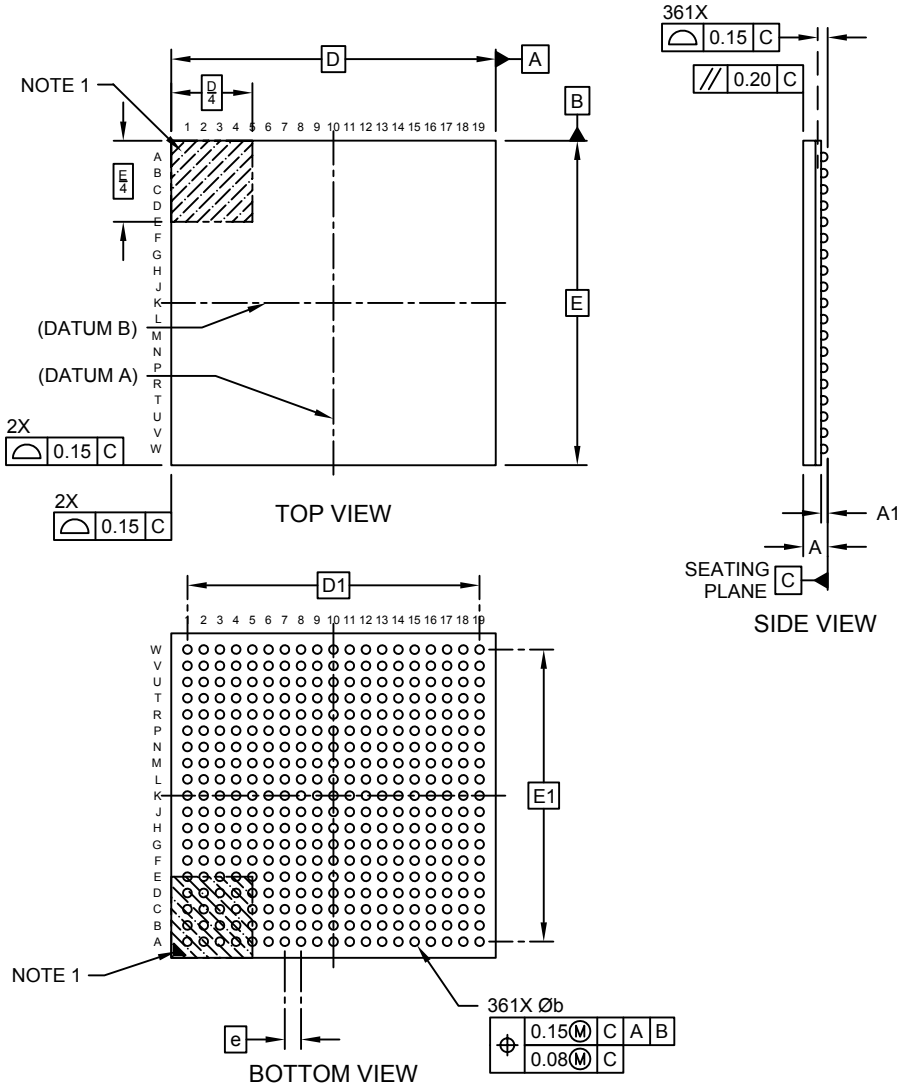
1. An “established” supply refers to a power supply established at 90% of its final value.

## 9. Mechanical Characteristics

### 9.1 361-ball TFBGA

**361-Ball Thin Fine Pitch Ball Grid Array (DYB) - 16x16 mm Body [TFBGA]**  
**Atmel Legacy Global Package Code CEP**

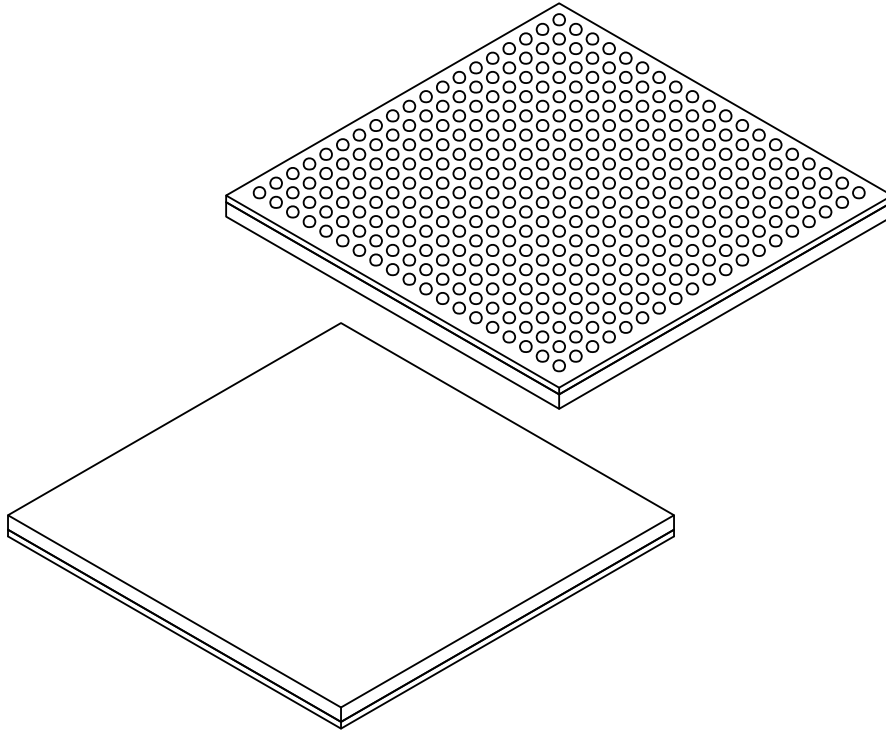
**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



Microchip Technology Drawing C04-21149-DYB Rev A Sheet 1 of 2

### 361-Ball Thin Fine Pitch Ball Grid Array (DYB) - 16x16 mm Body [TFBGA] Atmel Legacy Global Package Code CEP

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



| Dimension Limits    | Units | MILLIMETERS |     |      |
|---------------------|-------|-------------|-----|------|
|                     |       | MIN         | NOM | MAX  |
| Number of Terminals | N     | 361         |     |      |
| Pitch               | e     | 0.80 BSC    |     |      |
| Overall Height      | A     | -           | -   | 1.20 |
| Standoff            | A1    | 0.27        | -   | 0.37 |
| Overall Length      | D     | 16.00 BSC   |     |      |
| Overall Pitch       | D1    | 14.40 BSC   |     |      |
| Overall Width       | E     | 16.00 BSC   |     |      |
| Overall Pitch       | E1    | 14.40 BSC   |     |      |
| Terminal Width      | b     | 0.38        | -   | 0.48 |

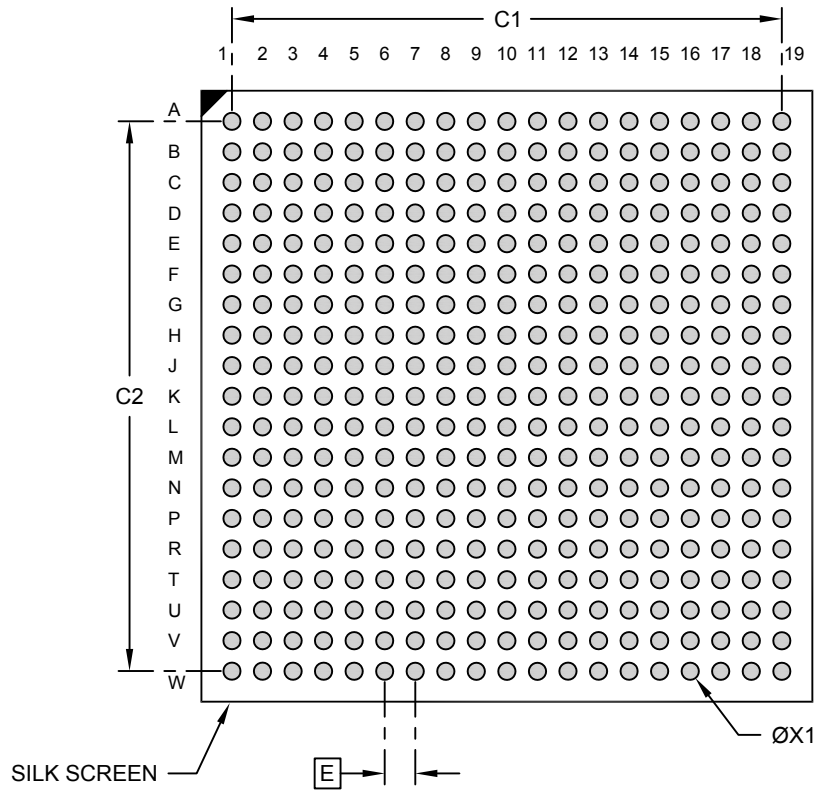
**Notes:**

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensioning and tolerancing per ASME Y14.5M  
 BSC: Basic Dimension. Theoretically exact value shown without tolerances.  
 REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-21149-DYB Rev A Sheet 2 of 2

**361-Ball Thin Fine Pitch Ball Grid Array (DYB) - 16x16 mm Body [TFBGA]  
Atmel Legacy Global Package Code CEP**

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>



**RECOMMENDED LAND PATTERN**

| Dimension               | Units | MILLIMETERS |     |      |
|-------------------------|-------|-------------|-----|------|
|                         |       | MIN         | NOM | MAX  |
| Contact Pitch           | E     | 0.80 BSC    |     |      |
| Contact Pad Spacing     | C1    | 14.40       |     |      |
| Contact Pad Spacing     | C2    | 14.40       |     |      |
| Contact Pad Width (X20) | X1    |             |     | 0.45 |

**Notes:**

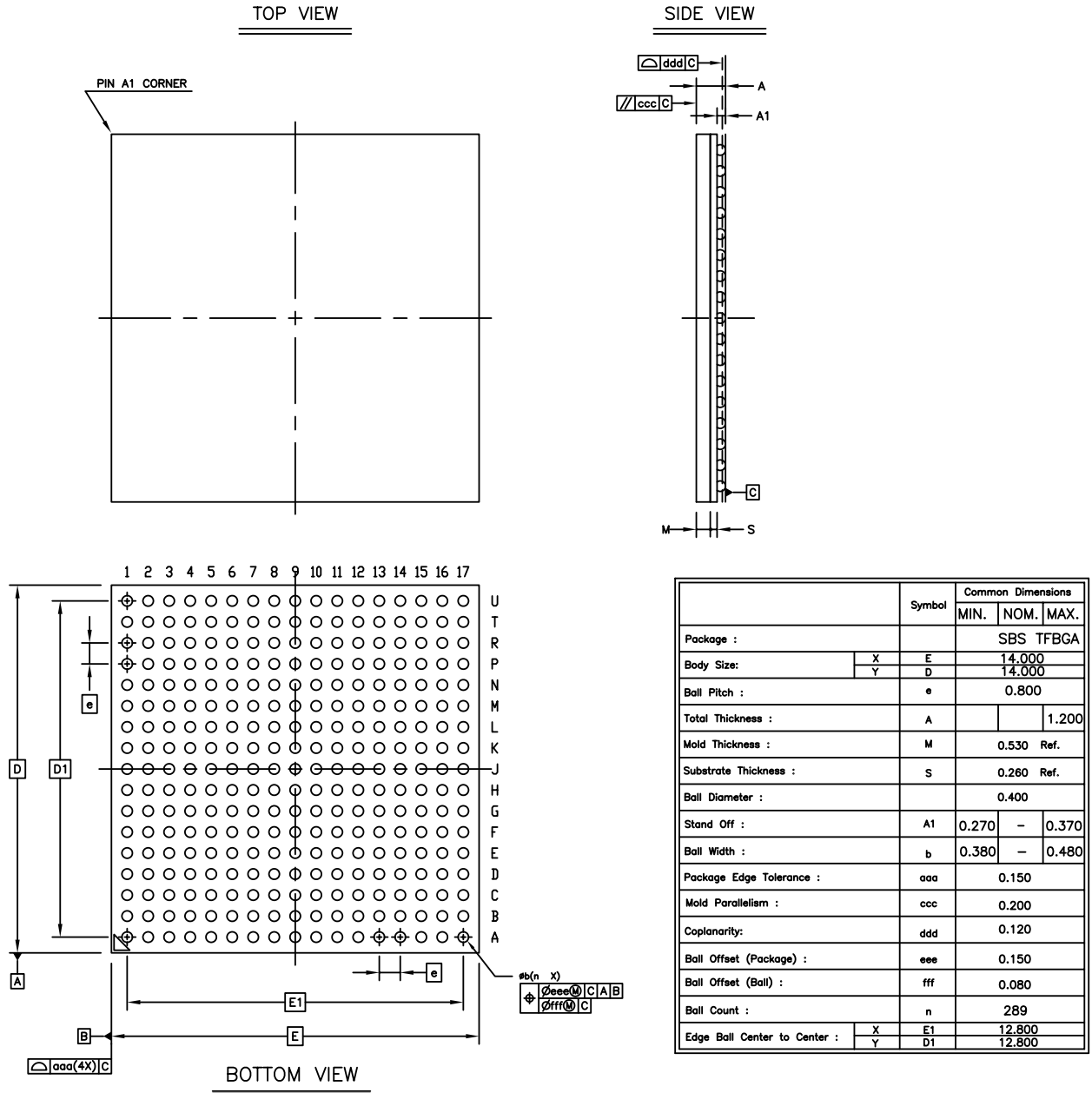
1. Dimensioning and tolerancing per ASME Y14.5M  
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-23149-DYB Rev A



### 9.2 289-ball TFBGA

**Note:** For the most current package drawings, please see the Microchip Packaging Specification located at <http://www.microchip.com/packaging>.



**Table 9-1. 289-ball TFBGA Package Characteristics**

|                            |   |
|----------------------------|---|
| Moisture Sensitivity Level | 3 |
|----------------------------|---|

**Table 9-2. Device and 289-ball TFBGA Package Weight**

| Device                   | Weight (mg) |
|--------------------------|-------------|
| ATSAMA5D27C-D5M (512 Mb) | 390         |

| .....continued           |             |
|--------------------------|-------------|
| Device                   | Weight (mg) |
| ATSAMA5D28C-D1G (1 Gbit) | 400         |

**Table 9-3. Package Reference**

|                          |    |
|--------------------------|----|
| JEDEC Drawing Reference  | NA |
| J-STD-609 Classification | e8 |

**Table 9-4. 289-ball TFBGA Package Information**

|                        |                     |
|------------------------|---------------------|
| Ball Land              | 0.450 mm $\pm$ 0.05 |
| Nominal Ball Diameter  | 0.4 mm              |
| Solder Mask Opening    | 0.350 mm $\pm$ 0.05 |
| Solder Mask Definition | SMD                 |
| Solder                 | OSP                 |

### 9.3 196-ball TFBGA

For mechanical characteristics of the 196-ball TFBGA package, refer to the *SAMA5D2 Series* data sheet, ref. no. DS60001476, available on [www.microchip.com](http://www.microchip.com).

**Note:** The weight of the SAMA5D2 SIP is not the same as the weight of SAMA5D2. The SIP weight is given below:

**Table 9-5. Device and 196-ball TFBGA Package Weight**

| Device                    | Weight (mg) |
|---------------------------|-------------|
| ATSAMA5D225C-D1M (128 Mb) | 240         |

## 10. Ordering Information

Table 10-1. Ordering Information

| Ordering Code        | MRL | Package | Carrier Type | Operating Temperature Range |
|----------------------|-----|---------|--------------|-----------------------------|
| ATSAMA5D225C-D1M-CU  | C   | BGA196  | Tray         | -40°C to +85°C              |
| ATSAMA5D225C-D1M-CUR |     |         | Tape & Reel  |                             |
| ATSAMA5D27C-D5M-CU   |     | BGA289  | Tray         |                             |
| ATSAMA5D27C-D5M-CUR  |     |         | Tape & Reel  |                             |
| ATSAMA5D27C-D1G-CU   |     |         | Tray         |                             |
| ATSAMA5D27C-D1G-CUR  |     |         | Tape & Reel  |                             |
| ATSAMA5D28C-D1G-CU   |     |         | Tray         |                             |
| ATSAMA5D28C-D1G-CUR  |     |         | Tape & Reel  |                             |
| ATSAMA5D27C-LD1G-CU  |     | BGA361  | Tray         |                             |
| ATSAMA5D27C-LD1G-CUR |     |         | Tape & Reel  |                             |
| ATSAMA5D27C-LD2G-CU  |     |         | Tray         |                             |
| ATSAMA5D27C-LD2G-CUR |     |         | Tape & Reel  |                             |
| ATSAMA5D28C-LD1G-CU  |     |         | Tray         |                             |
| ATSAMA5D28C-LD1G-CUR |     |         | Tape & Reel  |                             |
| ATSAMA5D28C-LD2G-CU  |     |         | Tray         |                             |
| ATSAMA5D28C-LD2G-CUR |     |         | Tape & Reel  |                             |

## 11. Revision History

### 11.1 DS60001484B - 11/2018

| Changes  |
|--|
| Added 1 Gbit and 2 Gbit LPDDR2 memory options. Added 361-ball TFBGA package option and mechanical drawing. |
| <a href="#">Pinout</a> : added PTC signals.  |
| Added section <a href="#">Electrical Characteristics</a> .   |

### 11.2 DS60001484A - 09/2017

| Changes      |
|--------------|
| First issue. |

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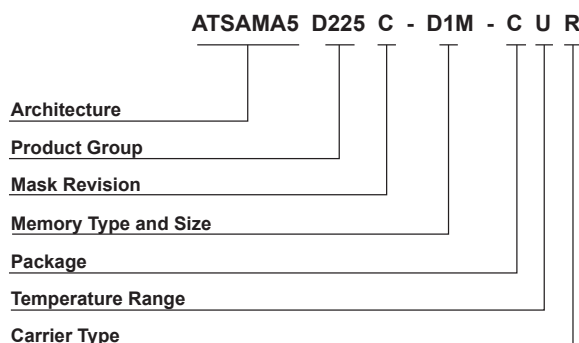
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|                       |         |  |
|-----------------------|---------|--|
| Architecture:         | ATSAMA5 | = Arm Cortex-A5 CPU  |
| Product Group:        | D225    | = 196-ball general-purpose microprocessor family             |
|                       | D27     | = 289-ball or 361-ball general-purpose microprocessor family |
|                       | D28     | = 289-ball or 361-ball general-purpose microprocessor family |
| Memory Type and Size: | D1M     | = 128-Mbit DDR2 SDRAM  |
|                       | D5M     | = 512-Mbit DDR2 SDRAM  |
|                       | D1G     | = 1-Gigabit DDR2 SDRAM                                       |
|                       | LD1G    | = 1-Gigabit LPDDR2 SDRAM                                     |
|                       | LD2G    | = 2-Gigabit LPDDR2 SDRAM                                     |
| Mask Revision:        | C       |  |
| Package:              | C       | = BGA  |
| Temperature Range:    | U       | = -40°C to +85°C (Industrial)                                |
| Carrier Type:         | Blank   | = Standard packaging (tray)                                  |
|                       | R       | = Tape and Reel  |

Examples:

- **ATSAMA5D225C-D1M-CU** = ARM Cortex-A5 general-purpose microprocessor, 128-Mbit DDR2 SDRAM, 196-ball, Industrial temperature, BGA Package.

**Note:** Tape and Reel identifier only appears in the catalog part number description. This identifier is used for ordering purposes and is not printed on the device package

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Microchip received ISO/TS-16949:2009 certification for its worldwide headquarters, design and wafer fabrication facilities in Chandler and Tempe, Arizona; Gresham, Oregon and design centers in California and India. The Company's quality system processes and procedures are for its PIC<sup>®</sup> MCUs and dsPIC<sup>®</sup> DSCs, KEELOQ<sup>®</sup> code hopping devices, Serial EEPROMs, microperipherals, nonvolatile memory and analog products. In addition, Microchip's quality system for the design and manufacture of development systems is ISO 9001:2000 certified.



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