

4.5V to 18V Input, 3-A Synchronous Step-Down Converter with Eco-Mode™

Check for Samples: [TPS54329E](#)

FEATURES

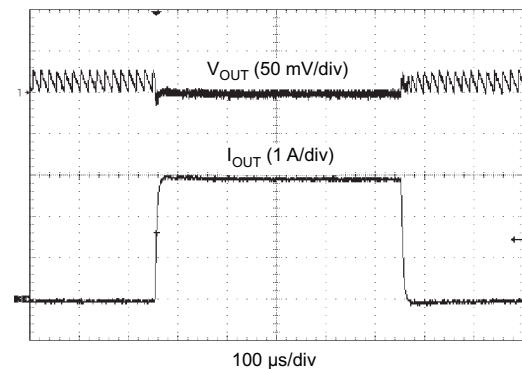
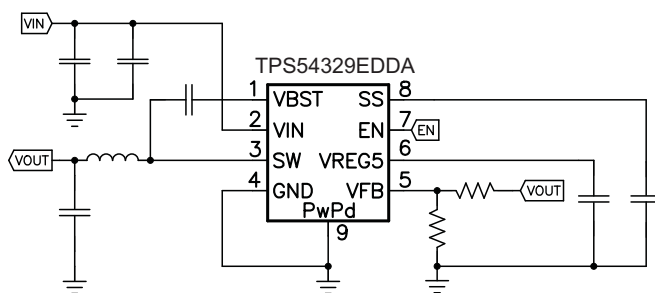
- **D-CAP2™ Mode Enables Fast Transient Response**
- **Low Output Ripple and Allows Ceramic Output Capacitor**
- **Wide V_{IN} Input Voltage Range: 4.5 V to 18 V**
- **Output Voltage Range: 0.76 V to 7.0 V**
- **Highly Efficient Integrated FETs Optimized for Lower Duty Cycle Applications**
 - 100 mΩ (High Side) and 74 mΩ (Low Side)
- **High Efficiency, less than 10 μA at shutdown**
- **High Initial Bandgap Reference Accuracy**
- **Adjustable Soft Start**
- **Pre-Biased Soft Start**
- **650-kHz Switching Frequency (f_{sw})**
- **Cycle By Cycle Over Current Limit**
- **Auto-Skip Eco-mode™ for High Efficiency at Light Load**

APPLICATIONS

- **Wide Range of Applications for Low Voltage System**
 - Digital TV Power Supply
 - High Definition Blu-ray Disc™ Players
 - Networking Home Terminal
 - Digital Set Top Box (STB)

DESCRIPTION

The TPS54329E is an adaptive on-time D-CAP2™ mode synchronous buck converter. The TPS54329E enables system designers to complete the suite of various end-equipment power bus regulators with a cost effective, low component count, low standby current solution. The main control loop for the TPS54329E uses the D-CAP2™ mode control that provides a fast transient response with no external compensation components. The adaptive on-time control supports seamless transition between PWM mode at higher load conditions and Eco-mode™ operation at light load conditions. Eco-mode™ allows the TPS54329E to maintain high efficiency during lighter load conditions. The TPS54329E also has a proprietary circuit that enables the device to adopt to both low equivalent series resistance (ESR) output capacitors, such as POSCAP or SP-CAP, and ultra-low ESR ceramic capacitors. The device operates from 4.5-V to 18-V V_{IN} input. The output voltage can be programmed between 0.76 V and 7 V. The device also features an adjustable soft start time. The TPS54329E is available in the 8-pin DDA package, and designed to operate from -40°C to 85°C .



G006



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

D-CAP2, Eco-mode are trademarks of Texas Instruments.
Blu-ray Disc is a trademark of Blu-ray Disc Association.

PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

Copyright © 2011–2012, Texas Instruments Incorporated

TPS54329E

SLVSAZ5A – SEPTEMBER 2011 – REVISED MARCH 2012

www.ti.com



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ORDERING INFORMATION⁽¹⁾

| T _A | PACKAGE ⁽²⁾ ⁽³⁾ | ORDERABLE PART NUMBER | PIN | TRANSPORT MEDIA |
|----------------|---------------------------------------|-----------------------|-----|-----------------|
| -40°C to 85°C | DDA | TPS54329EDDA | 8 | Tube |
| | | TPS54329EDDAR | | Tape and Reel |

- (1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
 (2) Package drawings, thermal data, and symbolization are available at www.ti.com/packaging.
 (3) All package options have Cu NIPDAU lead/ball finish.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

| | | VALUE | | UNIT |
|--|----------------------------|-------|-----|------|
| | | MIN | MAX | |
| Input voltage range | VIN, EN | -0.3 | 20 | V |
| | VBST | -0.3 | 26 | |
| | VBST (10 ns transient) | -0.3 | 28 | |
| | VBST (vs SW) | -0.3 | 6.5 | |
| | VFB, SS | -0.3 | 6.5 | |
| | SW | -2 | 20 | |
| | SW (10 ns transient) | -3 | 22 | |
| Output voltage range | VREG5 | -0.3 | 6.5 | V |
| | GND | -0.3 | 0.3 | |
| Voltage from GND to thermal pad, V _{diff} | | -0.2 | 0.2 | V |
| Electrostatic discharge | Human Body Model (HBM) | | 2 | kV |
| | Charged Device Model (CDM) | | 500 | V |
| Operating junction temperature, T _J | | -40 | 150 | °C |
| Storage temperature, T _{stg} | | -55 | 150 | |

- (1) Stresses beyond those listed under *absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *recommended operating conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

THERMAL INFORMATION

| THERMAL METRIC ⁽¹⁾ | | TPS54329E | UNITS |
|-------------------------------|--|--------------|-------|
| | | DDA (8 PINS) | |
| θ _{JA} | Junction-to-ambient thermal resistance | 42.1 | °C/W |
| θ _{JCtop} | Junction-to-case (top) thermal resistance | 50.9 | |
| θ _{JB} | Junction-to-board thermal resistance | 31.8 | |
| ψ _{JT} | Junction-to-top characterization parameter | 5 | |
| ψ _{JB} | Junction-to-board characterization parameter | 13.5 | |
| θ _{JCbot} | Junction-to-case (bottom) thermal resistance | 7.1 | |

- (1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](http://www.ti.com/lit/zip/spra953).

RECOMMENDED OPERATING CONDITIONS

over operating free-air temperature range, (unless otherwise noted)

| | | | MIN | MAX | UNIT |
|-----------------|--------------------------------|------------------------|------|-----|------|
| V _{IN} | Supply input voltage range | | 4.5 | 18 | V |
| V _I | Input voltage range | VBST | -0.1 | 24 | V |
| | | VBST (10 ns transient) | -0.1 | 27 | |
| | | VBST(vs SW) | -0.1 | 5.7 | |
| | | SS | -0.1 | 5.7 | |
| | | EN | -0.1 | 18 | |
| | | VFB | -0.1 | 5.5 | |
| | | SW | -1.8 | 18 | |
| | | SW (10 ns transient) | -3 | 21 | |
| | | GND | -0.1 | 0.1 | |
| V _O | Output voltage range | VREG5 | -0.1 | 5.7 | V |
| I _O | Output Current range | I _{VREG5} | 0 | 10 | mA |
| T _A | Operating free-air temperature | | -40 | 85 | °C |
| T _J | Operating junction temperature | | -40 | 150 | °C |

ELECTRICAL CHARACTERISTICS

over operating free-air temperature range, V_{IN} = 12 V (unless otherwise noted)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|--|---|-----|-----|------|------|
| SUPPLY CURRENT | | | | | | |
| I _{VIN} | Operating - non-switching supply current | V _{IN} current, T _A = 25°C, EN = 5 V, V _{F_B} = 0.8 V | | 800 | 1200 | μA |
| I _{VINSDN} | Shutdown supply current | V _{IN} current, T _A = 25°C, EN = 0 V | | 4.3 | 10 | μA |
| LOGIC THRESHOLD | | | | | | |
| V _{EN} | EN high-level input voltage | EN | 1.6 | | | V |
| | EN low-level input voltage | EN | | | 0.45 | V |
| R _{EN} | EN pin resistance to GND | V _{EN} = 12 V | 220 | 440 | 880 | kΩ |
| V_{F_B} VOLTAGE AND DISCHARGE RESISTANCE | | | | | | |
| V _{F_B} TH | V _{F_B} threshold voltage | T _A = 25°C, V _O = 1.05 V, I _O = 10 mA, Eco-mode™ operation | | 773 | | mV |
| | | T _A = 25°C, V _O = 1.05 V, continuous mode operation | 749 | 765 | 781 | mV |
| I _{V_{F_B}} | V _{F_B} input current | V _{F_B} = 0.8 V, T _A = 25°C | | 0 | ±0.1 | μA |
| V_{REG5} OUTPUT | | | | | | |
| V _{V_{REG5}} | V _{REG5} output voltage | T _A = 25°C, 6.0 V < V _{IN} < 18 V, 0 < I _{V_{REG5}} < 5 mA | | 5.5 | | V |
| I _{V_{REG5}} | Output current | V _{IN} = 6 V, V _{REG5} = 4.0 V, T _A = 25°C ⁽¹⁾ | | 60 | | mA |
| MOSFET | | | | | | |
| R _{DS(on)} | High side switch resistance | 25°C, V _{BST} - SW = 5.5 V ⁽¹⁾ | | 100 | | mΩ |
| | Low side switch resistance | 25°C ⁽¹⁾ | | 74 | | mΩ |
| CURRENT LIMIT | | | | | | |
| I _{o_{cl}} | Current limit | L out = 1.5 μH ⁽¹⁾ | 3.5 | 4.2 | 5.7 | A |

(1) Not production tested.

TPS54329E

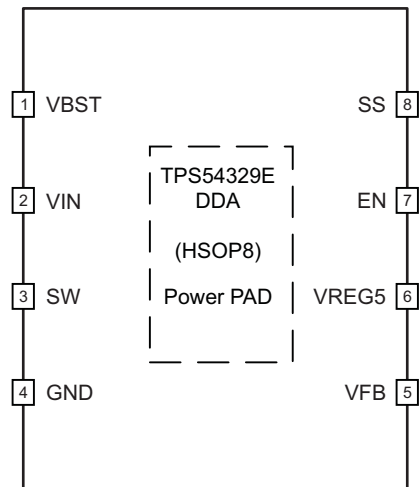
SLVSAZ5A – SEPTEMBER 2011 – REVISED MARCH 2012

www.ti.com
ELECTRICAL CHARACTERISTICS (continued)

 over operating free-air temperature range, $V_{IN} = 12\text{ V}$ (unless otherwise noted)

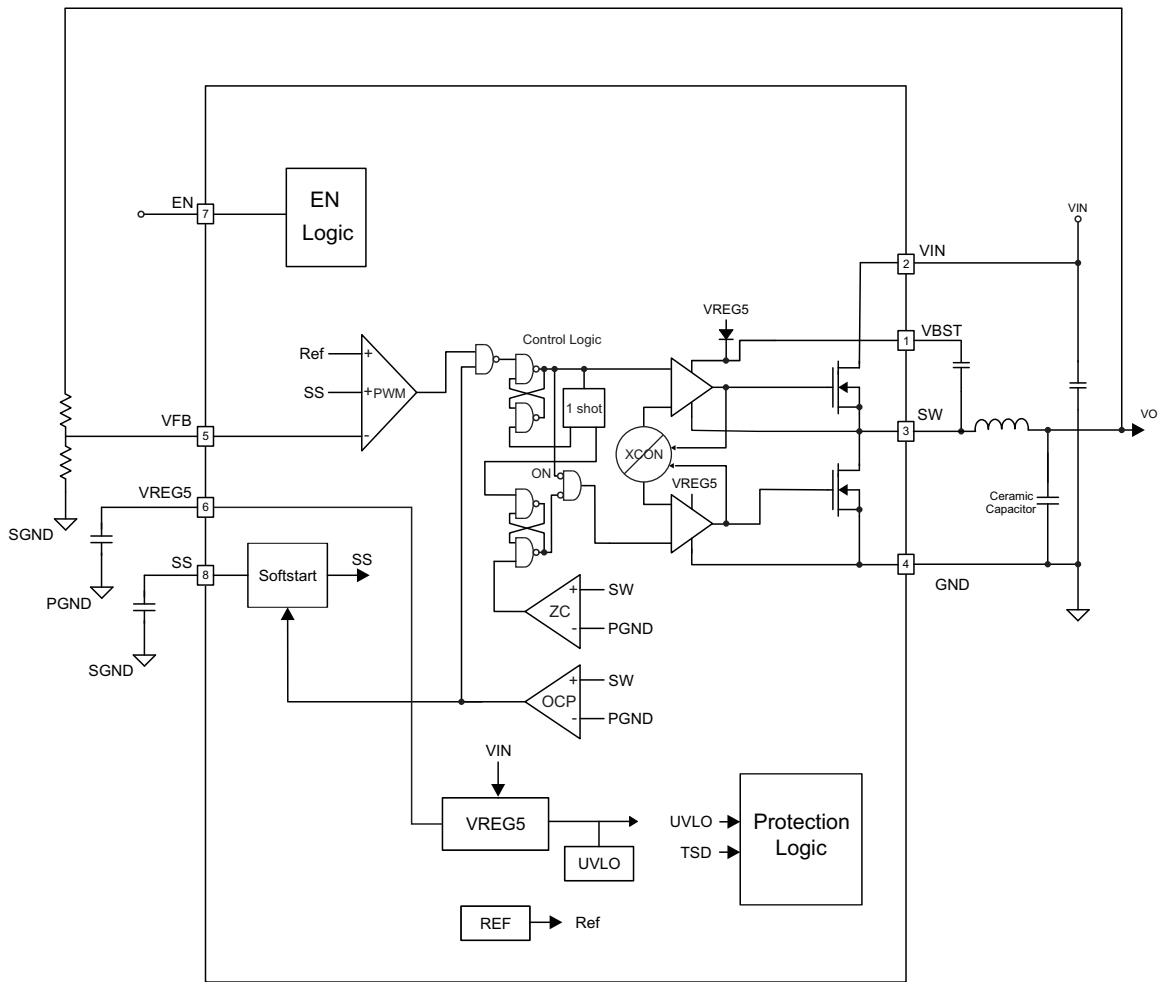
| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|------------------------------|----------------------------|--|------|-----|-----|------|
| THERMAL SHUTDOWN | | | | | | |
| T_{SDN} | Thermal shutdown threshold | Shutdown temperature ⁽²⁾ | 165 | | | °C |
| | | Hysteresis ⁽²⁾ | 35 | | | |
| ON-TIME TIMER CONTROL | | | | | | |
| t_{ON} | On time | $V_{IN} = 12\text{ V}$, $V_O = 1.05\text{ V}$ | 150 | | | ns |
| $t_{OFF(MIN)}$ | Minimum off time | $T_A = 25^\circ\text{C}$, $V_{FB} = 0.7\text{ V}^{(2)}$ | 260 | | | ns |
| SOFT START | | | | | | |
| I_{SS} | SS charge current | $V_{SS} = 1\text{ V}$ | 4.2 | 6.0 | 7.8 | μA |
| | SS discharge current | $V_{SS} = 0.5\text{ V}$ | 0.1 | 0.2 | | mA |
| UVLO | | | | | | |
| UVLO | UVLO threshold | Wake up V_{REG5} voltage | 3.75 | | | V |
| | | Hysteresis V_{REG5} voltage | 0.33 | | | |

(2) Not production tested.

DEVICE INFORMATION
**DDA PACKAGE
(TOP VIEW)**

PIN FUNCTIONS

| PIN | | DESCRIPTION |
|---------------------|-----------|---|
| NAME | NO. | |
| VBST | 1 | Supply input for the high-side FET gate drive circuit. Connect 0.1 μ F capacitor between VBST and SW pins. An internal diode is connected between VREG5 and VBST. |
| VIN | 2 | Input voltage supply pin. |
| SW | 3 | Switch node connection between high-side NFET and low-side NFET. |
| GND | 4 | Ground pin. Power ground return for switching circuit. Connect sensitive SS and VFB returns to GND at a single point. |
| VFB | 5 | Converter feedback input. Connect to output voltage with feedback resistor divider. |
| VREG5 | 6 | 5.5 V power supply output. A capacitor (typical 0.47 μ F) should be connected to GND. VREG5 is not active when EN is low. |
| EN | 7 | Enable input control. EN is active high and must be pulled up to enable the device. |
| SS | 8 | Soft-start control. An external capacitor should be connected to GND. |
| Exposed Thermal Pad | Back side | Thermal pad of the package. Must be soldered to achieve appropriate dissipation. Must be connected to GND. |

FUNCTIONAL BLOCK DIAGRAM



OVERVIEW

The TPS54329E is a 3 A synchronous step-down (buck) converter with two integrated N-channel MOSFETs. It operates using D-CAP2™ mode control. The fast transient response of D-CAP2™ control reduces the output capacitance required to meet a specific level of performance. Proprietary internal circuitry allows the use of low ESR output capacitors including ceramic and special polymer types.

DETAILED DESCRIPTION

PWM Operation

The main control loop of the TPS54329E is an adaptive on-time pulse width modulation (PWM) controller that supports a proprietary D-CAP2™ mode control. D-CAP2™ mode control combines constant on-time control with an internal compensation circuit for pseudo-fixed frequency and low external component count configuration with both low ESR and ceramic output capacitors. It is stable even with virtually no ripple at the output.

At the beginning of each cycle, the high-side MOSFET is turned on. This MOSFET is turned off after internal one shot timer expires. This one shot is set by the converter input voltage, VIN, and the output voltage, VO, to maintain a pseudo-fixed frequency over the input voltage range, hence it is called adaptive on-time control. The one-shot timer is reset and the high-side MOSFET is turned on again when the feedback voltage falls below the reference voltage. An internal ramp is added to reference voltage to simulate output ripple, eliminating the need for ESR induced output ripple from D-CAP2™ mode control.

PWM Frequency and Adaptive On-Time Control

TPS54329E uses an adaptive on-time control scheme and does not have a dedicated on board oscillator. The TPS54329E runs with a pseudo-constant frequency of 650 kHz by using the input voltage and output voltage to set the on-time one-shot timer. The on-time is inversely proportional to the input voltage and proportional to the output voltage; therefore, when the duty ratio is VOUT/VIN, the frequency is constant.

Auto-Skip Eco-Mode™ Control

The TPS54329E is designed with Auto-Skip Eco-mode™ to increase light load efficiency. As the output current decreases from heavy load condition, the inductor current is also reduced and eventually comes to point that its rippled valley touches zero level, which is the boundary between continuous conduction and discontinuous conduction modes. The rectifying MOSFET is turned off when its zero inductor current is detected. As the load current further decreases the converter run into discontinuous conduction mode. The on-time is kept almost the same as is was in the continuous conduction mode so that it takes longer time to discharge the output capacitor with smaller load current to the level of the reference voltage. The transition point to the light load operation IOUT(LL) current can be calculated in [Equation 1](#)

$$I_{OUT(LL)} = \frac{1}{2 \cdot L \cdot f_{sw}} \cdot \frac{(V_{IN} - V_{OUT}) \cdot V_{OUT}}{V_{IN}} \quad (1)$$

Soft Start and Pre-Biased Soft Start

The soft start function is adjustable. When the EN pin becomes high, 6 μA current begins charging the capacitor which is connected from the SS pin to GND. Smooth control of the output voltage is maintained during start up. The equation for the slow start time is shown in [Equation 2](#). VFB voltage is 0.765 V and SS pin source current is 6 μA.

$$t_{SS(ms)} = \frac{C_{SS}(nF) \times V_{REF} \times 1.1}{I_{SS}(\mu A)} = \frac{C_{SS}(nF) \times 0.765 \times 1.1}{6} \quad (2)$$

The TPS54329E contains a unique circuit to prevent current from being pulled from the output during startup if the output is pre-biased. When the soft-start commands a voltage higher than the pre-bias level (internal soft start becomes greater than feedback voltage VFB), the controller slowly activates synchronous rectification by starting the first low side FET gate driver pulses with a narrow on-time. It then increments that on-time on a cycle-by-cycle basis until it coincides with the time dictated by (1-D), where D is the duty cycle of the converter. This scheme prevents the initial sinking of the pre-bias output, and ensure that the out voltage (VO) starts and ramps up smoothly into regulation and the control loop is given time to transition from pre-biased start-up to normal mode operation.

Current Protection

The output overcurrent protection (OCP) is implemented using a cycle-by-cycle valley detect control circuit. The switch current is monitored by measuring the low-side FET switch voltage between the SW pin and GND. This voltage is proportional to the switch current. To improve accuracy, the voltage sensing is temperature compensated.

During the on time of the high-side FET switch, the switch current increases at a linear rate determined by V_{IN} , V_{OUT} , the on-time and the output inductor value. During the on time of the low-side FET switch, this current decreases linearly. The average value of the switch current is the load current I_{out} . The TPS54329E constantly monitors the low-side FET switch voltage, which is proportional to the switch current, during the low-side on-time. If the measured voltage is above the voltage proportional to the current limit, an internal counter is incremented per each SW cycle and the converter maintains the low-side switch on until the measured voltage is below the voltage corresponding to the current limit at which time the switching cycle is terminated and a new switching cycle begins. In subsequent switching cycles, the on-time is set to a fixed value and the current is monitored in the same manner. If the over current condition exists for 7 consecutive switching cycles, the internal OCL threshold is set to a lower level, reducing the available output current. When a switching cycle occurs where the switch current is not above the lower OCL threshold, the counter is reset and the OCL limit is returned to the higher value.

There are some important considerations for this type of over-current protection. The load current one half of the peak-to-peak inductor current higher than the over-current threshold. Also when the current is being limited, the output voltage tends to fall as the demanded load current may be higher than the current available from the converter. This may cause the output voltage to fall. When the over current condition is removed, the output voltage returns to the regulated value. This protection is non-latching.

UVLO Protection

Undervoltage lock out protection (UVLO) monitors the voltage of the V_{REG5} pin. When the V_{REG5} voltage is lower than UVLO threshold voltage, the TPS54329E is shut off. This protection is non-latching.

Thermal Shutdown

TPS54329E monitors the temperature of itself. If the temperature exceeds the threshold value (typically 165°C), the device is shut off. This is non-latch protection.

TYPICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

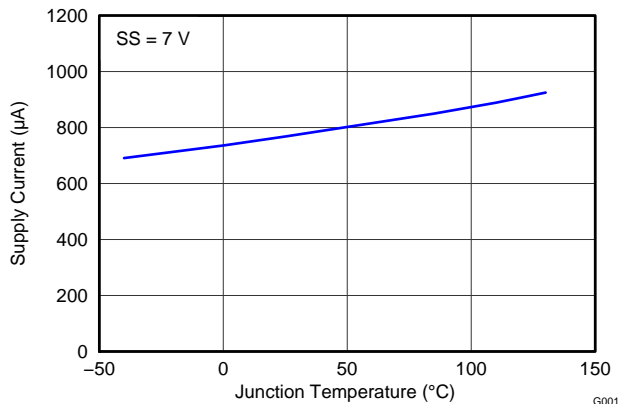


Figure 1. VIN CURRENT vs JUNCTION TEMPERATURE

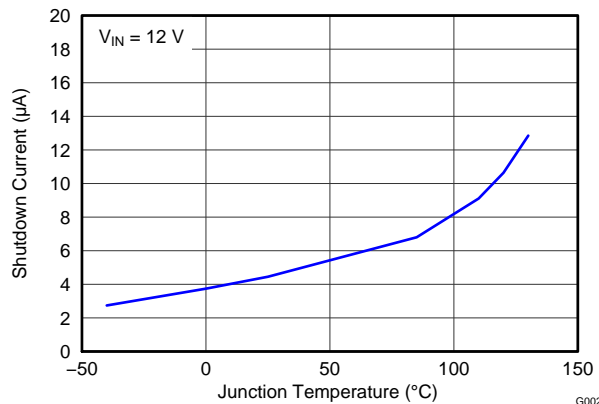


Figure 2. VIN SHUTDOWN CURRENT vs JUNCTION TEMPERATURE

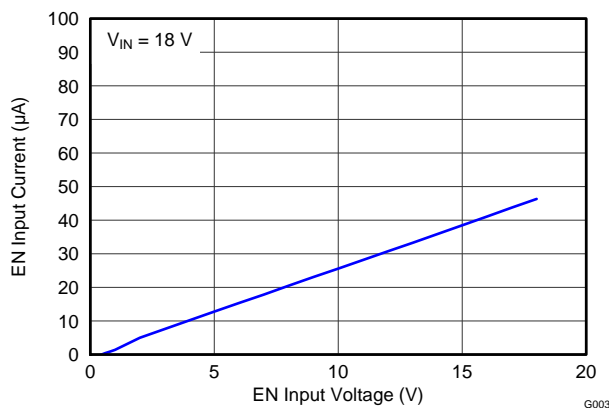


Figure 3. EN CURRENT vs EN VOLTAGE

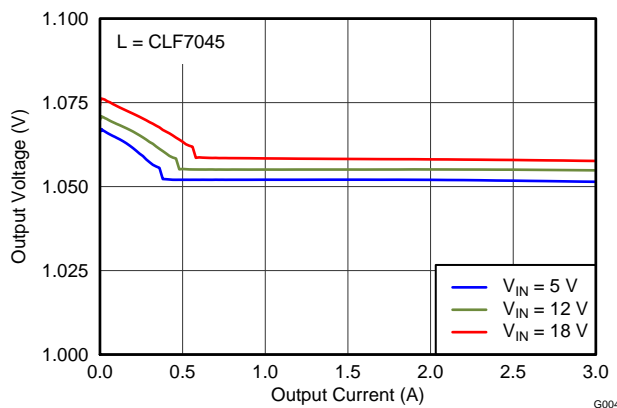


Figure 4. 1.05-V OUTPUT VOLTAGE vs OUTPUT CURRENT

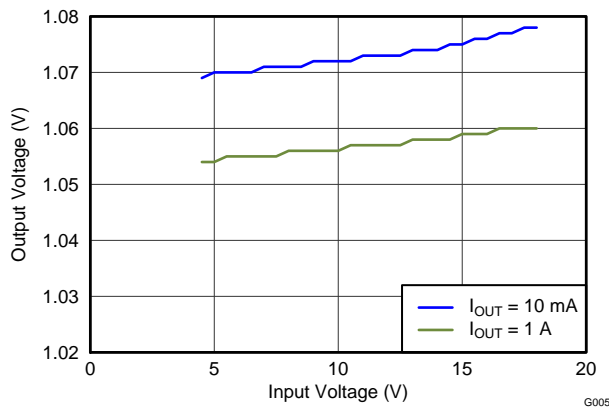


Figure 5. 1.05-V OUTPUT VOLTAGE vs INPUT VOLTAGE

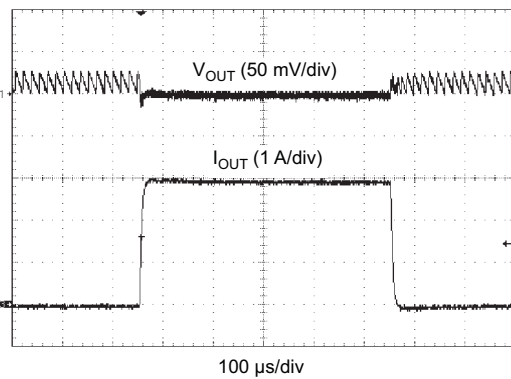


Figure 6. 1.05-V, LOAD TRANSIENT RESPONSE

TYPICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

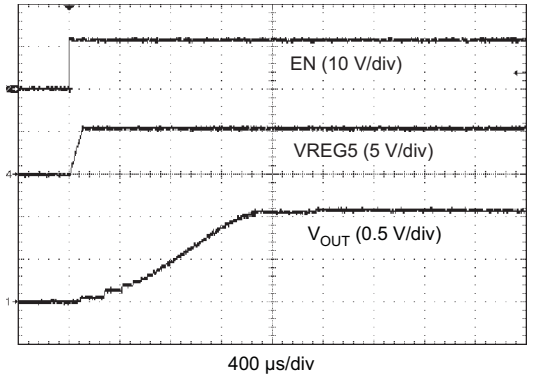


Figure 7. START-UP WAVE FORM

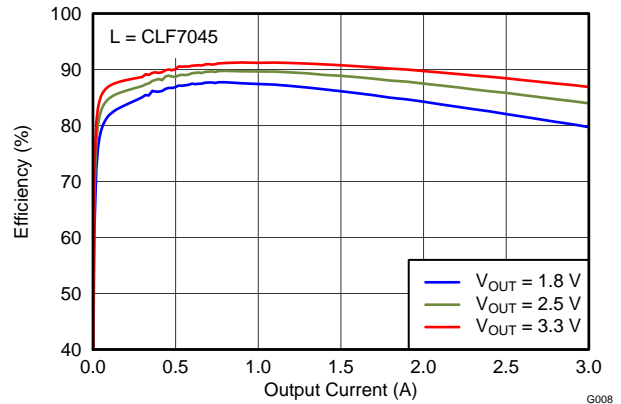


Figure 8. EFFICIENCY vs OUTPUT CURRENT

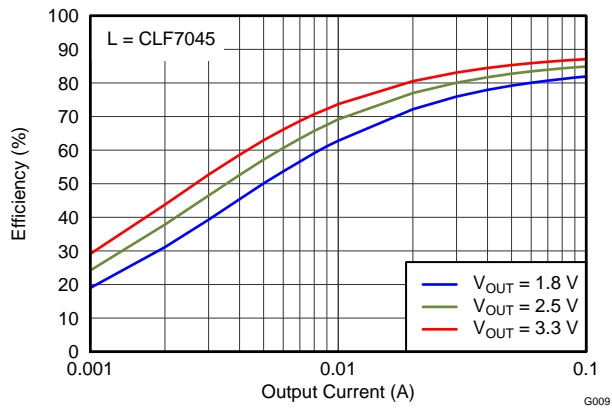


Figure 9. LIGHT LOAD EFFICIENCY vs OUTPUT CURRENT

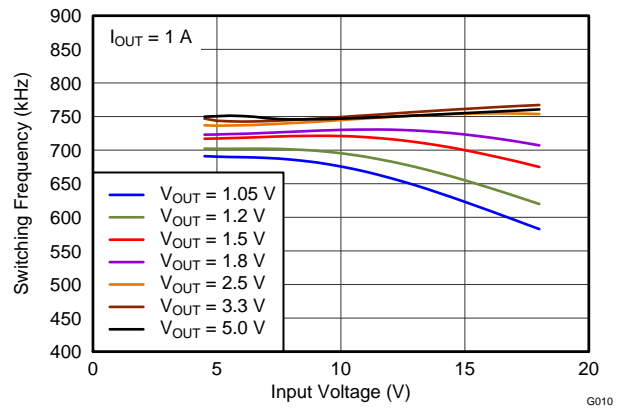


Figure 10. SWITCHING FREQUENCY vs INPUT VOLTAGE

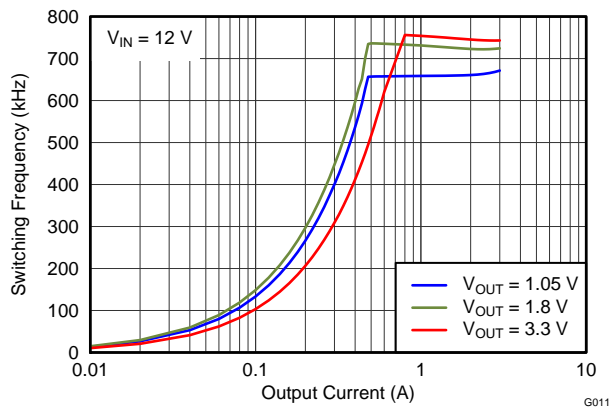


Figure 11. SWITCHING FREQUENCY vs OUTPUT CURRENT

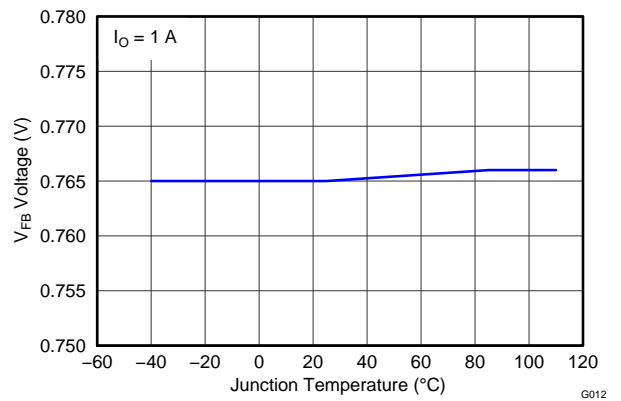


Figure 12. V_{FB} VOLTAGE vs JUNCTION TEMPERATURE

TYPICAL CHARACTERISTICS

$V_{IN} = 12\text{ V}$, $T_A = 25^\circ\text{C}$ (unless otherwise noted).

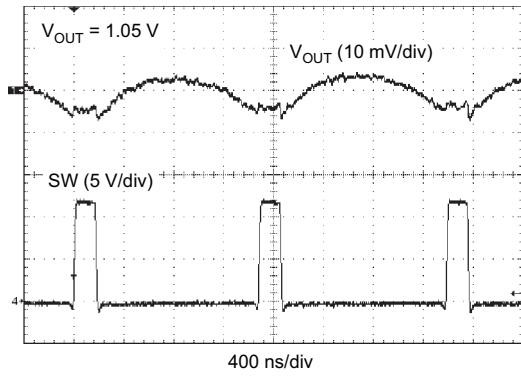


Figure 13. OUTPUT VOLTAGE RIPPLE ($I_O = 3\text{ A}$)

G013

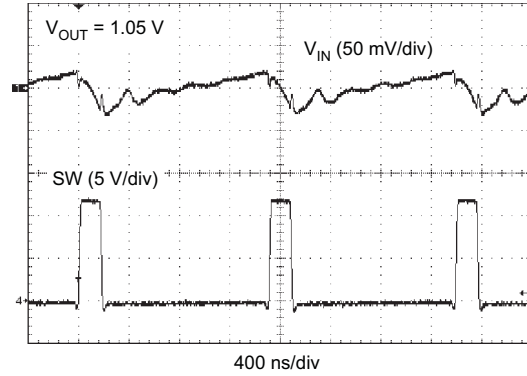


Figure 14. INPUT VOLTAGE RIPPLE ($I_O = 3\text{ A}$)

G014

DESIGN GUIDE

Step-By-Step Design Procedure

To begin the design process, the user must know a few application parameters:

- Input voltage range
- Output voltage
- Output current
- Output voltage ripple
- Input voltage ripple

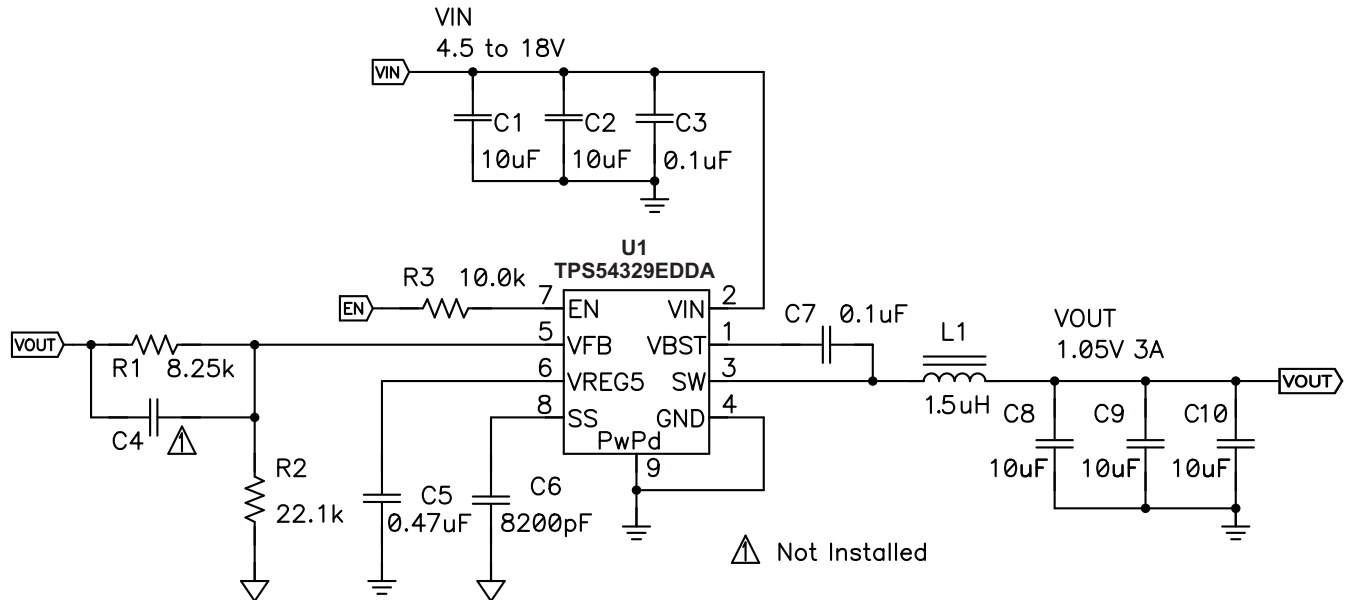


Figure 15. Shows the schematic diagram for this design example.

Output Voltage Resistors Selection

The output voltage is set with a resistor divider from the output node to the VFB pin. It is recommended to use 1% tolerance or better divider resistors. Start by using Equation 3 to calculate V_{OUT} .

To improve efficiency at light loads consider using larger value resistors, high resistance is more susceptible to noise, and the voltage errors from the VFB input current are more noticeable.

$$V_{OUT} = 0.765 \times \left(1 + \frac{R1}{R2} \right) \quad (3)$$

Output Filter Selection

The output filter used with the TPS54329E is an LC circuit. This LC filter has double pole at:

$$F_P = \frac{1}{2\pi\sqrt{L_{OUT} \times C_{OUT}}} \quad (4)$$

At low frequencies, the overall loop gain is set by the output set-point resistor divider network and the internal gain of the TPS54329E. The low frequency phase is 180 degrees. At the output filter pole frequency, the gain rolls off at a -40 dB per decade rate and the phase drops rapidly. D-CAP2™ introduces a high frequency zero that reduces the gain roll off to -20 dB per decade and increases the phase to 90 degrees one decade above the zero frequency. The inductor and capacitor selected for the output filter must be selected so that the double pole of Equation 4 is located below the high frequency zero but close enough that the phase boost provided by the high frequency zero provides adequate phase margin for a stable circuit. To meet this requirement use the values recommended in Table 1

Table 1. Recommended Component Values

| Output Voltage (V) | R1 (kΩ) | R2 (kΩ) | C4 (pF) ⁽¹⁾ | L1 (μH) | C8 + C9 + C10 (μF) |
|--------------------|---------|---------|------------------------|---------|--------------------|
| 1 | 6.81 | 22.1 | | 1.5 | 20 - 68 |
| 1.05 | 8.25 | 22.1 | | 1.5 | 20 - 68 |
| 1.2 | 12.7 | 22.1 | | 1.5 | 20 - 68 |
| 1.5 | 21.5 | 22.1 | | 1.5 | 20 - 68 |
| 1.8 | 30.1 | 22.1 | 5 - 22 | 2.2 | 20 - 68 |
| 2.5 | 49.9 | 22.1 | 5 - 22 | 2.2 | 20 - 68 |
| 3.3 | 73.2 | 22.1 | 5 - 22 | 2.2 | 20 - 68 |
| 5 | 124 | 22.1 | 5 - 22 | 3.3 | 20 - 68 |
| 6.5 | 165 | 22.1 | 5 - 22 | 3.3 | 20 - 68 |

(1) Optional

Since the DC gain is dependent on the output voltage, the required inductor value increases as the output voltage increases. For higher output voltages at or above 1.8 V, additional phase boost can be achieved by adding a feed forward capacitor (C4) in parallel with R1

The inductor peak-to-peak ripple current, peak current and RMS current are calculated using [Equation 5](#), [Equation 6](#) and [Equation 7](#). The inductor saturation current rating must be greater than the calculated peak current and the RMS or heating current rating must be greater than the calculated RMS current. Use 650 kHz for f_{sw} .

Make sure the chosen inductor is rated for the peak current of [Equation 6](#) and the RMS current of [Equation 7](#).

$$I_{IPP} = \frac{V_{OUT}}{V_{IN(max)}} \times \frac{V_{IN(max)} - V_{OUT}}{L_O \times f_{SW}} \quad (5)$$

$$I_{Ipeak} = I_O + \frac{I_{Ipp}}{2} \quad (6)$$

$$I_{Lo(RMS)} = \sqrt{I_O^2 + \frac{1}{12} I_{IPP}^2} \quad (7)$$

For this design example, the calculated peak current is 3.49 A and the calculated RMS current is 3.01 A. The inductor used is a TDK CLF7045T-1R5N with a peak current rating of 7.3 A and an RMS current rating of 4.9 A.

The capacitor value and ESR determines the amount of output voltage ripple. The TPS54329E is intended for use with ceramic or other low ESR capacitors. Recommended values range from 20μF to 68μF. Use [Equation 8](#) to determine the required RMS current rating for the output capacitor.

$$I_{Co(RMS)} = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{\sqrt{12} \times V_{IN} \times L_O \times f_{SW}} \quad (8)$$

For this design three TDK C3216X5R0J106M 10μF output capacitors are used. The typical ESR is 2 mΩ each. The calculated RMS current is 0.284 A and each output capacitor is rated for 4 A.

Input Capacitor Selection

The TPS54329E requires an input decoupling capacitor and a bulk capacitor is needed depending on the application. A ceramic capacitor over 10 μF is recommended for the decoupling capacitor. An additional 0.1 μF capacitor (C3) is required to provide additional high frequency filtering and insure accurate current limit operation. This capacitor must be placed as close to the IC pins 2 (VIN) and 4 (GND) as possible. The capacitor voltage rating needs to be greater than the maximum input voltage.

Bootstrap Capacitor Selection

A 0.1 μF. ceramic capacitor must be connected between the VBST to SW pin for proper operation. It is recommended to use a ceramic capacitor.

VREG5 Capacitor Selection

A 0.47 μF . ceramic capacitor must be connected between the VREG5 to GND pin for proper operation. It is recommended to use a ceramic capacitor.

THERMAL INFORMATION

This 8-pin DDA package incorporates an exposed thermal pad that is designed to be directly to an external heatsink. The thermal pad must be soldered directly to the printed board (PCB). After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the exposed thermal pad and how to use the advantage of its heat dissipating abilities, see the Technical Brief, PowerPAD™ Thermally Enhanced Package, Texas Instruments Literature No. [SLMA002](#) and Application Brief, PowerPAD™ Made Easy, Texas Instruments Literature No. [SLMA004](#).

The exposed thermal pad dimensions for this package are shown in the following illustration.

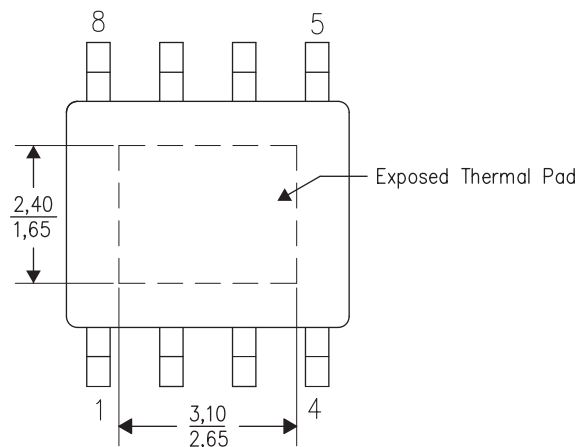


Figure 16. Thermal Pad Dimensions

LAYOUT CONSIDERATIONS

1. Keep the input switching current loop as small as possible.
2. Keep the SW node as physically small and short as possible to minimize parasitic capacitance and inductance and to minimize radiated emissions. Kelvin connections should be brought from the output to the feedback pin of the device.
3. Keep analog and non-switching components away from switching components.
4. Make a single point connection from the analog ground to power ground.
5. Do not allow switching current to flow under the device.
6. Keep the pattern lines for VIN and PGND broad.
7. Exposed pad of device must be connected to PGND with solder.
8. VREG5 capacitor should be placed near the device, and connected to PGND.
9. Output capacitor should be connected to a broad pattern of the PGND.
10. Voltage feedback loop should be as short as possible, and preferably with ground shield.
11. Lower resistor of the voltage divider which is connected to the VFB pin should be tied to analog ground trace.
12. Providing sufficient via is preferable for VIN, SW and PGND connection.
13. VIN input bypass capacitor and VIN high frequency bypass capacitor must be placed as near as possible to the device.
14. Performance based on four layer printed circuit board.

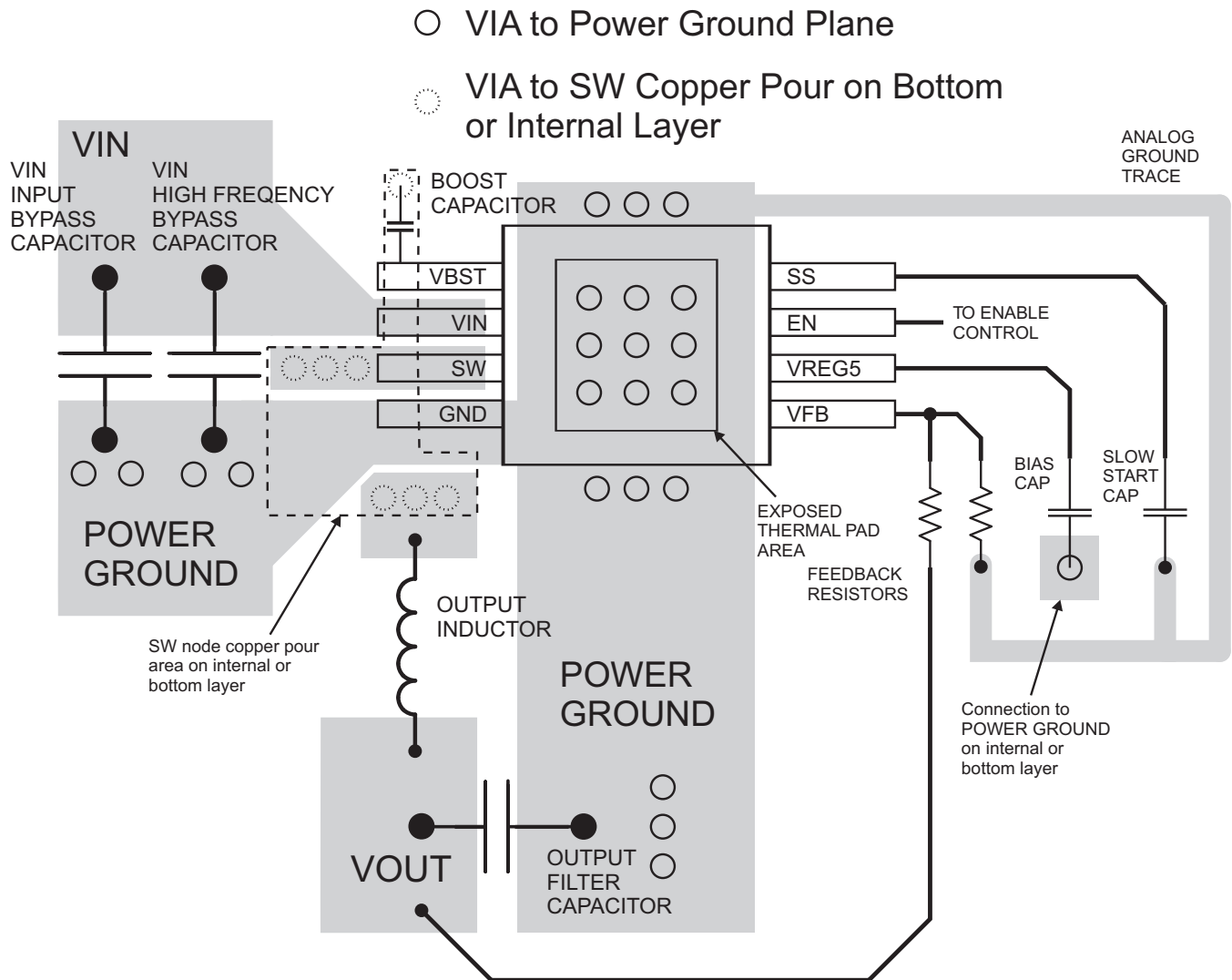


Figure 17. PCB Layout

REVISION HISTORY

| Changes from Original (September 2011) to Revision A | Page |
|---|------|
| • Removed SWIFT™ from the data sheet title | 1 |
| • Deleted from ELECTRICAL CHARACTERISTICS table, V_{LN5} and V_{LD5} , deleted V_{VREG5} MIN and MAX values | 3 |
| • Added in ELECTRICAL CHARACTERISTICS table, I_{VREG5} and $R_{DS(on)}$ footnote references | 3 |
| • Added in ELECTRICAL CHARACTERISTICS table, $t_{OFF(MIN)}$ footnote reference and deleted MAX value | 4 |
| • Deleted from ELECTRICAL CHARACTERISTICS, UVLO MIN and MAX values | 4 |
| • Added TYPICAL CHARACTERISTICS Condition | 9 |

PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|-------------------------|-------------------------|
| TPS54329EDDA | ACTIVE | SO PowerPAD | DDA | 8 | 75 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-2-260C-1 YEAR | -40 to 85 | 54329E | Samples |
| TPS54329EDDAR | ACTIVE | SO PowerPAD | DDA | 8 | 2500 | Green (RoHS & no Sb/Br) | CU NIPDAU CU SN | Level-2-260C-1 YEAR | -40 to 85 | 54329E | Samples |

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBsolete: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION



QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| TPS54329EDDAR | SO Power PAD | DDA | 8 | 2500 | 330.0 | 12.8 | 6.4 | 5.2 | 2.1 | 8.0 | 12.0 | Q1 |

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

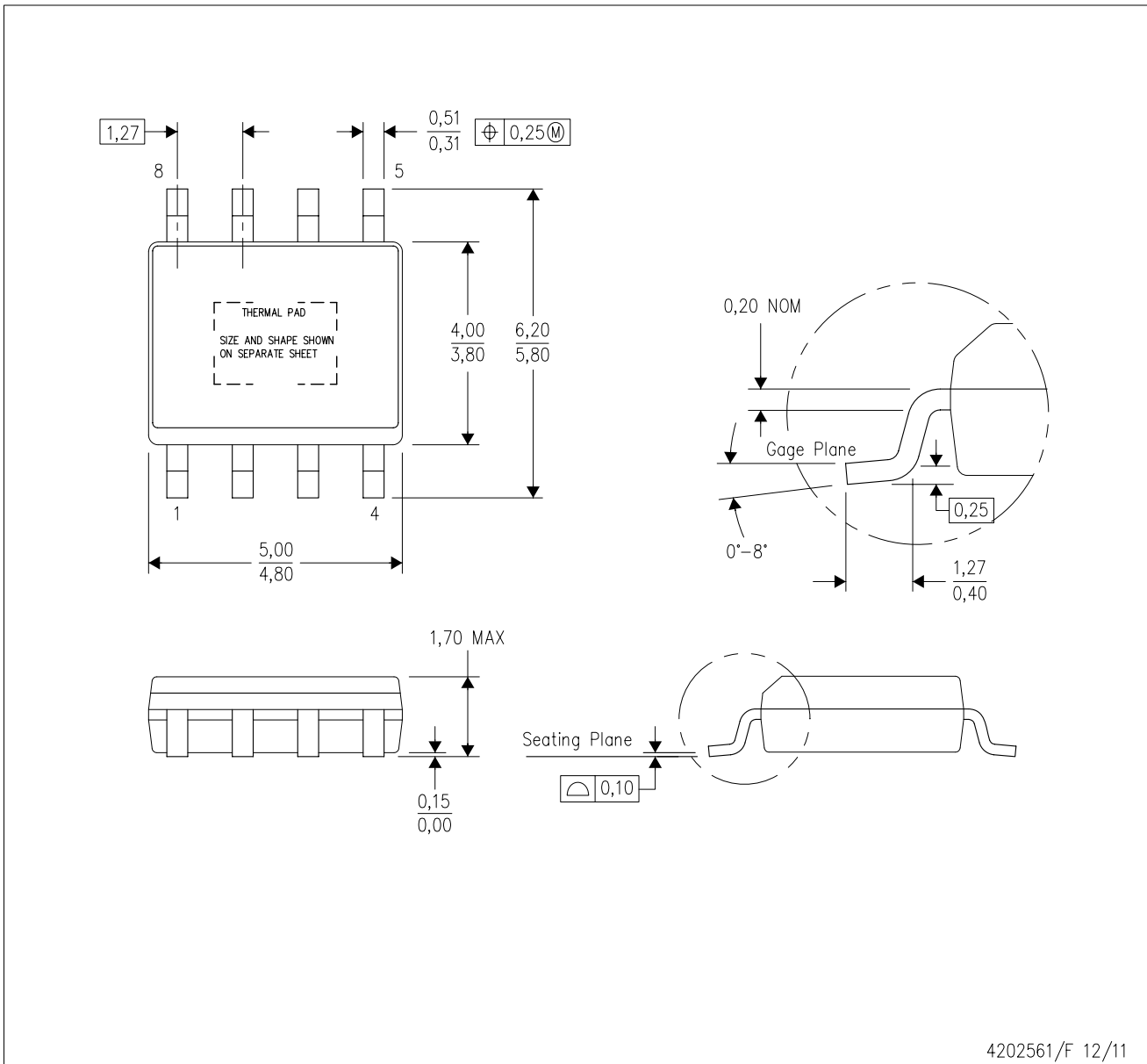
| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---------------|--------------|-----------------|------|------|-------------|------------|-------------|
| TPS54329EDDAR | SO PowerPAD | DDA | 8 | 2500 | 366.0 | 364.0 | 50.0 |



Images above are just a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.

DDA (R-PDSO-G8)

PowerPAD™ PLASTIC SMALL-OUTLINE



4202561/F 12/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5-1994.
 - B. This drawing is subject to change without notice.
 - C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 for information regarding recommended board layout. This document is available at www.ti.com <<http://www.ti.com>>.
 - E. See the additional figure in the Product Data Sheet for details regarding the exposed thermal pad features and dimensions.
 - F. This package complies to JEDEC MS-012 variation BA

PowerPAD is a trademark of Texas Instruments.

DDA (R-PDSO-G8)

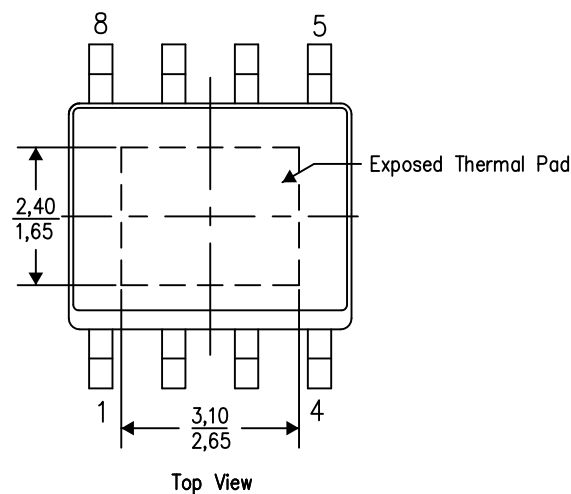
PowerPAD™ PLASTIC SMALL OUTLINE

THERMAL INFORMATION

This PowerPAD™ package incorporates an exposed thermal pad that is designed to be attached to a printed circuit board (PCB). The thermal pad must be soldered directly to the PCB. After soldering, the PCB can be used as a heatsink. In addition, through the use of thermal vias, the thermal pad can be attached directly to the appropriate copper plane shown in the electrical schematic for the device, or alternatively, can be attached to a special heatsink structure designed into the PCB. This design optimizes the heat transfer from the integrated circuit (IC).

For additional information on the PowerPAD package and how to take advantage of its heat dissipating abilities, refer to Technical Brief, PowerPAD Thermally Enhanced Package, Texas Instruments Literature No. SLMA002 and Application Brief, PowerPAD Made Easy, Texas Instruments Literature No. SLMA004. Both documents are available at www.ti.com.

The exposed thermal pad dimensions for this package are shown in the following illustration.



Exposed Thermal Pad Dimensions

4206322-6/L 05/12

NOTE: A. All linear dimensions are in millimeters

PowerPAD is a trademark of Texas Instruments



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Publication IPC-7351 is recommended for alternate designs.
 - D. This package is designed to be soldered to a thermal pad on the board. Refer to Technical Brief, PowerPad Thermally Enhanced Package, Texas Instruments Literature No. SLMA002, SLMA004, and also the Product Data Sheets for specific thermal information, via requirements, and recommended board layout. These documents are available at www.ti.com <<http://www.ti.com>>. Publication IPC-7351 is recommended for alternate designs.
 - E. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.
 - F. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PowerPAD is a trademark of Texas Instruments.

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to TI's Terms of Sale (www.ti.com/legal/termsofsale.html) or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265
Copyright © 2019, Texas Instruments Incorporated