

1.8 V / 2.5 V Differential D Flip-Flop w/ Reset and CML Outputs

Multi-Level Inputs w/ Internal Termination

NB7V52M

Description

The NB7V52M is a 10 GHz differential D flip-flop with a differential asynchronous Reset. The differential D/ $\bar{D}$, CLK/ $\bar{CLK}$ and R/ $\bar{R}$ inputs incorporate dual internal 50 Ω termination resistors and will accept LVPECL, CML, LVDS logic levels.

When Clock transitions from logic Low to High, Data will be transferred to the differential CML outputs. The differential Clock inputs allow the NB7V52M to also be used as a negative edge triggered device.

The 16 mA differential CML outputs provide matching internal 50 Ω termination and produce 400 mV output swings when externally receiver terminated with a 50 Ω resistor to V_{CC} .

The NB7V52M is offered in a low profile 3 mm x 3 mm 16-pin QFN package. The NB7V52M is a member of the GigaComm™ family of high performance clock products. Application notes, models, and support documentation are available at www.onsemi.com.

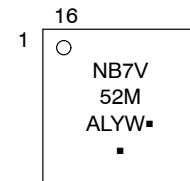
Features

- Maximum Input Clock Frequency > 10 GHz
- Maximum Input Data Rate > 10 Gb/s
- Random Clock Jitter < 0.8 ps RMS, Max
- 200 ps Typical Propagation Delay
- 35 ps Typical Rise and Fall Times
- Differential CML Outputs, 400 mV Peak-to-Peak, Typical
- Operating Range: $V_{CC} = 1.71$ V to 2.625 V with $V_{EE} = 0$ V
- Internal 50 Ω Input Termination Resistors
- QFN-16 Package, 3mm x 3mm
- -40°C to +85°C Ambient Operating Temperature
- These are Pb-Free Devices



QFN-16
MN SUFFIX
CASE 485G

MARKING DIAGRAM*



A	= Assembly Location
L	= Wafer Lot
Y	= Year
W	= Work Week
▪	= Pb-Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note [AND8002/D](#).

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

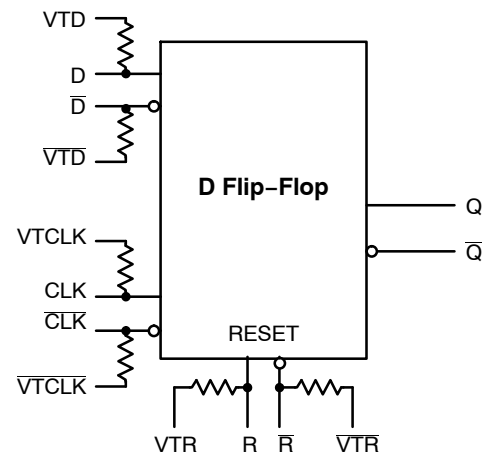


Figure 1. Logic Diagram

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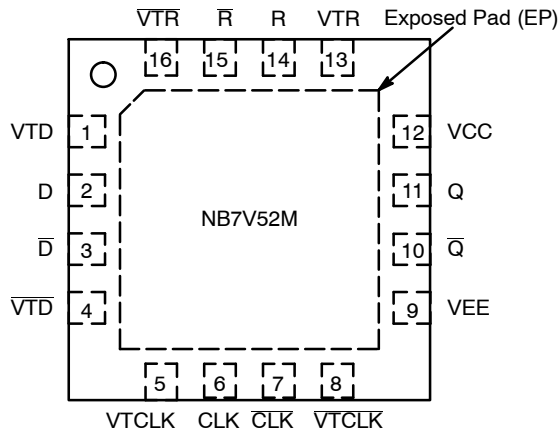


Table 1. INPUT/OUTPUT SELECT TRUTH TABLE

R	D	CLK	Q
H	x	x	L
L	L	Z	L
L	H	Z	H

Z = LOW to HIGH Transition
x = Don't care

Figure 2. Pin Configuration (Top View)

Table 1. Pin Description

Pin	Name	I/O	Description
1	VTD	–	Internal 50 Ω Termination Pin for D
2	D	LVPECL, CML, LVDS Input	Noninverted Differential Data Input. (Note 1)
3	$\bar{D}$	LVPECL, CML, LVDS Input	Inverted Differential Data Input. (Note 1)
4	$\bar{VTD}$	–	Internal 50 Ω Termination Pin for $\bar{D}$
5	VTCLK	–	Internal 50 Ω Termination Pin for CLK
6	CLK	LVPECL, CML, LVDS Input	Noninverted Differential Clock Input. (Note 1)
7	$\bar{CLK}$	LVPECL, CML, LVDS Input	Inverted Differential Clock Input. (Note 1)
8	$\bar{VTCLK}$	–	Internal 50 Ω Termination Pin for $\bar{CLK}$
9	VEE	–	Negative Supply Voltage. (Note 2)
10	$\bar{Q}$	CML Output	Inverted Differential Output
11	Q	CML Output	Noninverted Differential Output
12	VCC	–	Positive Supply Voltage. (Note 2)
13	VTR	–	Internal 50 Ω Termination Pin for R
14	R	LVPECL, CML, LVDS Input	Noninverted Asynchronous Differential Reset Input. (Note 1)
15	$\bar{R}$	LVPECL, CML, LVDS Input	Inverted Asynchronous Differential Reset Input. (Note 1)
16	$\bar{VTR}$	–	Internal 50 Ω Termination Pin for $\bar{R}$
–	EP	–	The Exposed Pad (EP) on the QFN–16 package bottom is thermally connected to the die for improved heat transfer out of package. The exposed pad must be attached to a heat-sinking conduit. The pad is electrically connected to the die, and must be electrically and thermally connected to VEE on the PC board.

1. In the differential configuration when the input termination pins (VT_x , $\bar{VT}_x$) are connected to a common termination voltage or left open, and if no signal is applied on CLK/ $\bar{CLK}$ input, then the device will be susceptible to self-oscillation.
2. All VCC and VEE pins must be externally connected to a power supply for proper operation.

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Table 2. ATTRIBUTES

Characteristics		Value
ESD Protection	Human Body Model Machine Model	> 2 kV > 200 V
Moisture Sensitivity	16-QFN	Level 1
Flammability Rating	Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count		173
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test		

For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	V _{EE} = 0 V		3.0	V
V _{IO}	Positive Input/Output Voltage	V _{EE} = 0 V	-0.5 ≤ V _{IO} ≤ V _{CC} + 0.5	-0.5 to V _{CC} + 0.5	V
V _{INPP}	Differential Input Voltage CLK - $\overline{\text{CLK}}$, D - $\overline{\text{D}}$, R - $\overline{\text{R}}$			1.89	V
I _{OUT}	Output Current Through R _{TOUT} (50 Ω Resistor)	Continuous Surge		34 40	mA
I _{IN}	Input Current Through R _{TIN} (50 Ω Resistor)			± 40	mA
T _A	Operating Temperature Range			-40 to +85	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-16 QFN-16	42 35	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case) (Note 3)		QFN-16	4	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

3. JEDEC standard multilayer board – 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 4. DC CHARACTERISTICS, Multi-Level Inputs $V_{CC} = 1.71\text{ V}$ to 2.625 V , $V_{EE} = 0\text{ V}$, $T_A = -40^\circ\text{C}$ to $+85^\circ\text{C}$ (Note 4)

Symbol	Characteristic	Min	Typ	Max	Unit
POWER SUPPLY CURRENT					
I _{CC}	Power Supply Current (Inputs and Outputs Open) V _{CC} = 2.5 V V _{CC} = 1.8 V		90 70	110 90	mA
CML OUTPUTS					
V _{OH}	Output HIGH Voltage (Note 5) V _{CC} = 2.5 V V _{CC} = 1.8 V	V _{CC} – 30 2470 1770	V _{CC} – 10 2490 1790	V _{CC} 2500 1800	mV
V _{OL}	Output LOW Voltage (Note 5) V _{CC} = 2.5 V V _{CC} = 1.8 V	V _{CC} – 650 1850	V _{CC} – 500 2000	V _{CC} – 400 2100	mV
		V _{CC} – 600 1200	V _{CC} – 450 1350	V _{CC} – 350 1450	
DIFFERENTIAL CLOCK INPUTS DRIVEN SINGLE-ENDED (Note 6) (Figures 5 and 7)					
V _{th}	Input Threshold Reference Voltage Range (Note 7)	1000		V _{CC} – 100	mV
V _{IH}	Single-Ended Input HIGH Voltage	V _{th} + 100		V _{CC}	mV
V _{IL}	Single-Ended Input LOW Voltage	V _{EE}		V _{th} – 100	mV
V _{ISE}	Single-Ended Input Voltage (V _{IH} – V _{IL})	200		1200	mV
DIFFERENTIAL D/D, CLK/CLK, R/R INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8) (Note 8)					
V _{IHD}	Differential Input HIGH Voltage	1100		V _{CC}	mV
V _{ILD}	Differential Input LOW Voltage	V _{EE}		V _{CC} – 100	mV
V _{ID}	Differential Input Voltage (V _{IHD} – V _{ILD})	100		1200	mV
V _{CMR}	Input Common Mode Range (Differential Configuration, Note 9) (Figure 10)	1050		V _{CC} – 50	mV
I _{IH}	Input HIGH Current (V _{Tx} /V _{Tx} Open)	–250		250	μA
I _{IL}	Input LOW Current (V _{Tx} /V _{Tx} Open)	–250		250	μA
TERMINATION RESISTORS					
R _{TIN}	Internal Input Termination Resistor	45	50	55	Ω
R _{TOUT}	Internal Output Termination Resistor	45	50	55	Ω

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfm.

- Input and output parameters vary 1:1 with V_{CC} .
- CML outputs loaded with $50\ \Omega$ to V_{CC} for proper operation.
- V_{th} , V_{IH} , V_{IL} , and V_{ISE} parameters must be complied with simultaneously.
- V_{th} is applied to the complementary input when operating in single-ended mode.
- V_{IHD} , V_{ILD} , V_{ID} and V_{CMR} parameters must be complied with simultaneously.
- V_{CMR} min varies 1:1 with V_{EE} , V_{CMR} max varies 1:1 with V_{CC} . The V_{CMR} range is referenced to the most positive side of the differential input signal.

Table 5. AC CHARACTERISTICS $V_{CC} = 1.71\text{ V to }2.625\text{ V}$; $V_{EE} = 0\text{ V}$; $T_A = -40^\circ\text{C to }85^\circ\text{C}$ (Note 10)

Symbol	Characteristic	Min	Typ	Max	Unit
f_{MAX}	Maximum Input Clock Frequency	10	12		GHz
$f_{DATA\ MAX}$	Maximum Input Data Rate (PRBS23)	10	12		Gbps
V_{OUTPP}	Output Voltage Amplitude (@ $V_{INPPmin}$) (See Figures 3 and 10, Note 11)	$f_{in} \leq 7\text{ GHz}$ 300 $f_{in} \leq 10\text{ GHz}$ 250	400 400		mV
t_{PLH} , t_{PHL}	Propagation Delay to Differential Outputs, @ 1 GHz, Measured at Differential Cross-point		CLK/CLK to Q/Q 200 R/R to Q/Q 300	350 600	ps
t_S	Setup Time (D to CLK)	40	15		ps
t_H	Hold Time (D to CLK)	50	20		ps
t_{RR}	Reset Recovery	275	200		ps
t_{PW}	Minimum Pulse Width	1			ns
t_{JITTER}	RJ – Output Random Jitter (Note 12)		$f_{in} \leq 10\text{ GHz}$ 0.2	0.8	ps RMS
V_{INPP}	Input Voltage Swing (Differential Configuration) (Note 13)	100		1200	mV
t_r , t_f	Output Rise/Fall Times @ 1 GHz (20% – 80%),		Q, $\bar{Q}$ 20	35 50	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm.

10. Measured using a 400 mV V_{INPP} source, 50% duty cycle clock source. All output loading with external $50\ \Omega$ to V_{CC} . Input edge rates $\geq 40\text{ ps}$ (20% – 80%).

11. Output voltage swing is a single-ended measurement operating in differential mode.

12. Additive RMS jitter with 50% duty cycle clock signal.

13. Input voltage swing is a single-ended measurement operating in differential mode.

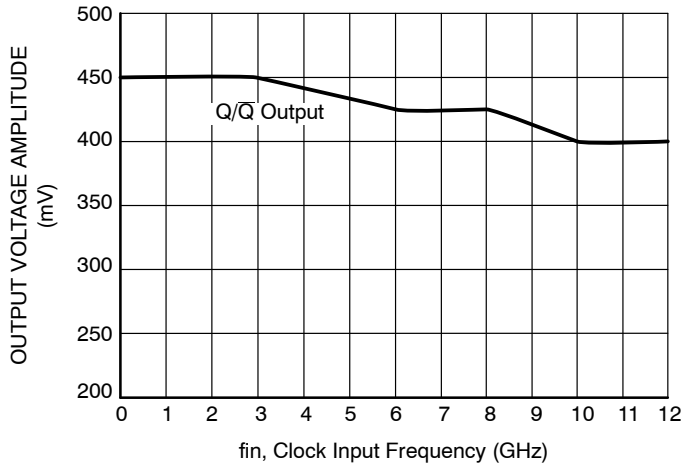


Figure 3. Clock Output Voltage Amplitude (V_{OUTPP}) vs. Input Frequency (f_{in}) at Ambient Temperature (Typ)

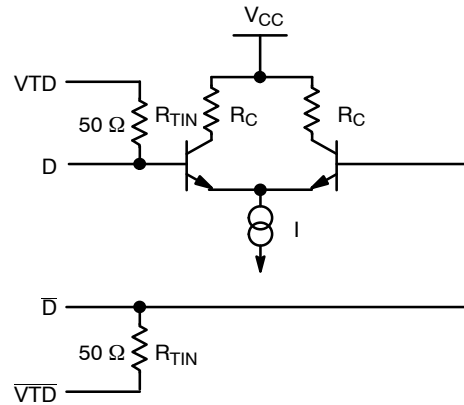


Figure 4. Simplified Input Structure

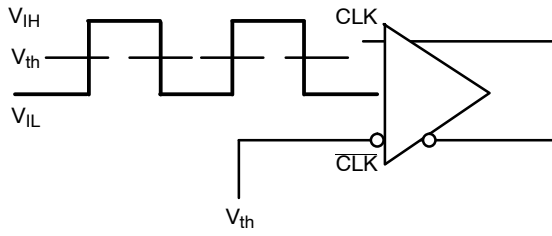


Figure 5. Differential Input Driven Single-Ended

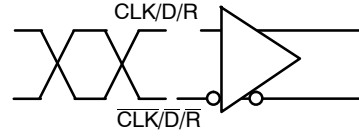


Figure 6. Differential Inputs Driven Differentially

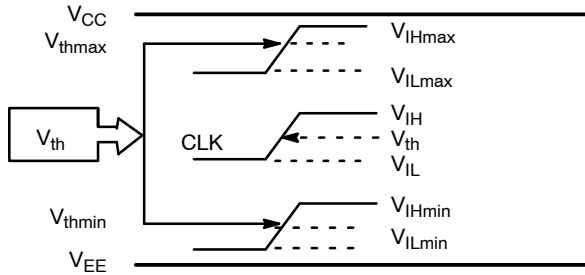


Figure 7. V_{th} Diagram

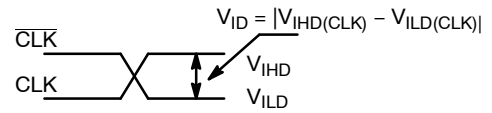


Figure 8. Differential Inputs Driven Differentially

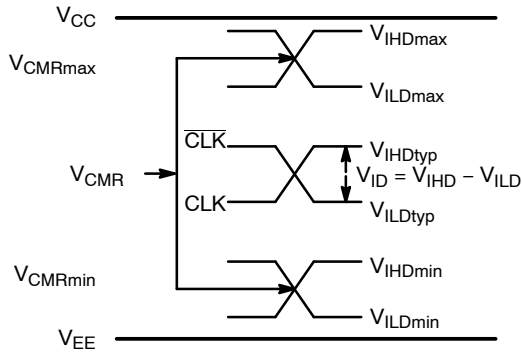


Figure 9. V_{CMR} Diagram

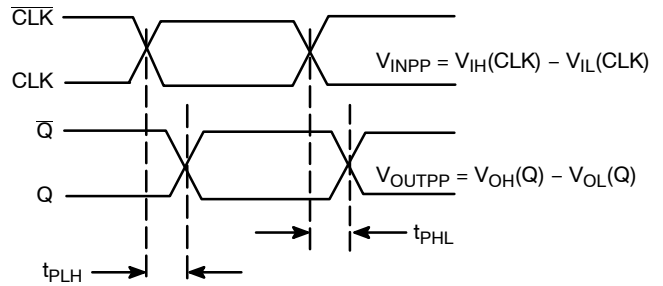


Figure 10. AC Reference Measurement

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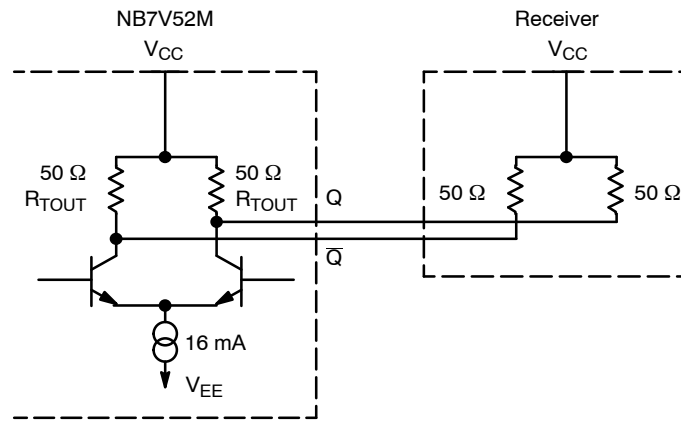


Figure 11. Typical CML Output Structure and Termination

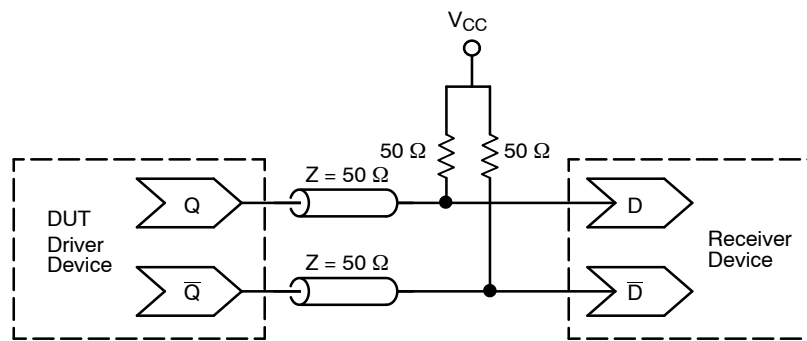


Figure 12. Typical Termination for CML Output Driver and Device Evaluation

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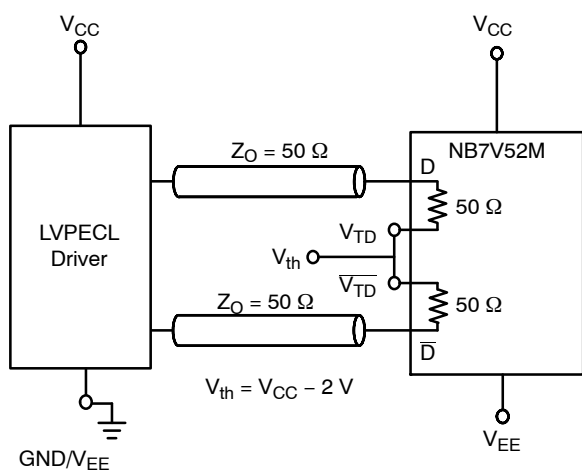


Figure 13. LVPECL Interface

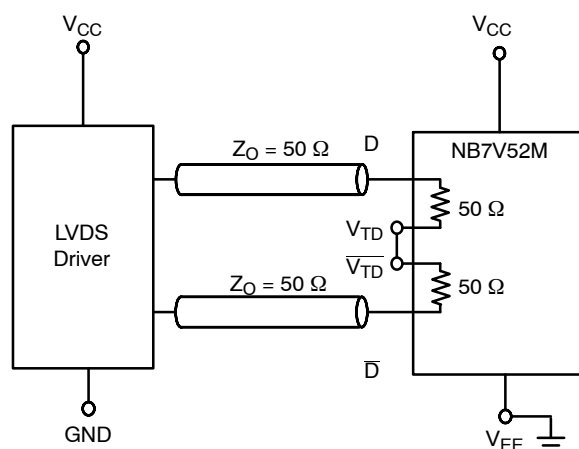


Figure 14. LVDS Interface

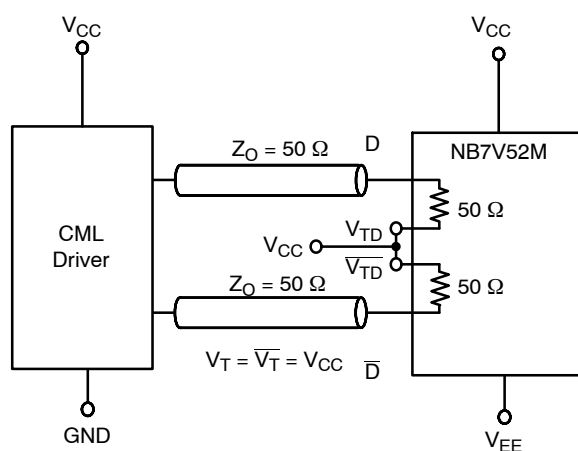


Figure 15. Standard 50 Ω Load CML Interface

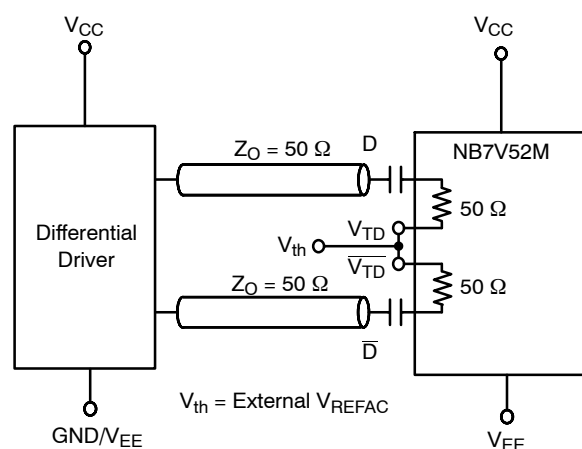


Figure 16. Capacitor-Coupled Differential Interface ($V_T/\bar{V}_T$ Connected to External V_{REFAC} ; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

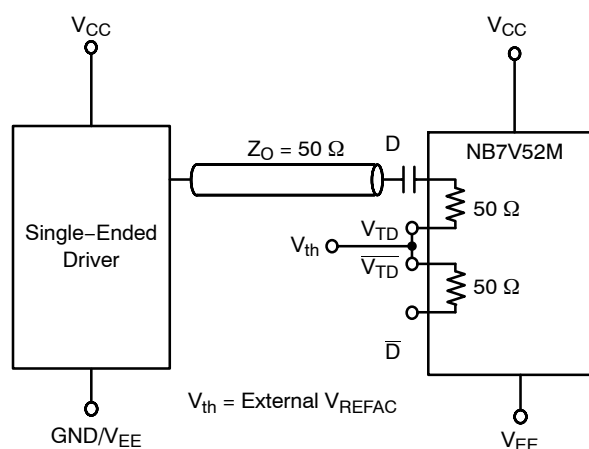


Figure 17. Capacitor-Coupled Single-Ended Interface ($V_T/\bar{V}_T$ Connected to External V_{REFAC} ; V_{REFAC} Bypassed to Ground with 0.1 μF Capacitor)

NB7V52M

ORDERING INFORMATION

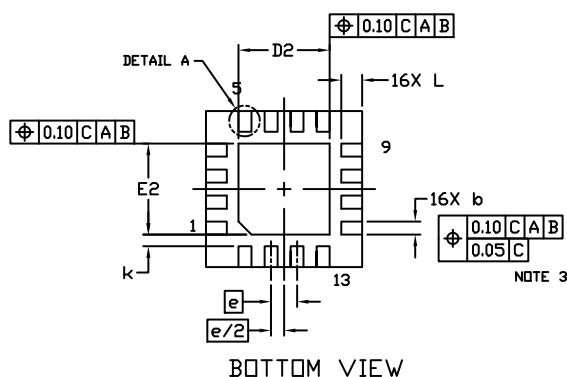
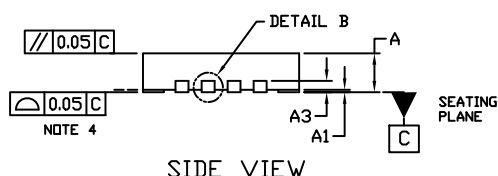
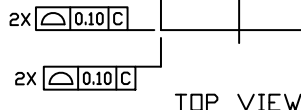
Device	Package	Shipping [†]
NB7V52MMNG	QFN-16 (Pb-free)	123 Units / Rail
NB7V52MMNHTBG	QFN-16 (Pb-free)	100 / Tape & Reel
NB7V52MMNTXG	QFN-16 (Pb-free)	3000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, [BRD8011/D](#).



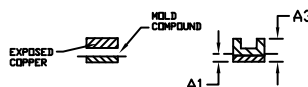
CASE 485G
ISSUE G

DATE 08 OCT 2021

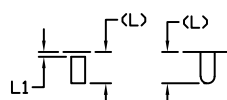


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.15 AND 0.30 MM FROM THE TERMINAL TIP.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.



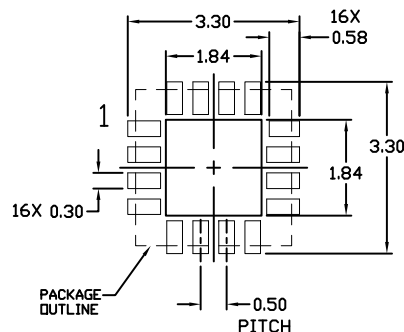
DETAIL B
ALTERNATE
CONSTRUCTIONS



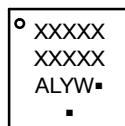
DETAIL A
ALTERNATE TERMINAL
CONSTRUCTIONS

DIM	MILLIMETERS		MAX.
	MIN.	NOM.	
A	0.80	0.90	1.00
A1	0.00	0.03	0.05
A3	0.20 REF		
b	0.18	0.24	0.30
D	3.00 BSC		
D2	1.65	1.75	1.85
E	3.00 BSC		
E2	1.65	1.75	1.85
e	0.50 BSC		
k	0.18 TYP		
L	0.30	0.40	0.50
L1	0.00	0.08	0.15

MOUNTING FOOTPRINT



GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb-Free Package

(Note: Microdot may be in either location)

*This information is generic. Please refer to device data sheet for actual part marking. Pb-Free indicator, "G" or microdot "•", may or may not be present. Some products may not follow the Generic Marking.

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DESCRIPTION:	QFN16 3X3, 0.5P	PAGE 1 OF 1

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