

## UPA2717AGR-VB Datasheet

### P-Channel 30 V (D-S) MOSFET

PRODUCT SUMMARY	
$V_{DS}$ (V)	-30
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 10$ V	0.0050
$R_{DS(on)}$ ( $\Omega$ ) at $V_{GS} = 4.5$ V	0.0080
$Q_g$ typ. (nC)	27
$I_D$ (A)	18
Configuration	Single

#### FEATURES

- Trench Gen IV p-channel power MOSFET
- Enables higher power density
- 100 %  $R_g$  and UIS tested



**RoHS**  
COMPLIANT  
HALOGEN  
**FREE**



#### APPLICATIONS

- Battery management in mobile devices
- Adapter and charger switch
- Battery switch
- Load switch

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25$ °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		$V_{DS}$	-30	V
Gate-source voltage		$V_{GS}$	$\pm 20$	
Continuous drain current ( $T_J = 150$ °C)	$T_C = 25$ °C	$I_D$	-18	A
	$T_C = 70$ °C		-13	
	$T_A = 25$ °C		-11	
	$T_A = 70$ °C		-8	
Pulsed drain current ( $t = 100$ $\mu$ s)		$I_{DM}$	-145	
Continuous source-drain diode current	$T_C = 25$ °C	$I_S$	-5	
	$T_A = 25$ °C		-2.8 <sup>b, c</sup>	
Single pulse avalanche current	$L = 0.1$ mH	$I_{AS}$	-25	mJ
Single pulse avalanche energy		$E_{AS}$	31.2	
Maximum power dissipation	$T_C = 25$ °C	$I_P$	5.6	W
	$T_C = 70$ °C		3.6	
	$T_A = 25$ °C		3.1 <sup>b, c</sup>	
	$T_A = 70$ °C		2 <sup>b, c</sup>	
Operating junction and storage temperature range		$T_J, T_{stg}$	-55 to +150	°C
Soldering recommendations (peak temperature) <sup>c</sup>			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		SYMBOL	TYPICAL	MAXIMUM	UNIT
Maximum junction-to-ambient <sup>b</sup>	$t \leq 10$ s	$R_{thJA}$	34	40	°C/W
Maximum junction-to-case (drain)	Steady state	$R_{thJF}$	18	22	

#### Notes

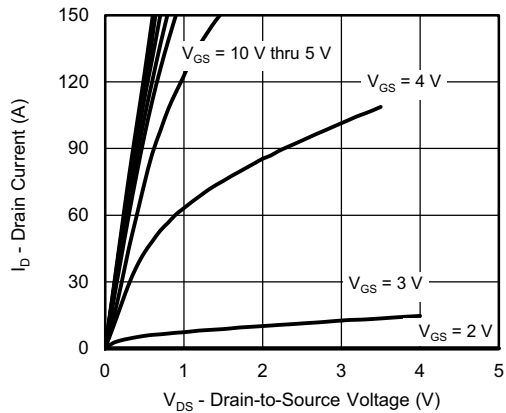
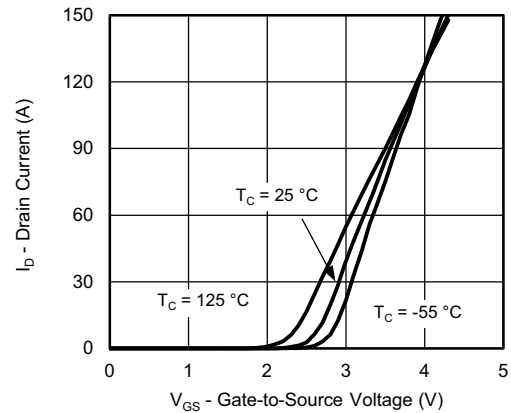
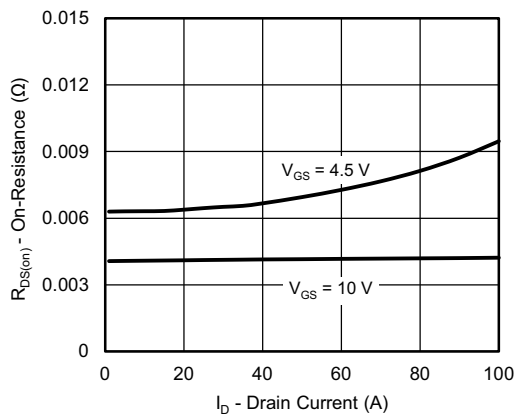
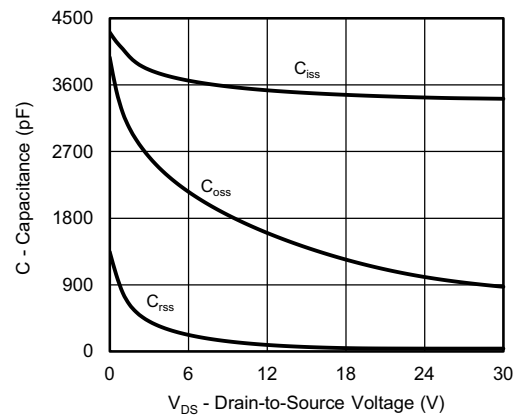
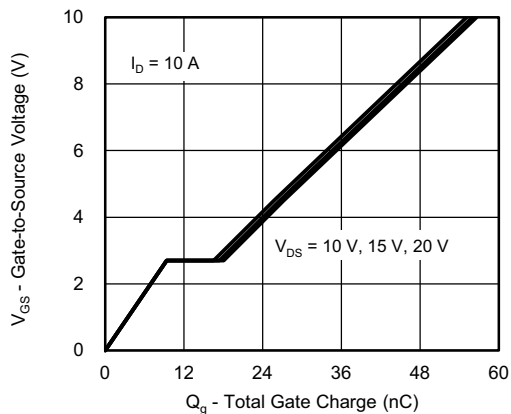
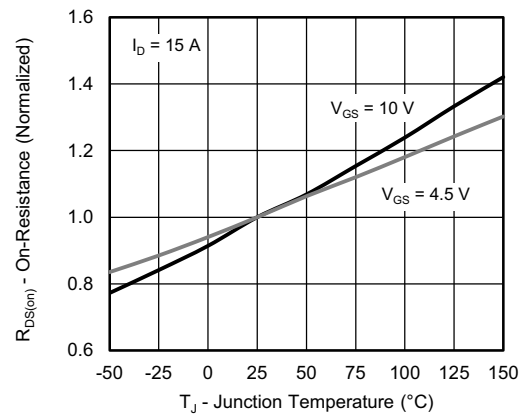
- Package limited
- Surface mounted on 1" x 1" FR4 board
- $t = 10$  s
- The SO-8 is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
- Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
- Maximum under steady state conditions is 85 °C/W
- $T_C = 25$  °C

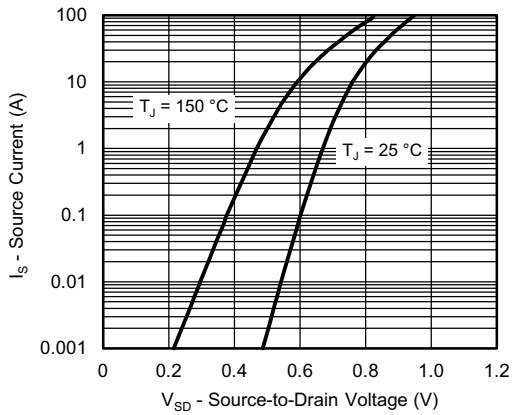
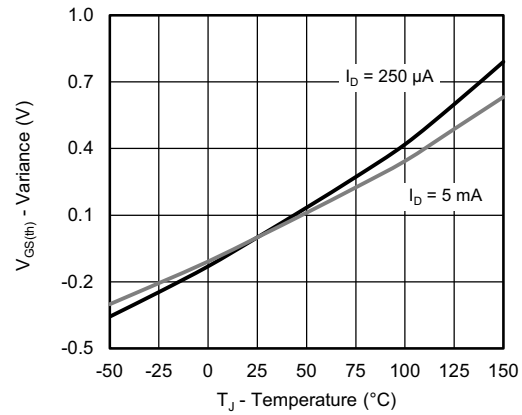
SPECIFICATIONS (T <sub>J</sub> = 25 °C, unless otherwise noted)						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Static						
Drain-source breakdown voltage	V <sub>DS</sub>	V <sub>GS</sub> = 0 V, I <sub>D</sub> = -250 μA	-30	-	-	V
V <sub>DS</sub> temperature coefficient	ΔV <sub>DS</sub> /T <sub>J</sub>	I <sub>D</sub> = -10 mA	-	-17	-	mV/°C
V <sub>GS(th)</sub> temperature coefficient	ΔV <sub>GS(th)</sub> /T <sub>J</sub>	I <sub>D</sub> = -250 μA	-	5.5	-	
Gate-source threshold voltage	V <sub>GS(th)</sub>	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μA	-1	-	-2.2	V
Gate-source leakage	I <sub>GSS</sub>	V <sub>DS</sub> = 0 V, V <sub>GS</sub> = +16 / -20 V	-	-	100	nA
Zero gate voltage drain current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V	-	-	-1	μA
		V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V, T <sub>J</sub> = 70 °C	-	-	-15	
On-state drain current <sup>a</sup>	I <sub>D(on)</sub>	V <sub>DS</sub> ≥ -10 V, V <sub>GS</sub> = -10 V	-40	-	-	A
Drain-source on-state resistance <sup>a</sup>	R <sub>DS(on)</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -15 A	-	0.0050	-	Ω
		V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -10 A	-	0.0080	-	
Forward transconductance <sup>a</sup>	g <sub>fs</sub>	V <sub>DS</sub> = -15 V, I <sub>D</sub> = -15 A	-	81	-	S
Dynamic <sup>b</sup>						
Input capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = 0 V, f = 1 MHz	-	3490	-	pF
Output capacitance	C <sub>oss</sub>		-	1420	-	
Reverse transfer capacitance	C <sub>rss</sub>		-	70	-	
Total gate charge	Q <sub>g</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -10 V, I <sub>D</sub> = -10 A	-	56	84	nC
Gate-source charge	Q <sub>gs</sub>	V <sub>DS</sub> = -15 V, V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -10 A	-	27	41	
Gate-drain charge	Q <sub>gd</sub>		-	9.4	-	
Gate resistance	R <sub>g</sub>	f = 1 MHz	-	8.2	-	
Turn-on delay time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 1.5 Ω, I <sub>D</sub> ≅ -10 A, V <sub>GEN</sub> = -10 V, R <sub>g</sub> = 1 Ω	1.5	3.5	6	Ω
Rise time	t <sub>r</sub>		-	15	30	ns
Turn-off delay time	t <sub>d(off)</sub>		-	6	12	
Fall time	t <sub>f</sub>		-	39	78	
Turn-on delay time	t <sub>d(on)</sub>	-	10	20		
Rise time	t <sub>r</sub>	V <sub>DD</sub> = -15 V, R <sub>L</sub> = 1.5 Ω, I <sub>D</sub> ≅ -10 A, V <sub>GEN</sub> = -4.5 V, R <sub>g</sub> = 1 Ω	-	34	68	
Turn-off delay time	t <sub>d(off)</sub>	-	86	172		
Fall time	t <sub>f</sub>	-	31	62		
		-	22	44		
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I <sub>S</sub>	T <sub>C</sub> = 25 °C	-	-	-5	A
Pulse diode forward current	I <sub>SM</sub>		-	-	-150	
Body diode voltage	V <sub>SD</sub>	I <sub>S</sub> = -5 A, V <sub>GS</sub> = 0 V	-	-0.73	-1.1	V
Body diode reverse recovery time	t <sub>rr</sub>	I <sub>F</sub> = -10 A, di/dt = 100 A/μs, T <sub>J</sub> = 25 °C	-	44	88	ns
Body diode reverse recovery charge	Q <sub>rr</sub>		-	41	82	nC
Reverse recovery fall time	t <sub>a</sub>		-	19	-	ns
Reverse recovery rise time	t <sub>b</sub>		-	25	-	

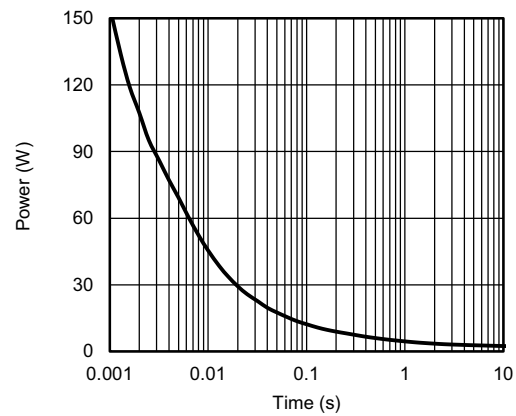
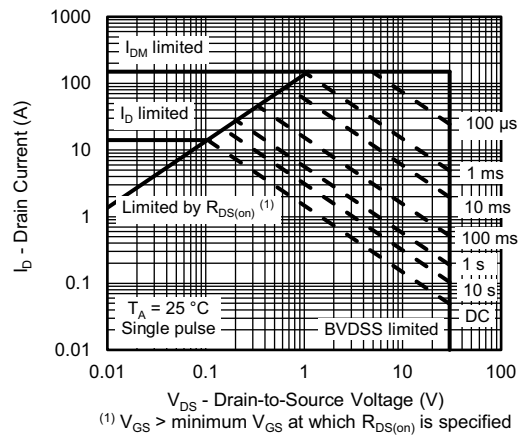
**Notes**

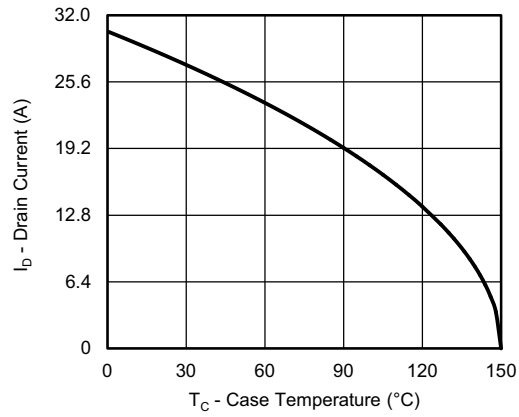
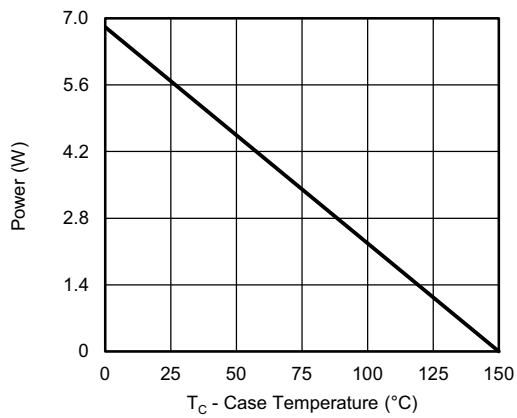
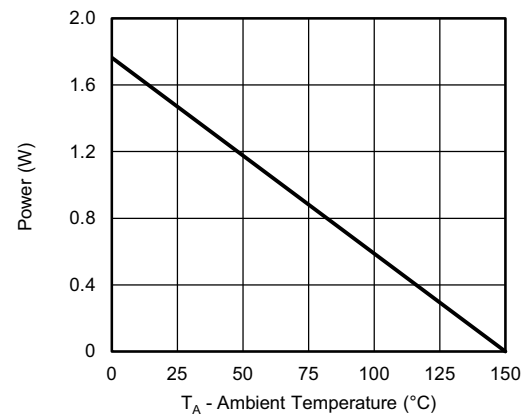
- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$   
 b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

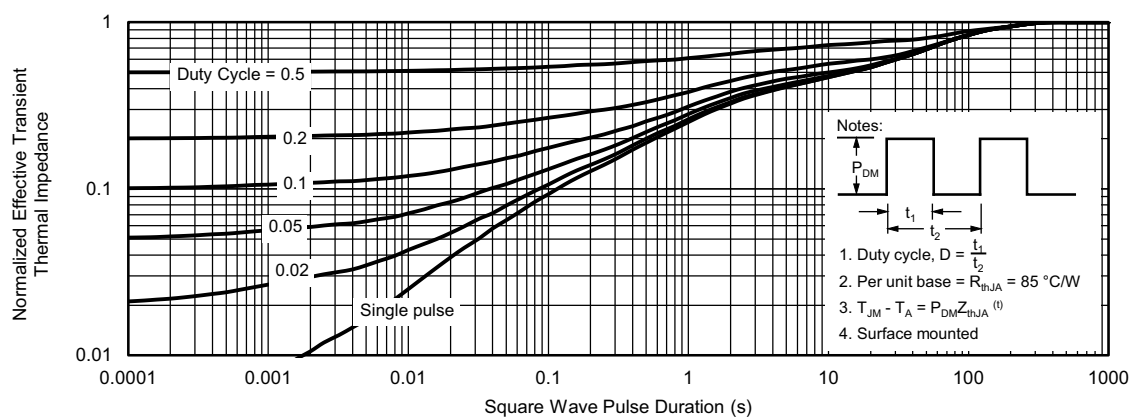
**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Output Characteristics**

**Transfer Characteristics**

**On-Resistance vs. Drain Current and Gate Voltage**

**Capacitance**

**Gate Charge**

**On-Resistance vs. Junction Temperature**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Source-Drain Diode Forward Voltage**

**Threshold Voltage**

**On-Resistance vs. Gate-to-Source Voltage**

**Single Pulse Power, Junction-to-Ambient**

**Safe Operating Area, Junction-to-Ambient**

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Current Derating <sup>a</sup>**

**Power, Junction-to-Case**

**Power, Junction-to-Ambient**
**Note**

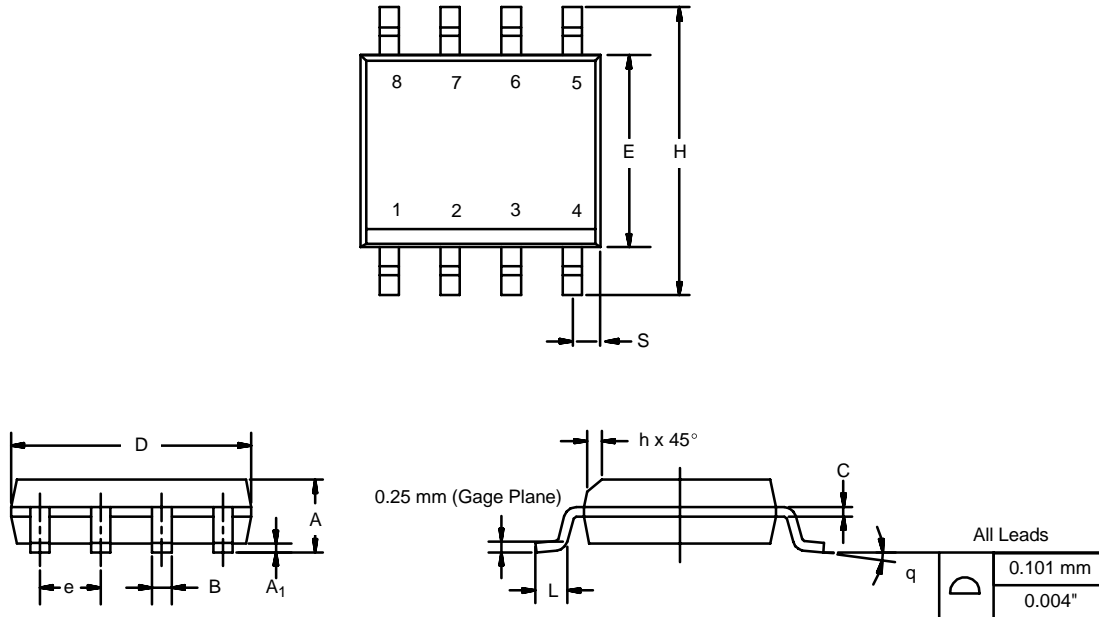
- a. The power dissipation  $P_D$  is based on  $T_J \text{ max.} = 150^\circ\text{C}$ , using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

**TYPICAL CHARACTERISTICS** (25 °C, unless otherwise noted)

**Normalized Thermal Transient Impedance, Junction-to-Ambient**

**Normalized Thermal Transient Impedance, Junction-to-Case**

**SOIC (NARROW): 8-LEAD**

JEDEC Part Number: MS-012



DIM	MILLIMETERS		INCHES	
	Min	Max	Min	Max
A	1.35	1.75	0.053	0.069
A <sub>1</sub>	0.10	0.20	0.004	0.008
B	0.35	0.51	0.014	0.020
C	0.19	0.25	0.0075	0.010
D	4.80	5.00	0.189	0.196
E	3.80	4.00	0.150	0.157
e	1.27 BSC		0.050 BSC	
H	5.80	6.20	0.228	0.244
h	0.25	0.50	0.010	0.020
L	0.50	0.93	0.020	0.037
q	0°	8°	0°	8°
S	0.44	0.64	0.018	0.026
ECN: C-06527-Rev. I, 11-Sep-06 DWG: 5498				

## RECOMMENDED MINIMUM PADS FOR SO-8



Recommended Minimum Pads  
Dimensions in Inches/(mm)



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