Final COM'L

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PAL20R8 Family

24-pin TTL Programmable Array Logic

DISTINCTIVE CHARACTERISTICS

- As fast as 7.5 ns maximum propagation delay
- Popular 24-pin architectures: 20L8, 20R8, 20R6, 20R4
- Programmable replacement for high-speed TTL logic
- Power-up reset for initialization

GENERAL DESCRIPTION

The PAL20R8 Family (PAL20L8, PAL20R8, PAL20R6, PAL20R4) is AMD's standard 24-pin PAL device family. The devices provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at a reduced chip count.

The family allows the systems engineer to implement the design on-chip, by opening fuse links to configure AND and OR gates within the device, according to the desired logic function. Complex interconnections between gates, which previously required time-consuming layout, are lifted from the PC board and placed on silicon, where they can be easily modified during prototyping or production.

The PAL device implements the familiar Boolean logic transfer function, the sum of products. The PAL device is a programmable AND array driving a fixed OR array. The AND array is programmed to create custom product terms, while the OR array sums selected terms at the outputs.

- Easy design with PALASM[®] software
- Programmable on standard PAL® device programmers
- 24-pin SKINNYDIP® and 28-pin PLCC packages save space

In addition, the PAL device provides the following options:

- Variable input/output pin ratio
- Programmable three-state outputs
- Registers with feedback ---



Product terms with all connections opened assume the logical HIGH state; product terms connected to both true and complement of any single input assume the logical LOW state. Registers consist of D-type flip-flops that are loaded on the LOW-to-HIGH transition of the clock. Unused input pins should be tied to Vcc or GND.

The entire PAL device family is supported by the PALASM software package. The PAL family is programmed on conventional PAL device programmers with appropriate personality and socket adapter modules. See the Programmer Reference Guide for approved programmers. Once the PAL device is programmed and verified an additional connection may be opened to prevent pattern readout. This feature secures proprietary circuits.

DEVICE	DEDICATED INPUTS	OUTPUTS	PRODUCT TERMS/ OUTPUT	FEEDBACK	ENABLE
PAL20L8	14	6 comb. 2 comb.	777	1/O _	prog. prog.
PAL20R8	12	8 reg.	8	reg.	pin
PAL20R6	12	6 reg. 2 comb.	8 7	reg. I/O	pin prog.
PAL20R4	12	4 reg. 4 comb.	8 7	reg. I/O	pin prog.

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Publication # 10294	Rev. B	Amendment /0
Issue Date: January 1	990	
		2-107



Advanced Micro

Devices

T-46-19-13

T-46-19-13

PERFORMANCE OPTIONS

(Commercial) 35 A-2 25 B-2 A (tpp, ns) 15 B 10 -10 7.5 -7 105 210

Power (Icc, mA)

Note:

For low power and high speed, the EE CMOS PALCE20V8 can directly replace the PAL20R8 Family.

OPERATING RANGES

Commercial	Military
-7	-12
-10	-15
B (15 ns)	B (20 ns)
B-2 (25 ns)	
A (25 ns)	A (30 ns)
A-2 (35 ns)	A-2 (50 ns)



12350-001A



PAL20R8 Family



12350-003A



2-110

CONNECTION DIAGRAMS Top View

SKINNYDIP/FLATPACK



12350-005A

Note	20L8	20R8	20R6	20R4
1	lo	CLK	CLK	CLK
2	113	ŌĒ	ŌĒ	ŌĒ
3	O1	O1	I/O ₁	I/O1
4	I/O2	O ₂	O ₂	I/O2
5	I/O3	O3	O3	O ₃
6	1/O₄	O4	O₄	O₄
7	I/O5	O ₅	O5	O5
8	I/O ₆	O ₆	O ₆	O ₆
9	I/O7	O7	O7	I/O7
10	O ₈	O8	1/O ₈	I/O8

PIN DESIGNATIONS

CLK	Clock
GND	Ground
1	Input
I/O	Input/Output
NC	No Connect
0	Output
OE	Output Enable
Vcc	Supply Voltage

PLCC/LCC JEDEC: Applies to -7(-12 mil), -10(-15 mil), B-2 Series Only 6 (NÓTE 9) 13 (NOTE 8). 14 🗋 24 23 (NOTE 7) ۱_s[22 NC 16 🗋 (NOTE 6) 21 가 20 (NOTE 4) ЪΕ <u>s</u> <u>s</u> <u>s</u> <u>s</u> <u>s</u> NOTE 3) 12350-006A

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PLCC Applies to B, A, A-2 Series Only





LCC Applies to B, A, A-2 Series Only



Note: Pin 1 is marked for orientation.

PAL20R8 Family

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ORDERING INFORMATION Commercial Products (AMD Marking Only)

T-46-19-13

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of:

- a. Family Type b.
 - Number of Array Inputs
- c. **Output Type** d. Number of Outputs
- Speed
- θ.
- f. Package Type g. Operating Conditions h. Optional Processing



Valid Combinations			
PAL20L8			
PAL20R8	7 10		
PAL20R6	-7, -10	PC, JC, DC	
PAL20R4			

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with AMD logo.

2-112

ORDERING INFORMATION

Commercial Products (MMI Marking Only)

T-46-19-13

AMD programmable logic products for commercial applications are available with several ordering options. The order number (Valid Combination) is formed by a combination of: a. Family Type

- b.
 - Number of Array Inputs
- Output Type Number of Outputs c. d.
- Speed
- е. f. Power
- Operating Conditions Package Type Optional Processing g. h.
- ١.



Valid Combinations				
PAL20L8, B-2 CNS, CFN, CJS				
PAL20R8,				
PAL20R6,	B, A,	CNS, CNL, CJS		
PAL20R4	A∙2			

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device, Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

PAL20R8 Family

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Valid Combinations				
PAL20L8				
PAL20R8	-12,			
PAL20R6	-15	/BLA, /B3A		
PAL20R4				

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

2-114

PAL20R8 Family

Valid Combinations

The Valid Combinations table lists configurations planned to be supported in volume for this device. . Consult the local AMD sales office to confirm availability of specific valid combinations, to check on newly released combinations, and to obtain additional data on AMD's standard military grade products.

Note: Marked with AMD logo.

ORDERING INFORMATION APL Products (MMI Marking Only)

T-46-19-13

AMD programmable logic products for Aerospace and Defense applications are available with several ordering options. APL (Approved Products List) products are fully compliant with MIL-STD-883 requirements. The order number (Valid Combination) is formed by a combination of: a. Family Type

A. Family Type b. Number of Array Inputs c. Output Type d. Number of Outputs e. Speed f. Power g. Operating Conditions h. Package Type I. Optional Processing PAL 20 R 8 A -2 M JS /883B



- ARRAY INPUTS
- c. OUTPUT TYPE · R = Registered
 - L = Active-Low Combinatorial
- d. NUMBER OF OUTPUTS -----
- e. SPEED B = Very High Speed (20 ns t_{PD}) A = High speed (30–50 ns t_{PD})
- f. POWER
 - Blank = Full Power (210 mA lcc) -2 = Half Power (105 mA lcc)
 - -2 = Half Power (105 mA lcc)

Valid Combinations				
PAL20L8 MJS/883B,				
PAL20R8	B, A,	MW/883B,		
PAL20R6	A-2	ML/883B		
PAL20R4				





The Valid Combinations table lists configurations planned to be supported in volume for this device. Consult the local AMD sales office to confirm availability of specific valid combinations, and to check on newly released combinations.

Note: Marked with MMI logo.

Group A Tests

Group A Tests consist of Subgroups: 1, 2, 3, 7, 8, 9, 10, 11.

Military Burn-In

Military burn-in is in accordance with the current revision of MIL-STD-883, Test Methods 1015, Conditions A through E. Test conditions are selected at AMD's option.

PAL20R8 Family

FUNCTIONAL DESCRIPTION Standard 24-pin PAL Family

The standard 24-pin PAL family is comprised of four different devices, including both registered and combinatorial devices. All parts are produced with a fuse link at each input to the AND gate array, and connections may be selectively removed by applying appropriate voltages to the circuit. Utilizing an easily-implemented programming algorithm, these products can be rapidly programmed to any customized pattern. Information on approved programmers can be found in the Programmer Reference Guide. Extra test words are pre-programmed during manufacturing to ensure extremely high field programming yields, and provide extra test paths to achieve excellent parametric correlation.

Variable Input/Output Pin Ratio

The registered devices have twelve dedicated input lines, and each combinatorial output is an I/O pin. The PAL20L8 has fourteen dedicated input lines, and only six of the eight combinatorial outputs are I/O pins. Buffers for device inputs have complementary outputs to provide user-programmable input signal polarity. Unused input pins should be tied to Vcc or GND.

Programmable Three-State Outputs

Each output has a three-state output buffer with threestate control. On combinatorial outputs, a product term controls the buffer, allowing enable and disable to be a function of any product of device inputs or output feedback. The combinatorial output provides a bidirectional I/O pin, and may be configured as a dedicated input if the buffer is always disabled. On registered outputs, an input pin controls the enabling of the three-state outputs.

Registers with Feedback

Registered outputs are provided for data storage and synchronization. Registers are composed of D-type flipflops that are loaded on the LOW-to-HIGH transition of the clock input.

Power-Up Reset

All flip-flops power-up to a logic LOW for predictable system initialization. Outputs of the PAL20R8 Family will be HIGH due to the active-low outputs. The Vcc rise must be monotonic and the reset delay time is 1000 ns maximum.

Register Preload

T-46-19-13

Applies to -7 (-12 Mil), -10 (-15 Mil), Series Only

The register on the listed Series can be preloaded from the output pins to facilitate functional testing of complex state machine designs. This feature allows direct loading of arbitrary states, making it unnecessary to cycle through long test vector sequences to reach a desired state. In addition, transitions from illegal states can be verified by loading illegal states and observing proper recovery.

Security Fuse

After programming and verification, a PAL20R8 Family design can be secured by programming the security fuse. Once programmed, this fuse defeats readback of the internal programmed pattern by a device programmer, securing proprietary designs from competitors. When the security fuse is programmed, the array will read as if every fuse is unprogrammed. An exception is the -7 (-12 Mil) Series, where the array will read as if every fuse is programmed.

Pinouts

All members of the PAL20R8 Family have the same SKINNYDIP pinouts independent of technology, performance, and operating conditions. Because the 24-pin SKINNYDIP requires four no-connects when mapped into the 28-pin PLCC/LCC packages, the PLCC/LCC pinouts can vary.

Two different PLCC pinouts are offered. Newer devices and all future devices will follow the JEDEC electronics committee's standard pinout ("JEDEC pinout") with noconnects on pins 1, 8, 15, and 22. The devices following this pinout are the -7, -10, and B-2 Series. Older devices retain their original pinouts, with no-connects on pins 5, 8, 11, and 19. These include the B, A, and A-2 Series.

PAL20R8 Family devices with the MMI marking indicate the PLCC pinout by the package designator. FN indicates JEDEC, and NL indicates non-JEDEC. Devices with the AMD marking all follow the JEDEC pinout.

Two different LCC pinouts are offered for military products. Newer devices and all future devices will follow the JEDEC pinout with no-connects on pins 1, 8, 15, and 22. These include the -12 and -15 Series. Older devices retain their original pinouts, with no-connects on pins 4, 11, 18, and 25. These include the B, A, and A-2 Series.

Series	Com'i PLCC No-connects	Mil LCC No-connects
-7, -10, B-2	1, 8, 15, 22 (JEDEC)	N/A
-12, -15	N/A	1, 8, 15, 22 (JEDEC)
B, A, A-2	5, 8, 11, 19	4, 11, 18, 25

Quality and Testability

The PAL20R8 Family offers a very high level of built-in quality. Extra programmable fuses provide a means of verifying performance of all AC and DC parameters. In addition, this verifies complete programmability and functionality of the device to provide the highest programming yields and post-programming functional yields in the industry.

T-46-19-13

Technology

The high-speed -7 (-12 Mil) and -10 (-15 Mil) Series are fabricated with AMD's advanced oxide-isolated bipolar process. This process reduces parasitic capacitances and minimum geometries to provide higher performance. The array connections are formed with proven PtSi fuses for the -7 and TiW fuses for the -10. The B, B-2, A, and A-2 Series are fabricated with AMD's junction-isolated process, utilizing TiW fuses.



PAL20R8 Family

LOGIC DIAGRAM DIP (JEDEC PLCC and LCC) Pinouts See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

T-46-19-13



2-118

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T-46-19-13

LOGIC DIAGRAM

DIP (JEDEC PLCC and LCC) Pinouts

See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts



LOGIC DIAGRAM DIP (JEDEC PLCC and LCC) Pinouts See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts





DIP (JEDEC PLCC and LCC) Pinouts See Connection Diagrams for B, A, A-2 Series PLCC/LCC Pinouts

T-46-19-13



PAL20R8 Family

- 2

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ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.2 V to Vcc + 0.5 V
DC Output or I/O Pin Voltage	-0.5 V to Vcc + 0.5 V
Static Discharge Voltage	2001 V

OPERATING RANGES

Commercial (C) Devices Ambient Temperature (T_A) Operating in Free Air Supply Voltage (V_{CC}) with Respect to Ground

T-46-19-13

0°C to +75°C

+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	$\label{eq:loh} \begin{array}{l} l_{OH} = -3.2 \text{ mA} V_{IN} = V_{IH} \text{ or } V_{IL} \\ V_{CC} = Min. \end{array}$	2.4		V
VOL	Output LOW Voltage	$I_{OL} = 24 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	·	0.5	V
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
ViL	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all inputs (Note 1)		0.8	v
V	Input Clamp Voltage	$I_{IN} = -18 \text{ mA}, V_{CC} = Min.$		-1.2	v
<u>lin</u>	Input HIGH Current	V _{IN} = 2.7 V, V _{CC} = Max. (Note 2)		25	μA
lıı,	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 2)		-250	μΑ
li –	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.	<u> </u>		mA
lozh	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7 V$, $V_{CC} = Max$. $V_{IN} = V_{IH} \text{ or } V_{IL}$ (Note 2)		100	μA
lozl	Off-State Output Leakage Current LOW	Vout = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
Isc	Output Short-Circuit Current	Vour = 0.5 V, Vcc = Max. (Note 3)	-30	-130	mA
	Supply Current	$V_{IN} = 0 V$, Outputs Open ($I_{OUT} = 0 mA$) $V_{CC} = Max$.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.

2. I/O pin leakage is the worst case of $I_{\rm IL}$ and $I_{\rm OZL}$ (or $I_{\rm IH}$ and $I_{\rm OZH}$).

Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

2-122

PAL20R8-7 Series (Com'i)

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CAPACITANCE (Note ⁻	11

CAPACITA	NCE (Note 1)	T-46-19-13	3		
Parameter Symbol	Parameter Description	Test Conditions	3	Тур.	Unit
Cin	Input Capacitance	V _{IN} = 2.0 V	$V_{CC} = 5.0 V$ $T_A = +25^{\circ}C$	7	- 5
Солт	Output Capacitance	V _{OUT} = 2.0 V	$f_A = +25^{\circ}C$ f = 1 MHz	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Parameter Symbol	Parameter Des	cription			Min. (Note 3)	Max.	Unit	
tpd	Input or Feedba Combinatorial C		1 Output Switching		20L8, 20R6 20R4	<u>3</u> 3	7.5 7	ns
ts	Setup Time from	n Input or Feedba	ack to	Clock		7		ns
tн	Hold Time					0		ns
tco	Clock to Output	· · · · · · · · · · · · · · · · · · ·				3	6.5	ns
tCF	Clock to Feedb	ack (Note 4)					3	ns
tskew	Skew Between	Registered Outputs (Note 5)			20R8, 20R6,		1	ns
twL	Clock Width	LOW	LOW		20R4	5		ns
twн		HIGH				5		ns
	Maximum	External Feed	lback	1/(ts + tco)		74		MHz
fmax	Frequency	Internal Feed	back	$1/(t_{S} + t_{CF})$		100		MHz
	(Note 6)	No Feedback		1/(twн + tw⊾)		100		MHz
tezx	OE to Output E	nable				3	8	ns
texz	OE to Output D	isable				3	8	ns
tEA	Input to Output	Enable Using Pr	oduct -	Term Control	20L8, 20R6	3	10	ns
ten	Input to Output	Disable Using Pr	oduct	Term Control	20R4	3	10	ns



Notes:

2. See Switching Test Circuit for test conditions.

3. Output delay minimums are measured under best-case conditions.

4. Calculated from measured fMAX internal.

5. Skew is measured with all outputs switching in the same direction.

6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

PAL20R8-7 Series (Com'i)

ADV MICRO PLA/PLE/ARRAYS 28E D M 0257526 0029460 3 M AMD2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	-1.2 V to Vcc + 0.5 V
DC Output or I/O Pin Voltage	-0.5 V to V _{CC} + 0.5 V
Static Discharge Voltage	2001 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested. OPERATING RANGES Military (M) Devices (Note 1)

Operating Case (T_C) Temperature Supply Voltage (V_{CC}) with Respect to Ground

-55°C to +125°C

T-46-19-13

+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at Tc = +25°C , +125°C, and -55°C per MIL-STD-883.



Note 2)		A REAL STREET				
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit	
V _{OH}	Output HIGH Voltage	$V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	2.4		V.	
VOL	Output LOW Voltage	$\dot{O}_{L} = 12 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$		0.5	v	
VIH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V	
ViL	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	· V	
Vi	Input Clamp Voltage	$I_{IN} = -18 \text{ mA}, V_{CC} = \text{Min.}$		-1.2	v	
- IIH	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 4)		25	μA	
hr.	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 4)		-250	μA	
lı –	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		1	mA	
Іогн	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4 \text{ V}, V_{CC} = \text{Max.}$ $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		100	μA	
I _{OZL}	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4 \text{ V}, V_{CC} = \text{Max.}$ $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		100	μA	
Isc	Output Short-Circuit Current	Vout = 0.5 V, Vcc = Max. (Note 5)	-30	-130	mA	
lcc	Supply Current	$V_{IN} = 0$ V, Outputs Open ($I_{OUT} = 0$ mA) $V_{CC} = Max$.		210	mA	

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2)

Notes:

V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with
respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values
without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).

5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

2-124

PAL20R8-12 Series (Mil)

^{2.} For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

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CARACITANCE (Note 1)

CAPACITANCE (Note 1)					-13
Parameter Symbol	Parameter Description	Test Conditions	5	Тур.	Unit
CiN	Input Capacitance	V _{IN} = 2.0 V	V _{CC} = 5.0 V	9	· · · ·
Солт	Output Capacitance	V _{OUT} = 2.0 V	T _A = +25°C f = 1 MHz	10	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

Parameter Symbol	Parameter Description					Min. (Note 3)	Max.	Unit
tpd	Input or Feedback Combinatorial Ou		20L8, 20R6 1 Output Switching 20R4			3	12.5 12	ns
ts	Setup Time from	Input or Fe	out or Feedback to Clock			્રી2 ઁ		ns
tн	Hold Time	ne			0		ns	
tco	Clock to Output	ANNAL				3	11	ns
tcr	Clock to Feedback (Note 4)					6.5	ns	
tskew	Skew Between R	v Between Registered Outputs (Note 5)					1	ns
twL	Clock Width	LOW	4	19	20R8, 20R6	10		ns
twн		ңі́бн	6 2 1		20R4	8		ns
	Maximum	External	Feedback	1/(ts + tco)		43.4		MHz
f MAX	Frequency	Internal F	eedback	$1/(t_{S} + t_{CF})$]	54		MHz
	(Note 6)	No Feedt	back	1/(twn + twl)]	55.5		MHz
tezx	OE to Output Ena	able (Note	7)	· · · · · · · · · · · · · · · · · · ·]	3	20	'ns
texz	OE to Output Dis	able (Note	7)]	3	20	ns
t _{EA}		Input to Output Enable Using Product Term Control (Note 7)			20L8, 20R6	3	20	ns
ter	Input to Output D Term Control (No		g Product		20R4	3	20	ns

Notes:

- 2. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- 3. Minimum value for tPD, tCO, tPZX, tPXZ, tEA, and tER parameters should be used for simulation purposes only and are not tested.
- 4. Calculated from measured fMAX internal.
- 5. Skew is measured with all outputs switching in the same direction.
- 6. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
- 7. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

PAL20R8-12 Series (Mil)



Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where tep may be affected.

2-126

PAL20R8-7/12 Series (Com'l/Mil)

ADV MICRO PLA/PLE/ARRAYS 28E D BB 0257526 0029463 9 BB AMD2

CURRENT VS. VOLTAGE (I-V) CHARACTERISTICS $V_{CC} = 5.0 \text{ V}, T_A = 25^{\circ}\text{C}$





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10240-004A









PAL20R8-7/12 Series (Com'l/Mil)

ADV MICRO PLA/PLE/ARRAYS 28E D MM 0257526 0029464 0 MMAMD2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	-0.5 V to V _{CC} + 0.5 V
DC Output or I/O Pin Voltage	-0.5 V to Vcc Max.
DC Input Current	-30 mA to +5 mA

OPERATING RANGES Commercial (C) Devices

Ambient Temperature (T_A) Operating in Free Air Supply Voltage (V_{cc}) with Respect to Ground T-46-19-13

0°C to +75°C

+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	$I_{OH} = -3.2 \text{ mA} V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	2.4		V
Vol	Output LOW Voltage	$l_{OL} = 24 \text{ mA} \qquad V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$		0.5	۷
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0	· · · · ·	V
ViL	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	۷
V	Input Clamp Voltage	$I_{IN} = -18 \text{ mA}, V_{CC} = \text{Min}.$		-1.5	V
lін	Input HIGH Current	VIN = 2.7 V, Vcc = Max. (Note 2)		25	μA
hi.	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 2)		-250	μA
lı	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		100	μA
l _{OZH}	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7 V$, $V_{CC} = Max$. $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 2)}$		100	μA
lozi	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4 V$, $V_{CC} = Max$. $V_{IN} = V_{IH} \text{ or } V_{IL} (Note 2)$		-100	μA
lsc	Output Short-Circuit Current	Vour = 0.5 V, Vcc = Max. (Note 3)	-30	130	mA
lcc	Supply Current	$V_{IN} = 0 V$, Outputs Open ($I_{OUT} = 0 mA$) $V_{CC} = Max$.		210	mA

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.

2. I/O pin leakage is the worst case of $I_{\rm H}$ and $I_{\rm OZL}$ (or $I_{\rm IH}$ and $I_{\rm OZH}$).

3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

PAL20R8-10 Series (Com'l)

C257526 0029465 2 MAMD2 ADV MICRO PLA/PLE/ARRAYS 28E D

CAPACITANCE (Note 1)

CAPACITANCE (Note 1) T-						-13
Parameter Symbol	Parameter Description	Test Conditio	ons	 _ [Тур.	Unit
CiN	Input Capacitance	V _{IN} = 2.0 V	$V_{CC} = 5.0 V$ $T_A = 25^{\circ}C$	CLK, OE Other Inputs	12 7	75
Солт	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	Outputs	8	pF

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified

where capacitance may be affected.

Parameter Symbol	Parameter Des	cription			Min. (Note 3)	Max.	Unit
tpp	Input or Feedba Combinatorial (20L8, 20R6 20R4	3	10	ns
ts	Setup Time fro	m Input or Feedback to	Clock		10		ns
tн	Hold Time				0	:	ns
tco	Clock to Outpu	t			2	8	ns
tcF	Clock to Feedb	ack (Note 4)	20R8, 20R6		7	ns	
twL	Clock Width	LOW		20R4	7		ns
twn		HIGH			7		ПŚ
	Maximum	External Feedback	1/(ts + tco)		55.5	-	MHz
fmax	Frequency	Internal Feedback	$1/(t_{S} + t_{CF})$		58.8		MHz
	(Note 5)	No Feedback	1/(t _{WH} + t _{WL})		71.4		MHz
tezx	OE to Output E	nable			1	10	ns
texz	OE to Output D	visable			1	10	ns
tEA	Input to Output	Enable Using Product	Term Control	20L8, 20R6	3	10	ns
ten	Input to Output	Disable Using Product	Term Control	20R4	3	10	ns

Notes:

2. See Switching Test Circuit for test conditions.

3. Output delay minimums are measured under best-case conditions.

4. Calculated from measured f_{MAX} internal.

5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where the frequency may be affected.

PAL20R8-10 Series (Com'l)

ADV MICRO PLA/PLE/ARRAYS 28E D

ABSOLUTE MAXIMUM RATINGSStorage Temperature-65°C to +150°CAmbient Temperature-55°C to +125°Cwith Power Applied-55°C to +125°CSupply Voltage with-0.5 V to +7.0 VPC Input Voltage-0.5 V to +7.0 VDC Input Voltage-0.5 V to +5.5 VDC Output or I/O Pin Voltage-0.5 V to Vcc Max.DC Input Current-30 mA to + 5 mA

S OPERATING RANGES 0+150°C Military (M) Devices (Note 1) Ambient Temperature (T_A) Operating in Free Air

Operating Case (Tc)

Supply Voltage (Vcc)

with Respect to Ground

Temperature

T-46-19-13

(1A) --55°C Min. +125°C Max.

0257526 0029466 4 **68** AMD2

+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

 Military products are tested at Tc = +25°C, +125°C, and -55°C per MIL-STD-883.

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified (Note 2) Parameter **Parameter Description** Symbol **Test Conditions** Min. Max. Unit Vон **Output HIGH Voltage** $I_{OH} = -2 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ 2.4 v V_{CC} = Min. Vol Output LOW Voltage loL = 12 mA VIN = VIH or VIL 0.5 v Vcc = Min. Vін Input HIGH Voltage Guaranteed Input Logical HIGH 2.0 v Voltage for all Inputs (Note 3) ViL Input LOW Voltage Guaranteed Input Logical LOW 0.8 V Voltage for all Inputs (Note 3) Vi Input Clamp Voltage $I_{IN} = -18 \text{ mA}, V_{CC} = \text{Min}.$ -1.5 v Iн Input HIGH Current VIN = 2.4 V, Vcc = Max. (Note 4) 25 μA Input LOW Current hι VIN = 0.4 V, Vcc = Max. (Note 4) -250 μA h Maximum Input Current $V_{IN} = 5.5 V$, $V_{CC} = Max$. 100 μA Off-State Output Leakage Іогн $V_{OUT} = 2.7 V$, $V_{CC} = Max$. 100 μA Current HIGH VIN = VIH or VIL (Note 4) lozu Off-State Output Leakage Vour = 0.4 V, Vcc = Max. -100 μA Current LOW $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$ **Output Short-Circuit Current** lsc Vour = 0.5 V, Vcc = Max. (Note 5) -30 -130 mA lcc Supply Current V_{IN} = 0 V, Outputs Open (I_{OUT} = 0 mA) 210 mΑ Vcc = Max.

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. VIL and VIH are input conditions of output tests and are not themselves directly tested. VIL and VIH are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of IIL and IOZL (or IIH and IOZH).

Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V
has been chosen to avoid test problems caused by tester ground degradation.

2-130

PAL20R8-15 Series (Mil)

ADV MICRO PLA/PLE/ARRAYS 28E D 🔤 0257526 0029467 6 🖼 AMD2

CAPACITANCE (Note 1)

Parameter Symbol	Parameter Description	Test Conditio	ns		Тур.	Unit
C _{IN}	Input Capacitance	V _{IN} = 2.0 V	$V_{CC} = 5.0 V$	CLK, ÕË	12	
			T _A = 25°C	Other Inputs	7	٦٥
Сол	Output Capacitance	V _{OUT} = 2.0 V	f = 1 MHz	Outputs	8	

Note:

1. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where capacitance may be affected.

SWITCHING CHARACTERISTICS over MILITARY operating ranges (Note 2)

Parameter Symbol	Parameter Des	cription			Min. (Note 3)	Max.	Unit
t _{PD}	Input or Feedback to Combinatorial Output			20L8, 20R6 20R4	3	15	ns
ts	Setup Time from Input or Feedback to Clock				15		ns
tн	Hold Time				0		ns
tco	Clock to Output			2	13	ns	
t CF	Clock to Feedb	ack (Note 4)	20R8, 20R6		12	ns	
tw.	Clock Width	LOW		10		ns	
twн		HIGH		20R4	10		ns
	Maximum Frequency (Note 5)	External Feedback	1/(ts + tco)		35.7		MHz
f MAX		Internal Feedback	1/(ts + tcr)		37		MHz
		No Feedback	1/(twH + twL)		50		MHz
tpzx	OE to Output E	nable (Note 6)			1	15	ns
texz	OE to Output Disable (Note 6)				1	15	ns
t _{EA}		Input to Output Enable Using Product Term Control (Note 6)		20L8, 20R6	3	15	ns
ler	Input to Output Disable Using Product Term Control (Note 6)			20R4	3	15	ns



T-46-19-13

Notes:

 See Switching Test Circuit for test conditions. For APL products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. Minimum value for tPD, tCO, tPZX, tPXZ, tEA, and tER parameters should be used for simulation purposes only and are not tested.

4. Calculated from measured fMAX internal.

5. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

 These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

PAL20R8-15 Series (Mil)

ADV MICRO PLA/PLE/ARRAYS 28E D 🔤 0257526 0029468 8 🖼 AMD2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	–55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to Vcc + 0.5 V
DC Output or I/O Pin Voltage	-0.5 V to V _{CC} + 0.5 V

OPERATING RANGES

Commercial (C) Devices	
Ambient Temperature (T _A) Operating in Free Air	C
Supply Voltage (Vcc) with Respect to Ground	4

T-46-19-13

0°C to +75°C

+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

Parameter Symbol	Parameter Description	Test Conditions	3		
		Test Conditions	Min.	Max.	Unit
Vон	Output HIGH Voltage	Iон = -3.2 mA ViN = Viн or Vit	2.4		V
Vol	Output LOW Voltage	$I_{OL} = 24 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	Å	0.5	V
VIH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
ViL	Input LOW Voltage	Guaranteed Input Logical LOW		0.8	V
VI	Input Clamp Voltage	$l_{IN} = -18 \text{ mA}, \text{ Vcc} = Min_{P}$		-1.5	v
liH.	Input HIGH Current	VIN = 2.7 V, Vcc = Max. (Note 2)		25	μA
lı <u>r</u>	Input LOW Current	VIN = 0.4 V, Vcc = Max. (Note 2)	<u> </u>	-250	μA
<u>h</u>	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		100	μA
Іогн	Off-State Output Leakage Current HIGH	Vout = 2.7 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		100	μA
lozl	Off-State Output Leakage Current LOW	Vout = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
lsc	Output Short-Circuit Current	Vour = 0.5 V, V _{CC} = Max. (Note 3)	-30	-130	mA
lcc	Supply Current	$V_{IN} = 0 V$, Outputs Open ($I_{OUT} = 0 mA$) $V_{CC} = Max$.		210	mA

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.

2. I/O pin leakage is the worst case of $I_{\rm IL}$ and $I_{\rm OZL}$ (or $I_{\rm H}$ and $I_{\rm OZH}$).

Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

PAL20R8B Series (Com'l)

ADV MICRO PLA/PLE/ARRAYS 28E D D 0257526 0029469 T DAMD2

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Des	cription T-46	5-19-13		Min.	Max.	Unit
tpd	Input or Feedba Combinatorial C			20L8, 20R6 20R4		15	ns
ts	Setup Time from	n Input or Feedback to (Clock		15		ns
tH	Hold Time				0		ns
tco	Clock to Output	or Feedback		20R8		12	ns
twL	Clock Width	LOW		20R6	10		ns
twn		HIGH		20R4	12		ns
	Maximum	External Feedback	1/(ts + tco)		37		MHz
fmax	Frequency (Note 2)	No Feedback	1/(t _{WH} + t _{WL})	1	45	>	MHz
tpzx	OE to Output E	nable			N 65	<u>15</u>	ns
texz	OE to Output D	isable	A Ca	144	12	ns	
tea	Input to Output Enable Using Product Term Control			20L8, 20R6	and the second	18	ns
ten	Input to Output Disable Using Product Term Control			20R4		15	ns

Notes:

1. See Switching Test Circuit for test conditions

2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.



PAL20R8B Series (Com'l)

ADV MICRO PLA/PLE/ARRAYS 28E D 🔤 0257526 0029470 6

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to + 5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested.

OPERATING RANGES Military (M) Devices (Note 1) T-46-19-13 Ambient Temperature (T_A) Operating in Free Air -55°C Min. Operating Case (T_C) Temperature +125°C Max. Supply Voltage (V_{CC}) with Respect to Ground +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

SCIMA 🔤

Note:

1. Military products are tested at To = +25°C, +125°C, and -55°C per MIL-STO 883

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unii
VoH	Output HIGH Voltage	$IoH = -2^{\circ} mA \qquad V_{IN} = V_{IH} \text{ or } V_{IL} \\ V_{CC} = Min. \qquad \qquad$	2.4		V
Vol	Output LOW Voltage	$loc = 12 \text{ mA} V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	Ì	0.5	v
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
ViL	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
<u>Vı</u>	Input Clamp Voltage	$l_{IN} = -18 \text{ mA}, V_{CC} = Min.$		-1.5	v
lih	Input HIGH Current	VIN \$ 2.4 V, Vcc = Max. (Note 4)		25	 μΑ
<u>lic</u>	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 4)		-250	μA
<u>lı</u>	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.			mA
Югн	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4 V, V_{CC} = Max.$ $V_{IN} = V_{IH} \text{ or } V_{IL} (Note 4)$		100	μA
lozl	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4 V$, $V_{CC} = Max$. $V_{IN} = V_{IH}$ or V_{IL} (Note 4)		-100	μA
lsc	Output Short-Circuit Current	Vour = 0.5 V, Vcc = Max. (Note 5)	-30	-130	mA
lcc	Supply Current	$V_{IN} = 0 V$, Outputs Open (lout = 0 mA) $V_{CC} = Max$.		210	mA

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

3. V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.

4. I/O pin leakage is the worst case of I_{IL} and IozL (or I_{IH} and IozH).

 Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

2-134

PAL20R8B Series (Mil)

ADV MICRO PLA/PLE/ARRAYS 28E D 🔤 0257526 0029471 8 🖬 AMD2

Parameter Symbol	Parameter Description				Min.	Max.	Uniț	
tPD	Input or Feedba Combinatorial C			20L8, 20R6 20R4		20	ΠS	
ts	Setup Time fror	Input or Feedback to Clock			20		ns	
tн	Hold Time			0	•	ns		
tco	Clock to Output	or Feedback			15	ns		
tw.		LOW		20R8, 20R6	12		i ns	
twн	Clock Width	HIGH		20R4	12		ns	
f _{MAX}	Maximum	External Feedback	$1/(t_{\rm S} + t_{\rm CO})$		28.5		MHz	
	Frequency (Note 2)	No Feedback	1/(twn + twL)	h	41.6		MHz	
tpzx	OE to Output E	nable (Note 3)			LA M	20	ns	
texz	OE to Output D	isable (Note 3)		(PA)	KAV	20	ns].
tEA	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6	Washing of the second s	25	ns	
ten	Input to Output Term Control (1	20L8, 20R6		20	ns			

Notes:

 See Switching Test Circuit for test conditions. For APD products Group A, Subgroups 9, 10, and 11 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

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- 2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where irequency may be affected.
- These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.

PAL20R8B Series (Mil)

🖬 0257526 0029472 T 📰 AMD2 ADV MICRO PLA/PLE/ARRAYS 28E D

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	55°C to +125°C
Supply Voltage with Respect to Ground	-0.5 V to +7.0 V
DC Input Voltage	-1.5 V to Vcc + 0.5 V
DC Output or I/O Pin Voltage	-0.5 V to V _{cc} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES Commercial (C) Devices

T-46-19-13

Ambient Temperature (TA) Operating in Free Air 0°C to +75°C Supply Voltage (Vcc) with Respect to Ground

+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Voh	Output HIGH Voltage	$I_{OH} = -3.2 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	2.4		V
Vol	Output LOW Voltage	$loc = 24 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min.}$	S.	0.5	v
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		V
ViL	Input LOW Voltage	Guaranteed Input Logical LOW		0.8	V
VI	Input Clamp Voltage	In=+18 mA, Vcc = Min,	<u> </u>	-1.5	v
lін	Input HIGH Current	Vin = 2.7 V, Vcc = Max. (Note 2)		25	μA
N	Input LOW Current	VIN = 0.4 V, Vcc = Max. (Note 2)		-250	μA
l <u>ı</u>	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		100	μΑ
Іогн	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.7 V$, $V_{CC} = Max$. $V_{IN} = V_{IH}$ or V_{IL} (Note 2)		100	μA
lozl	Off-State Output Leakage Current LOW	Vout = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
lsc	Output Short-Circuit Current	Vout = 0.5 V, Vcc = Max. (Note 3)	-30	-130	mA
lcc	Supply Current	V _{IN} = 0 V, Outputs Open (I _{OUT} = 0 mA) V _{CC} = Max.		105	mA

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.

2. I/O pin leakage is the worst case of $I_{\rm IL}$ and $I_{\rm OZL}$ (or $I_{\rm IH}$ and $I_{\rm OZH}).$

3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. $V_{OUT} = 0.5 V$ has been chosen to avoid test problems caused by tester ground degradation.

PAL20R8B-2 Series (Com'l)

ADV MICRO PLA/PLE/ARRAYS 28E, D ECMA 🖬 0257526 0029473 1 🖿 AMD2

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Des	cription T-46-	-19-13		Min.	Max.	Unit
tPD	Input or Feedba Combinatorial C			20L8, 20R6 20R4		25	ns
ts	Setup Time from	n Input or Feedback to	Clock		25		ns
tн	Hold Time				0		ns
tco	Clock to Output	1				15	ns
tcr	Clock to Feedb	ack (Note 2)		20R8, 20R6		10	ns
twi	Clock Width	LOW		20R4	15		ns
twn		HIGH			15	4	ns
	Maximum	External Feedback	1/(ts + tco)		<u>⁄25</u>	A.	MHz
fmax	Frequency	Internal Feedback	$1/(t_{S} + t_{CF})$	l a	28.5	S.A.	MHz
	(Note 3)	No Feedback	1/(tw∺ + tw∟)		S3.3 🔩	مى مەربىلىكى بىلىكى بىل مەربىلىكى بىلىكى بىل	MHz
tezx	OE to Output E	nable	Ĩ		A Vienan	20	ns
texz	OE to Output D	isable	~ K		9	20	ns
tEA	Input to Output Enable Using Product Term Control			201.8, 20R6		25	ns
ter	Input to Output	Disable Using Product	Term Control	20R4 -	193.5	25	ns



Notes:

- 1. See Switching Test Circuit for test conditions.
- Calculated from measured f_{MAX} internal.
 These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected, ිම

PAL20R8B-2 Series (Com'l)

ADV MICRO PLA/PLE/ARRAYS 0257526 0029474 3 MM AMD2 28E D 5

ABSOLUTE MAXIMUM RATINGS

-65°C to +150°C
-55°C to +125°C
-0.5 V to +7.0 V
-1.5 V to V _{CC} + 0.5 V
–0.5 V to V _{CC} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliabil-

ity. Programming conditions may differ.

OPERATING RANGES	
Commercial (C) Devices	T-46-19-13
Ambient Temperature (TA)	
Operating in Free Air	0°C to +75°C
Supply Voltage (Vcc)	
with Respect to Ground	+4.75 V to +5.25 V
- ·	

Operating ranges define those limits between which the functionality of the device is guaranteed.

Parameter	1		<u>a 1895</u>	<u>2</u>	
Symbol	Parameter Description	Test Conditions	Min.	Max.	Unit
Voh	Output HIGH Voltage	$I_{OH} = -3.2 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	2.4		V
Vol	Output LOW Voltage	$t_{OL} = 24 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min.}$		0.5	v
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 1)	2.0		v
VIL	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 1)		0.8	V
Vi	Input Clamp Voltage	IN = -18 mA, Vcc = Min		-1.5	v
Ін с	Input HIGH Current	VIN = 2.7 V, Vcc = Max. (Note 2)		25	μA
ارر	Input LOW Current	VIN = 0.4 V, Vcc = Max. (Note 2)		-250	μΑ
h ·	Maximum Input Current	Vin = 5.5 V, Vcc = Max.		100	μA
lozh	Off-State Output Leakage Current HIGH	Vout = 2.7 V, Vcc = Max. VIN = VIH or VIL (Note 2)		100	μ <u>Α</u>
lozl	Off-State Output Leakage Current LOW	Vout = 0.4 V, V _{CC} = Max. V _{IN} = V _{IH} or V _{IL} (Note 2)		-100	μA
lsc	Output Short-Circuit Current	Vout = 0.5 V, Vcc = Max. (Note 3)	30	-130	mA
lcc	Supply Current	$V_{IN} = 0 V$, Outputs Open (lout = 0 mA) Vcc = Max.		210	mA

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.

2. I/O pin leakage is the worst case of IIL and IOZL (or IIH and IOZH).

3. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. VOUT = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

PAL20R8A Series (Com'I)

D257526 0029475 5 I E C M A ADV MICRO PLA/PLE/ARRAYS 28E D

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Description T-46-19-13					Max.	Unit
tpd	Input or Feedba Combinatorial (25	ns
ts	Setup Time from	m Input or Feedback to	Clock		25		ns
t _H	Hold Time			-	0		ns
tco	Clock to Output	t				15	ns
tcr	Clock to Feedb	ack (Note 2)	ck (Note 2) 20R8			10	ns
tw∟	Clock Width	LOW		20R4	15		ns
twн		HIGH			15		ns
	Maximum	External Feedback	1/(ts + tco)		25		MHz
fmax	Frequency	Internal Feedback	1/(ts + tcr)		28.5		MHz
	(Note 3)	No Feedback	1/(t _{WH} + t _{WL})		33,	and the second sec	MHz
tezx	OE to Output E	nable			C. Salar	20	ns
texz	OE to Output Disable			L 🖒		20	. NS
tea	Input to Output Enable Using Product Term Control			20L8, 20R6		25	ns
ter	Input to Output Disable Using Product Term Control			689	25	ns	



Notes:

1. See Switching Test Circuit for test conditions.

1. El

- These parameters are not 100% tested, but are calculated at initial character where frequency may be affected. ization and at any time the design is modified

PAL20R8A Series (Com'l)

28E D 🔳 0257526 0029476 7 🔳 AMD2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ. Absolute Maximum Ratings are for system design reference; parameters given are not tested. Operating in Free Air Operating Case (Tc) Temperature Supply Voltage (Vcc) with Respect to Ground

OPERATING RANGES

Military (M) Devices (Note 1) Ambient Temperature (T_A)

–55°C Min. +125°C Max.

T-46-19-13

+4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at To +25°C, +125°C, and -55°C per MIL-STO-883.

Note 2)	T				
Parameter Symbol	Parameter Description	Test Conditions	Min.	Max.	Uni
VoH	Output HIGH Voltage	$I_{OH} = -2 \text{ mA}$ $V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = \text{Min.}$	24		V
Vol	Output LOW Voltage	$\begin{aligned} I_{OL} &= 12 \text{ mA}^{-1} V_{IN} &= V_{IH} \text{ of } V_{II} \\ V_{CC} &= M_{II} \text{ of } V_{II} \end{aligned}$	S.	0.5	V
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		V
ViL	Input LOW Voltage	Guaranteed Input Logical LOW Voltage for all Inputs (Note 3)		0.8	V
Vi 🤺	Input Clamp Voltage	$l_{\rm IN} = -18 {\rm m}$ Å, Vcc = Min.		-1.5	٧
hn X	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 4)		25	μA
11	Input LOW Current	ViN = 0.4 V, Vcc = Max. (Note 4)		.–250	·μA
lı .	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		. 1	mA
Іодн	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4 \text{ V}, V_{CC} = \text{Max.}$ $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		100	μA
lozl	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4 \text{ V}, V_{CC} = \text{Max.}$ $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-100	μA
lsc	Output Short-Circuit Current	Vour = 0.5 V, Vcc = Max. (Note 5)	-30	-130	mA
lcc	Supply Current	$V_{IN} = 0 V$, Outputs Open (lour = 0 mA) $V_{CC} = Max$.		210	mA

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified

Notes:

2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.

V_{IL} and V_{IH} are input conditions of output tests and are not themselves directly tested. V_{IL} and V_{IH} are absolute voltages with
respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values
without suitable equipment.

4. I/O pin leakage is the worst case of $I_{\rm IL}$ and IozL (or IIH and IozH).

Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

2-140

PAL20R8A Series (Mil)

🚾 0257526 0029477 9 페 AMD2 ADV MICRO PLA/PLE/ARRAYS 28E D T-46-19-13

Parameter Symbol	Parameter Des	scription		ł	Min.	Max.	Unit
tpp	Input or Feedba Combinatorial C					30	ns
ts	Setup Time from	m Input or Feedback to	Clock		30		ns
ţн	Hold Time			l I	0		ns
tco	Clock to Output	or Feedback		I		20	ns
tw.	Clock Width	LOW		20R8, 20R6	20		ns
twн		HIGH		20R4	20		ns
4	Maximum	External Feedback	$1/(t_{\rm S} + t_{\rm CO})$		20		MHz
Т МАХ	Frequency (Note 2)	No Feedback	1/(twn + twL)	~	125	A	MHz
t _{PZX}	OE to Output E	nable (Note 3)			KA V	-25	ns
tpxz	OE to Output D	isable (Note 3)			KAV	25	пs
tea	Input to Output Term Control (N	Enable Using Product Note 3)	R.	20L8, 20R6	Cane, and	30	ns
ter	Input to Output Term Control (N	Disable Using Product Note 3)	1 APN C	20R4		30	ns



Notes:

- 1. See Switching Test Circuit for test conditions. For APL products Group A, Subgroups tested per MIL-STD-883, Method 5005, unless otherwise noted. lÖ
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
 These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified.
- 3. These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected. X 襞 5 🌮

PAL20R8A Series (Mil)

ADV MICRO PLA/PLE/ARRAYS 28E D B 0257526 0029478 0 B AMD2

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Amblent Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	-1.5 V to Vcc + 0.5 V
DC Output or I/O Pin Voltage	–0.5 V to V _{cc} + 0.5 V

Stresses above those listed under Absolute Maximum Ratings may cause permanent device failure. Functionality at or above these limits is not implied. Exposure to Absolute Maximum Ratings for extended periods may affect device reliability. Programming conditions may differ.

OPERATING RANGES	T-46-19-13
Commercial (C) Devices	
Ambient Temperature (TA)	
Operating in Free Air	0°C to +75°C
Supply Voltage (Vcc)	
with Respect to Ground	+4.75 V to +5.25 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

DC CHARACTERISTICS over COMMERCIAL operating ranges unless otherwise specified Parameter Symbol **Parameter Description Test Conditions** Min. Max. Unit **Output HIGH Voltage** Vон -3.2 mA VIN = VIH or VI ٧ Юн 2.4 Vcc = Min. Output LOW Voltage VOL 0.5 v ٧н Input HIGH Voltage Guaranteed Input Logical HIGH. 2.0 ٧ Voltage for all inputs (Note 1) Input LOW Voltage ViL Guaranteed Input Logical LOW 0.8 ۷ 徽 100 Voltage for all Inputs (Note 1) Vi Input Clamp Voltage $I_{IN} = -18 \text{ mA}, \text{ Vcc} = Min^{-1}$ -1.5 ٧ łн Input HIGH Current VIN = 2.7 V, Vcc = Max. (Note 2) 25 μA h 80 Input LOW Current VIN = 0.4 V, Vcc = Max. (Note 2) -250 μA h Maximum Input Current VIN = 5.5 V, Vcc = Max. 100 μA Off-State Output Leakage lozн Vout = 2.7 V, Vcc = Max. 100 μΑ £ 74 Current HIGH VIN = VIH or VIL (Note 2) lozl Off-State Output Leakage Vour = 0.4 V, Vcc = Max. -100 μA Current LOW V_{IN} = V_{IH} or V_{IL} (Note 2) Output Short-Circuit Current lsc Vour = 0.5 V, Vcc = Max. (Note 3) -30 -130 mA lcc Supply Current VIN = 0 V, Outputs Open (lout = 0 mA) 105 mΑ Vcc = Max.

Notes:

1. These are absolute values with respect to device ground and all overshoots due to system and/or tester noise are included.

2. I/O pin leakage is the worst case of IIL and IOZL (or IIH and IOZH).

Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second.
 VOUT = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

PAL20R8A-2 Series (Com'l)

ADV MICRO PLA/PLE/ARRAYS 28E D M 0257526 0029479 2 M AMD2

SWITCHING CHARACTERISTICS over COMMERCIAL operating ranges (Note 1)

Parameter Symbol	Parameter Des	Parameter Description T-46-19-13				Max.	Unit
tpp	Input or Feedba Combinatorial C			35	ns		
ts	Setup Time fron	n Input or Feedback to	Input or Feedback to Clock				ns
tн	Hold Time						ns
tco	Clock to Output	or Feedback	r Feedback 20			25	ns
• tw.	Clock Width	LOW		20R4	25		ns
twн		HIGH			25		ns
fmax	Maximum Frequency	External Feedback	1/(ts + tco)		16		MHz
IMAX	(Note 2)	No Feedback	1/(t _{WH} + t _{WL})		1205		MHz
tpzx	OE to Output Er	nable			64 8	<u>_</u> 25	ns
tpxz	OE to Output Di		NA V	25	ns.		
tea	Input to Output Enable Using Product Term Control			20L8, 20R6	A Sector State	35	ns
ter	Input to Output Disable Using Product Term Control					35	ns



Notes:

1. See Switching Test Circuit for test conditions

2. These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.

PAL20R8A-2 Series (Com'l)

ABSOLUTE MAXIMUM RATINGS

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied	-55°C to +125°C
Supply Voltage with Respect to Ground	–0.5 V to +7.0 V
DC Input Voltage	-1.5 V to +5.5 V
DC Output or I/O Pin Voltage	5.5 V

T-46-19-13 **OPERATING RANGES**

Military (M) Devices (Note 1) Ambient Temperature (T_A) Operating in Free Air Supply Voltage (Vcc)

-55°C to +125°C with Respect to Ground +4.50 V to +5.50 V

Operating ranges define those limits between which the functionality of the device is guaranteed.

Note:

1. Military products are tested at $T_C = +25^{\circ}C$, +125°C, and -55°C per MIL-STD-883.

Stresses above those listed under Absolute Maximum Rat-
ings may cause permanent device failure. Functionality at or
above these limits is not implied. Exposure to Absolute Maxi-
mum Ratings for extended periods may affect device reliabil-
ity. Programming conditions may differ. Absolute Maximum
Ratings are for system design reference; parameters given
are not tested.

Note 2)	·		A BURNER AND A BURNER A		
Parameter Symbol	Parameter Description	Test Conditions	_Min.	Max.	Unit
V _{OH}	Output HIGH Voltage	$loi = -2 \text{ mA} V_{IN} = V_{IH} \text{ or } V_{IL}$ $V_{CC} = Min.$	2,4		۷
VOL	Output LOW Voltage	$I_{OL} = 12 \text{ mA}$ $V_{IN} = V_{IH} \text{ of } V_{IL}$ $V_{CC} = Min$	S.	0.5	۷
ViH	Input HIGH Voltage	Guaranteed Input Logical HIGH Voltage for all Inputs (Note 3)	2.0		٧
ViL	Input LOW Voltage	Guarantèed Inpùt Logical LOW Voltage for all Inputs (Note 3)		0.8	V
VI	Input Clamp Voltage	$I_{\rm IN} = -18$ mÅ, $V_{\rm CC} = Min$.		-1.5	V
lin I	Input HIGH Current	V _{IN} = 2.4 V, V _{CC} = Max. (Note 4)		25	μA
HL	Input LOW Current	V _{IN} = 0.4 V, V _{CC} = Max. (Note 4)		-250	μA
4	Maximum Input Current	V _{IN} = 5.5 V, V _{CC} = Max.		1	mA
Югн	Off-State Output Leakage Current HIGH	$V_{OUT} = 2.4 \text{ V}, V_{CC} = \text{Max.}$ $V_{IN} = V_{IH} \text{ or } V_{IL} (\text{Note } 4)$		100	μA
lozi	Off-State Output Leakage Current LOW	$V_{OUT} = 0.4 \text{ V}, V_{CC} = \text{Max.}$ $V_{IN} = V_{IH} \text{ or } V_{IL} \text{ (Note 4)}$		-100	μA
lsc	Output Short-Circuit Current	V _{OUT} = 0.5 V, V _{CC} = Max. (Note 5)	-30	-130	mA
	Supply Current	$V_{IN} = 0 V$, Outputs Open ($t_{OUT} = 0 mA$) $V_{CC} = Max$.		105	mA

DC CHARACTERISTICS over MILITARY operating ranges unless otherwise specified

Notes:

- 2. For APL Products, Group A, Subgroups 1, 2, and 3 are tested per MIL-STD-883, Method 5005, unless otherwise noted.
- 3. VIL and VIH are input conditions of output tests and are not themselves directly tested. VIL and VIH are absolute voltages with respect to device ground and include all overshoots due to system and/or tester noise. Do not attempt to test these values without suitable equipment.
- 4. I/O pin leakage is the worst case of I_{IL} and I_{OZL} (or I_{IH} and I_{OZH}).
- 5. Not more than one output should be tested at a time. Duration of the short-circuit should not exceed one second. Vour = 0.5 V has been chosen to avoid test problems caused by tester ground degradation.

2-144

PAL20R8A-2 Series (Mil)

ADV MICRO PLA/PLE/ARRAYS III 0257526 0029481 0 III AMD2 28E D

SWITCHIN	IG CHARACT	ERISTICS over Mil	LITARY ope	rating ranges	(Note 1) 1	-46-19
Parameter Symbol	Parameter Description				Min.	Max.	Unit
t _{PD}	Input or Feedba Combinatorial (20L8, 20R6 20R4		50	ns	
ts	Setup Time from	m Input or Feedback to		50		ns	
ţн	Hold Time			0		ns	
tco	Clock to Output	t or Feedback			25	ns	
tw.	Clock Width	LOW		20R8, 20R6	25		ns
twn		HIGH		20R4	25		ns
fmax	Maximum Frequency	External Feedback	1/(ts + tco)		13.3		MHz
	(Note 2)	No Feedback	$1/(t_{WH} + t_{WL})$		20		MHz
tezx	OE to Output Enable (Note 3)				LA 1/8	_25	ns
texz	OE to Output Disable (Note 3)			CP2	KAN	25	ns
tea	Input to Output Enable Using Product Term Control (Note 3)			20L8, 20R6	Value and	45	ns
ter	Input to Output Disable Using Product Term Control (Note 3)			20R4		45	ns

Notes:

- 1. See Switching Test Circuit for test conditions. Fot APL products Group A, Subgroups tested per MIL-STD-883, Method 5005 unless otherwise noted.
- These parameters are not 100% tested, but are calculated at initial characterization and at any time the design is modified where frequency may be affected.
 These parameters are not 100% tested, but are evaluated at initial characterization and at any time the design is modified where these parameters may be affected.
- 50

PAL20R8A-2 Series (Mil)



- 1. V_T = 1.5 V
- 2. Input pulse amplitude 0 V to 3.0 V
- 3. Input rise and fall times 2-5 ns typical.

(2-4 ns for -7 (-12 Mil) and -10 (-15 Mil) Series)

2-146

KEY TO SWITCHING WAVEFORMS



SWITCHING TEST CIRCUIT



	S ₁		Commercial		Military		Measured	
Specification		CL	R ₁	R ₂	R ₁	R ₂	Output Value	
tpd, tco, tcf	Closed						1.5 V	
tpzx, tea	$Z \rightarrow H$: Open $Z \rightarrow L$: Closed	50 pF	200 Ω	390 Ω	390 Ω	750 Ω	1.5 V	
tpxz, ter	$H \rightarrow Z$: Open L $\rightarrow Z$: Closed	5 pF					H → Z: V _{OH} – 0.5 V L → Z: V _{OL} + 0.5 V	

PAL20R8 Family

2-147

.

INPUT/OUTPUT EQUIVALENT SCHEMATICS

Typical input

Typical Output

T-46-19-13





2-148

T-46-19-13

OUTPUT REGISTER PRELOAD Applies to -7 (-12 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

- 1. Raise Vcc to VccH.
- 2. Set \overline{OE} to V_{IHP} to disable output registers.
- 3. Raise pin 2 to V_{HH} to enter preload mode.
- Apply either V_{HH} or V_{ILP} to all registered outputs. Use V_{HH} to preload a LOW in the flip-flop; use V_{ILP} to

preload a HIGH in the flip-flop. Leave combinatorial outputs floating.

- 5. Lower pin 2 to VILP.
- 6. Remove VILP/VHH from all registered output pins.
- 7. Lower \overline{OE} to V_{HP} to enable the output registers.
- Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
Vнн	Super-level input voltage	10	11	12	v
VILP	Low-level input voltage	0	0	0.5	V
VIHP	High-level input voltage	2.4	5.0	5,5	v
Vссн	Power supply during preload	5.4	5.7	6.0	v
to	Delay time	100	200	1000	ns





Output Register Preload Waveform

PAL20R8 Family

OUTPUT REGISTER PRELOAD Applies to -10 (-15 Mil) Series Only

The preload function allows the register to be loaded from the output pins. This feature aids functional testing of sequential designs by allowing direct setting of output states. The procedure for preloading follows.

- 1. Raise Vcc to 4.5 V.
- 2. Set \overline{OE} to V_{IHP} to disable output registers.
- 3. Apply either VIHP or VILP to all registered outputs. Use VIHP to preload a HIGH in the flip-flop; use VILP to
- preload a LOW in the flip-flop. Leave combinatorial outputs floating.

T-46-19-13

- 4. Pulse pin 10 to V_{HH} , then back to 0 V.
- 5. Remove VILP/VIHP from all registered output pins.
- 6. Lower \overline{OE} to V_{ILP} to enable the output registers.
- Verify V_{OL}/V_{OH} at all registered output pins. Note that because of the output inverter, a register that has been preloaded HIGH will provide a LOW at the output.

Parameter Symbol	Parameter Description	Min.	Rec.	Max.	Unit
Vнн	Super-level input voltage	19	20	21	v
VILP	Low-level input voltage	. 0	0	0.5	V
VIHP	High-level input voltage	2.4	5.0	5.5	V
to	Delay time	100	200	1000	ns



10294-004A

Output Register Preload Waveform

2-150

POWER-UP RESET

The power-up reset feature ensures that all flip-flops will be reset to LOW after the device has been powered up.

The output state will be HIGH due to the inverting output buffer. This feature is valuable in simplifying state ma-

chine initialization. A timing diagram and parameter ta-

ble are shown below. Due to the synchronous operation of the power-up reset and the wide range of ways V_{CC}

T-46-19-13

can rise to its steady state, two conditions are required to ensure a valid power-up reset. These conditions are:

- 1. The V_{CC} rise must be monotonic.
- 2. Following reset, the clock input must not be driven from LOW to HIGH until all applicable input and feedback setup times are met.

Parameter Symbol	Parameter Description	Max.	Unit		
ter	Power-up Reset Time	1000	ns		
ts	Input or Feedback Setup Time	See Switchi	See Switching		
twL	Clock Width LOW	Characterist	Characteristics		



Power-Up Reset Waveform

PAL20R8 Family