TP65H070G4LSGB

650V SuperGaN® GaN FET in PQFN (source tab)

Description

The TP65H070G4LSGB 650V, 72mΩ Gallium Nitride (GaN) FET is a normally-off device. It combines state-of-the-art high voltage GaN HEMT and low voltage silicon MOSFET technologies—offering superior reliability and performance.

The Gen IV SuperGaN® platform uses advanced epi and patented design technologies to simplify manufacturability while improving efficiency over silicon via lower gate charge, output capacitance, crossover loss, and reverse recovery charge

Related Literature

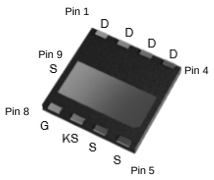
- Recommended External Circuitry for GaN FETs
- Printed Circuit Board Layout and Probing
- Recommendations for Vapor Phase Reflow
- Paralleling GaN FETs
- PQFN Tape and Reel Information
- Low cost driver solution

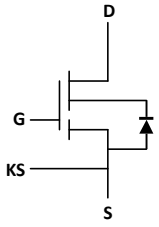
Ordering Information

Part Number	Package	Package Configuration
TP65H070G4LSGB-TR	8x8 PQFN	Source

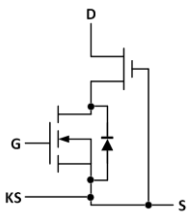
* "-TR" suffix refers to tape and reel. Refer to AN0012 for details.

TP65H070G4LSGB
PQFN
(Bottom view)





Cascode Schematic Symbol



Cascode Device Structure

Features

- Gen IV technology
- JEDEC-qualified GaN technology
- Dynamic $R_{DS(on)eff}$ production tested
- Robust design, defined by
  - — Wide gate safety margin
  - — Transient over-voltage capability
- Very low Q_{RR}
- Reduced crossover loss
- RoHS compliant and Halogen-free packaging

Benefits

- Achieves increased efficiency in both hard- and soft-switched circuits
  - — Increased power density
  - — Reduced system size and weight
  - — Overall lower system cost
- Easy to drive with commonly-used gate drivers
- GSD pin layout improves high speed design

Applications

- Datacom
- Broad industrial
- PV inverter
- Servo motor
- Consumer
- Computing

Key Specifications	
V_{DSS} (V)	650
$V_{DSS(TR)}$ (V)	800
$R_{DS(on)eff}$ (mΩ) max*	85
Q_{oss} (nC) typ	78
Q_G (nC) typ	8.4

* Dynamic on-resistance; see Figures 18 and 19

Absolute Maximum Ratings (T_c=25°C unless otherwise stated.)

Symbol	Parameter		Limit Value	Unit
V_{DSS}	Drain to source voltage (T_J = -55°C to 150°C)		650	V
$V_{DSS(TR)}$	Transient drain to source voltage [a]		800	
V_{GSS}	Gate to source voltage		±20	
P_D	Maximum power dissipation @T_C=25°C		96	W
I_D	Continuous drain current @T_C=25°C [b]		29	A
	Continuous drain current @T_C=100°C [b]		18.4	A
I_{DM}	Pulsed drain current (pulse width: 10µs)		120	A
T_C	Operating temperature	Case	-55 to +150	°C
T_J		Junction	-55 to +150	°C
T_S	Storage temperature		-55 to +150	°C
T_{SOLD}	Reflow soldering temperature [c]		260	°C

Notes:

a. In off-state, spike duration <30 µs, non-repetitive

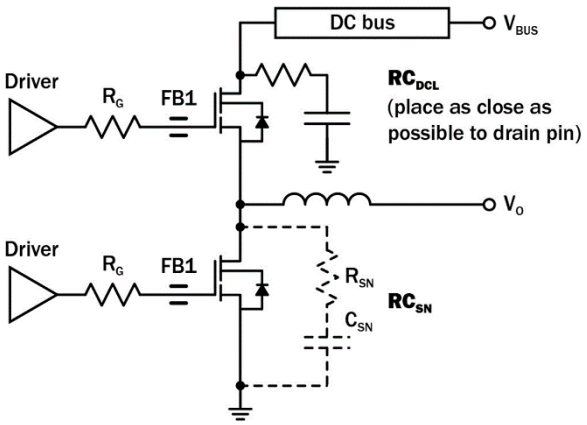
b. For increased stability at high current operation, see Circuit Implementation on page 3

c. Reflow MSL3

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\Theta JC}$	Junction-to-case	1	°C/W
$R_{\Theta JA}$	Junction-to-ambient	62	°C/W

Circuit Implementation



Simplified Half-bridge Schematic (See also on Figure 13)

For additional gate driver options/configurations, please see Application Note Recommended External Circuitry for GaN FETs

Layout Recommendations

Gate Loop:

- Gate Driver: SiLab Si823x/Si827x
- Keep gate loop compact
- Minimize coupling with power loop

Power loop: (For reference see page 13)

- Minimize power loop path inductance
- Minimize switching node coupling with high and low power plane
- Add DC bus snubber to reduce to voltage ringing
- Add Switching node snubber for high current operation

Recommended gate drive: (0V, 12V) with R_G= 50Ω

Gate Ferrite Bead (FB1)	Required DC Link RC Snubber (RC_{DCL}) [d]	Recommended Switching Node RC Snubber (RC_{SN}) [e]
200 – 300Ω at 100MHz	10nF + 5Ω	Not necessary [e]

Notes:

d. RC_{DCL} should be placed as close as possible to the drain pin

e. RC_{SN} (68pF + 15Ω) is needed only if R_G is smaller than recommendations

Electrical Parameter (T_J=25 °C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Forward Device Characteristics						
$V_{(BL)DSS}$	Drain-source voltage	650	—	—	V	V_{GS}=0V
$V_{GS(th)}$	Gate threshold voltage	3.2	4	4.6	V	V_{DS}=V_{GS}, I_D=0.7mA
$R_{DS(on)eff}$	Drain-source on-resistance (f)	—	72	85	mΩ	V_{GS}=10V, I_D=16A,T_J=25 °C
		—	148	—		V_{GS}=10V, I_D=16A, T_J=150 °C
I_{DSS}	Drain-to-source leakage current	—	3	30	μA	V_{DS}=650V, V_{GS}=0V, T_J=25 °C
		—	12	—		V_{DS}=650V, V_{GS}=0V, T_J=150 °C
I_{GSS}	Gate-to-source forward leakage current	—	—	100	nA	V_{GS}=20V
	Gate-to-source reverse leakage current	—	—	-100		V_{GS}=-20V
C_{ISS}	Input capacitance	—	600	—	pF	V_{GS}=0V, V_{DS}=400V, *f*=1MHz
C_{OSS}	Output capacitance	—	74	—		
C_{RSS}	Reverse transfer capacitance	—	2	—		
$C_{O(er)}$	Output capacitance, energy related (g)	—	109	—	pF	V_{GS}=0V, V_{DS}=0V to 400V
$C_{O(tr)}$	Output capacitance, time related (h)	—	200	—		
Q_G	Total gate charge	—	8.4	—	nC	V_{DS}=400V, V_{GS}=0V to 10V, I_D=16A
Q_{GS}	Gate-source charge	—	3.3	—		
Q_{GD}	Gate-drain charge	—	2.3	—		
Q_{OSS}	Output charge	—	78	—	nC	V_{GS}=0V, V_{DS}=0V to 400V
$t_{D(on)}$	Turn-on delay	—	27	—	ns	V_{DS}=400V, V_{GS}=0V to 12V, I_D=16A, R_G=50Ω
t_R	Rise time	—	9	—		
$t_{D(off)}$	Turn-off delay	—	71	—		
t_F	Fall time	—	6.5	—		

Notes:

f. Dynamic on-resistance; see Figures 5 and 6 for test circuit and conditions

g. Equivalent capacitance to give same stored energy as V_{DS} rises from 0V to 400V

h. Equivalent capacitance to give same charging time as V_{DS} rises from 0V to 400V

Electrical Parameters (T_J=25°C unless otherwise stated)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions
Reverse Device Characteristics						
I_S	Reverse current	—	—	16	A	V_{GS}=0V, T_C=100°C, ≤25% duty cycle
V_{SD}	Reverse voltage [i]	—	2.2	2.6	V	V_{GS}=0V, I_S=16A
		—	1.6	1.9		V_{GS}=0V, I_S=8A
t_{RR}	Reverse recovery time	—	34	—	ns	I_S=16A, V_{DD}=400V, di/dt=1000A/ms
Q_{RR}	Reverse recovery charge [j]	—	0	—	nC	
$(di/dt)_{RDMC}$	Reverse diode di/dt [k]	—	—	1900	A/µs	

Notes:

i. Includes dynamic $R_{DS(on)}$ effect

j. Excludes Qoss

k. Reverse conduction di/dt will not exceed this max value with recommended R_G.

Typical Characteristics (T_c=25 °C unless otherwise stated)

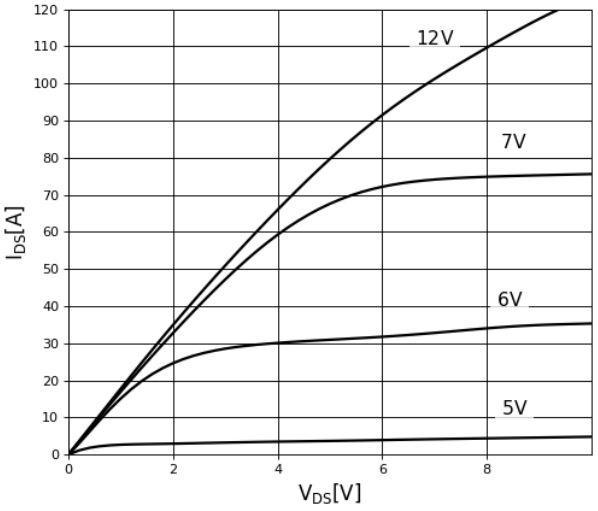


Figure 1. Typical Output Characteristics T_J=25 °C
Parameter: V_{GS}

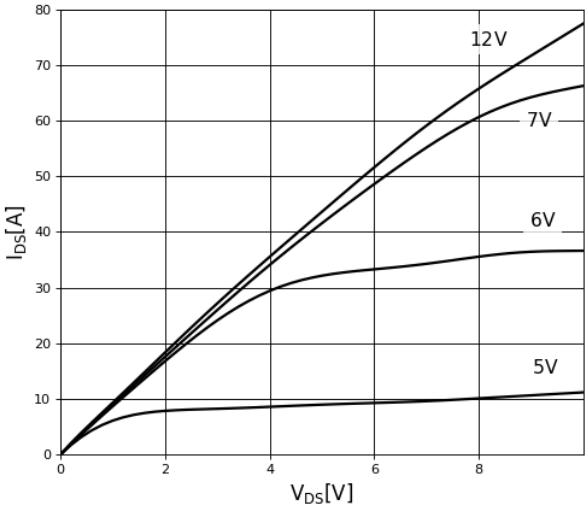


Figure 2. Typical Output Characteristics T_J=150 °C
Parameter: V_{GS}

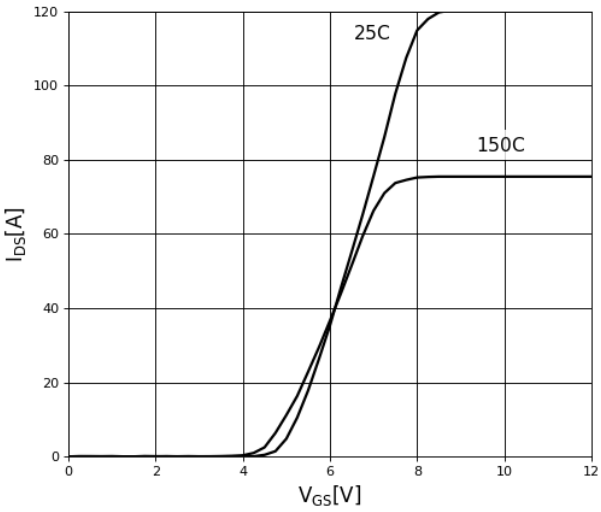


Figure 3. Typical Transfer Characteristics
V_{DS}=10V, parameter: T_J

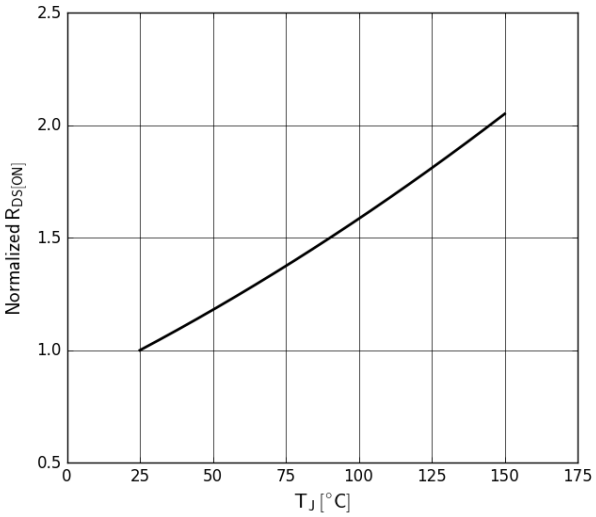


Figure 4. Normalized On-resistance
I_D=16A, V_{GS}=10V

Typical Characteristics (T_c=25 °C unless otherwise stated)

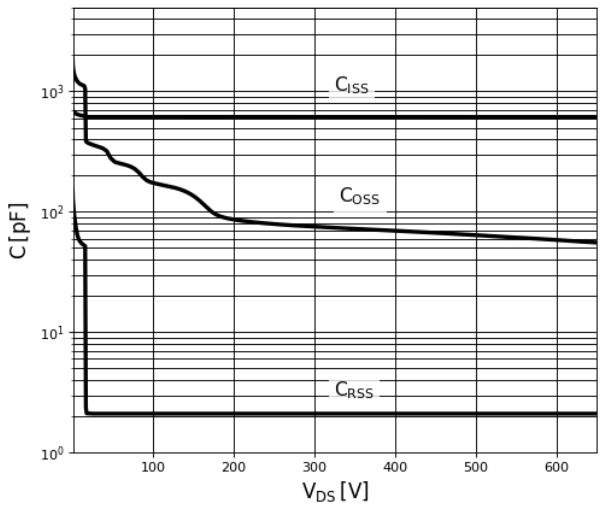


Figure 5. Typical Capacitance

V_{GS}=0V, f=1MHz

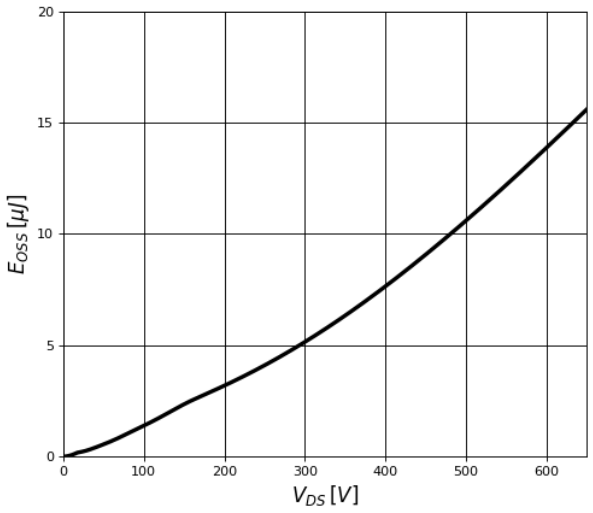


Figure 6. Typical C_{OSS} Stored Energy

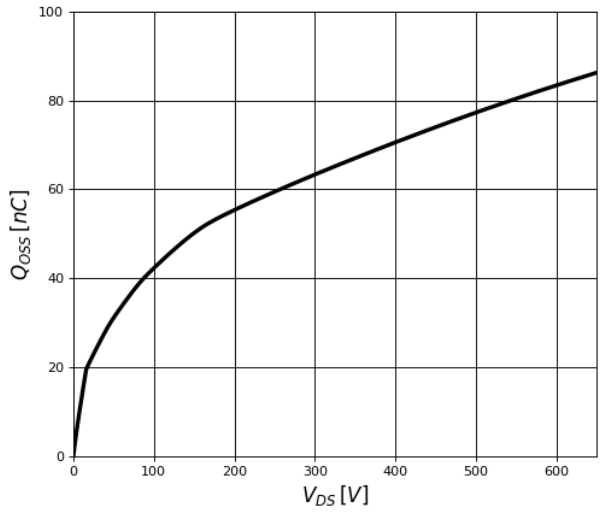


Figure 7. Typical Q_{OSS}

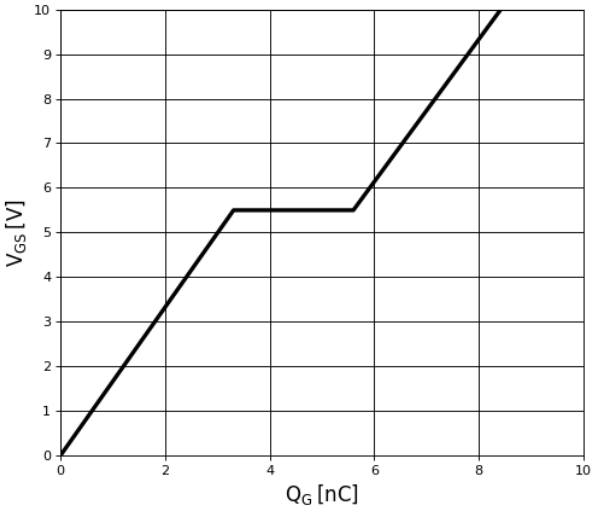


Figure 8. Typical Gate Charge

I_{DS}=16A, V_{DS}=400V

Typical Characteristics (T_c=25 °C unless otherwise stated)

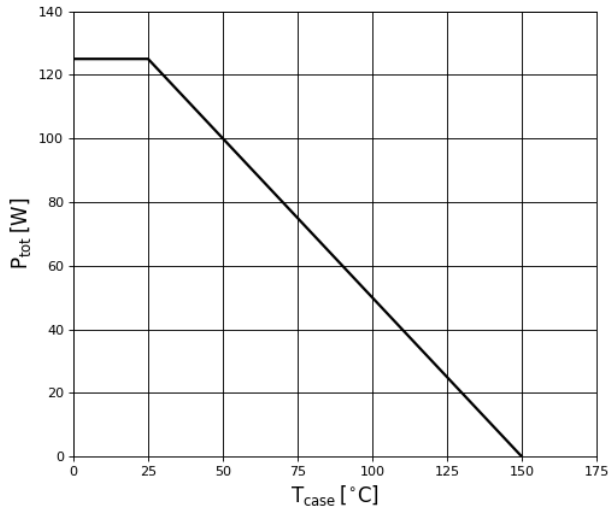


Figure 9. Power Dissipation

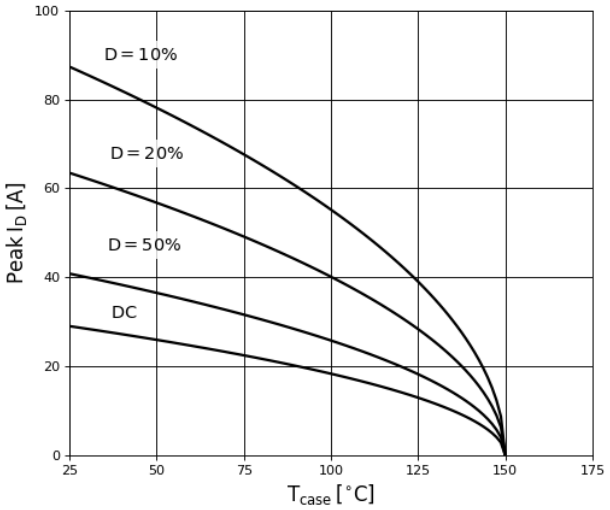


Figure 10. Current Derating

Pulse width ≤ 10µs, V_{GS} ≥ 10V

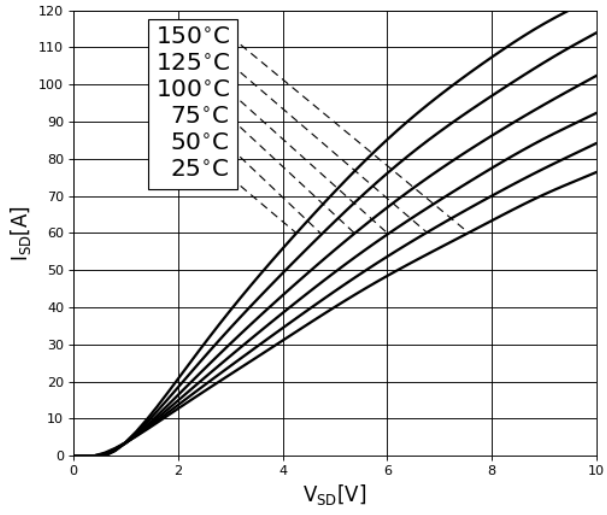


Figure 11. Forward Characteristics of Rev. Diode

I_S=f(V_{SD}), parameter: T_J

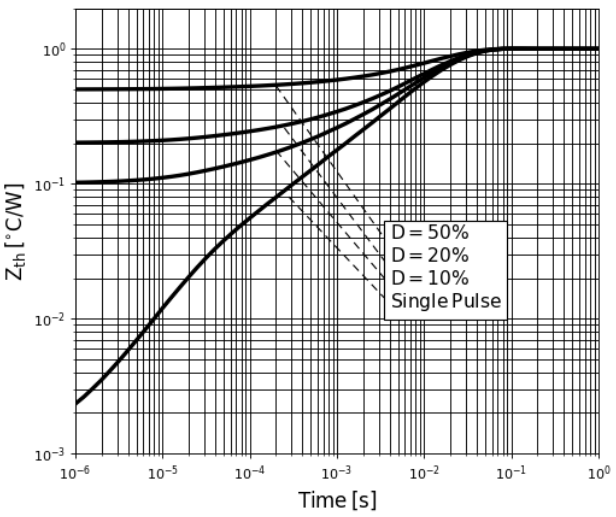


Figure 12. Transient Thermal Resistance

Typical Characteristics (T_c=25 °C unless otherwise stated)

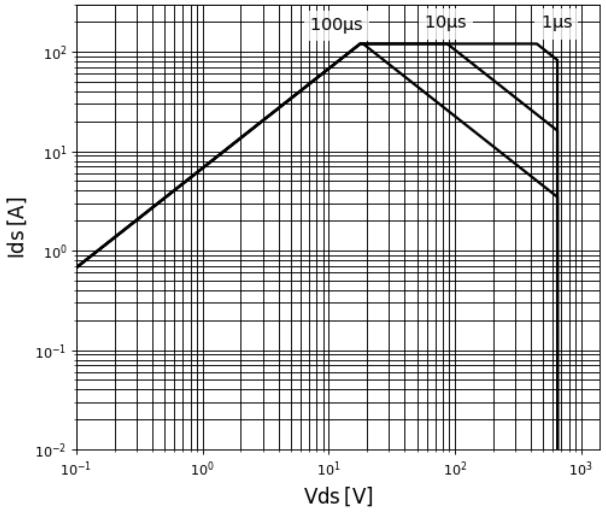


Figure 13. Safe Operating Area T_C=25 °C

Test Circuits and Waveforms

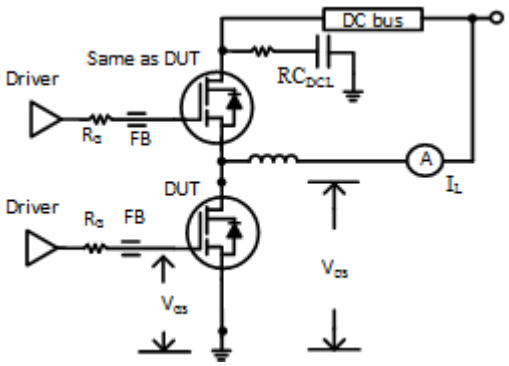


Figure 14. Switching Time Test Circuit

(see circuit implementation on page 3 for methods to ensure clean switching)

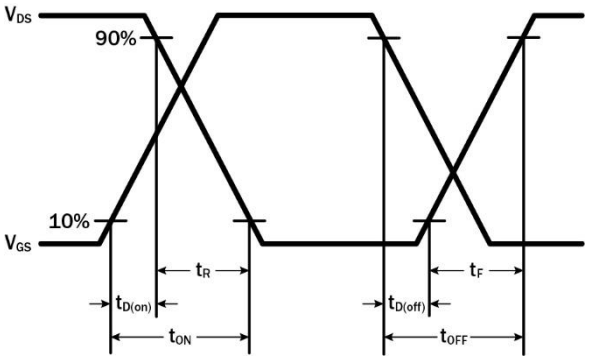


Figure 15. Switching Time Waveform

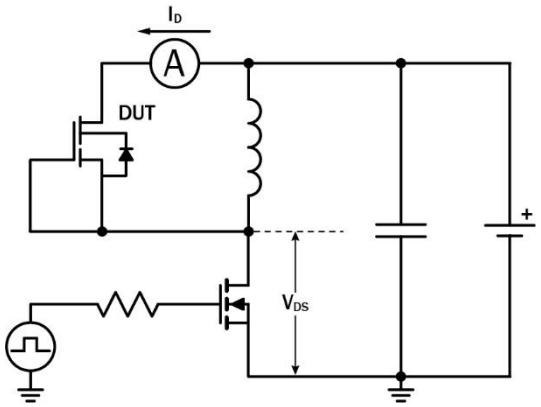


Figure 16. Diode Characteristics Test Circuit

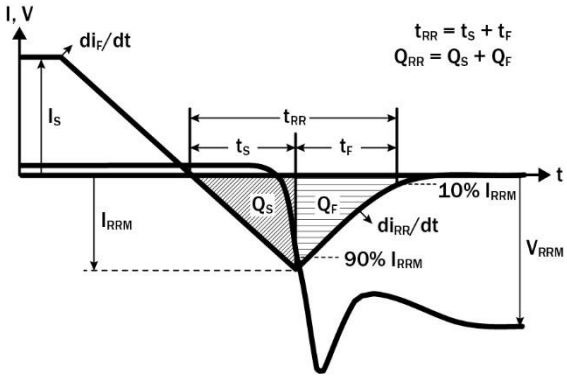


Figure 17. Diode Recovery Waveform

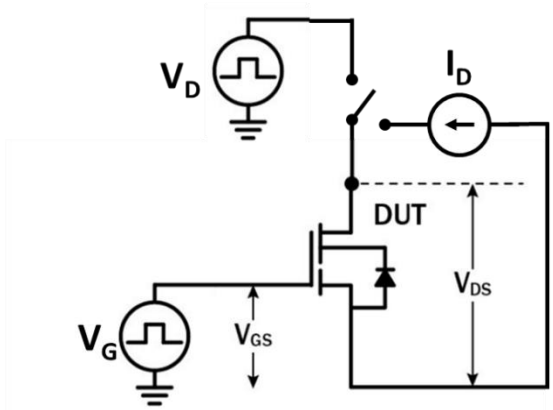


Figure 18. Dynamic $R_{DS(on)eff}$ Test Circuit

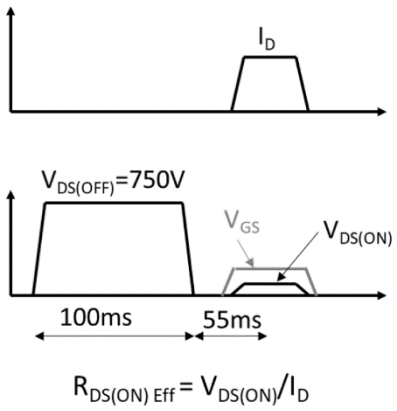


Figure 19. Dynamic $R_{DS(on)eff}$ Waveform

Design Considerations

The fast switching of GaN devices reduces current-voltage crossover losses and enables high frequency operation while simultaneously achieving high efficiency. However, taking full advantage of the fast switching characteristics of GaN switches requires adherence to specific PCB layout guidelines and probing techniques.

Before evaluating Renesas GaN devices, see application note Printed Circuit Board Layout and Probing for GaN Power Switches. The table below provides some practical rules that should be followed during the evaluation.

When Evaluating Renesas GaN Devices:

DO	DO NOT
Minimize circuit inductance by keeping traces short, both in the drive and power loop	Twist the pins of TO-220 or TO-247 to accommodate GDS board layout
Minimize lead length of TO-220 and TO-247 package when mounting to the PCB	Use long traces in drive circuit, long lead length of the devices
Use shortest sense loop for probing; attach the probe and its ground connection directly to the test points	Use differential mode probe or probe ground clip with long wire
See Printed Circuit Board Layout and Probing	

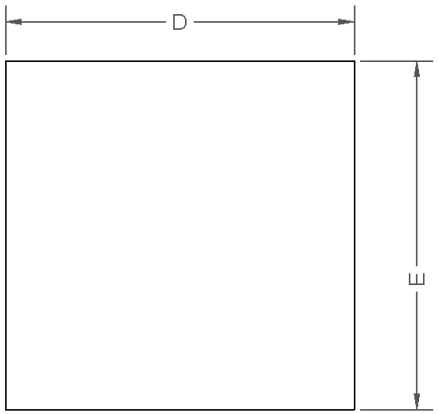
GaN Design Resources

The complete technical library of GaN design tools can be found at Renesasusa.com/design:

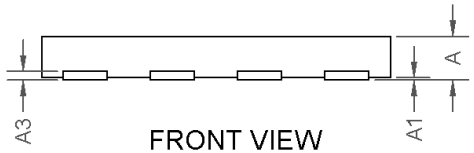
- Reference designs
- Evaluation kits
- Application notes
- Design guides
- Simulation models
- Technical papers and presentations

Mechanical

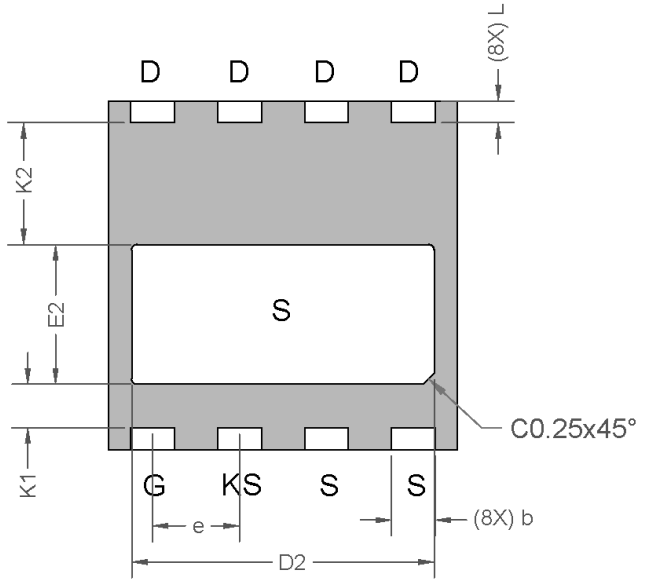
8x8 PQFN Package



TOP VIEW



FRONT VIEW



BOTTOM VIEW

G: Gate
S: Source
D: Drain
K: Kelvin
Lead finish: Sn plating

DIM	mm			inch		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.90	1.00	1.10	0.035	0.039	0.043
A1	0.00	-	0.05	0.000	-	0.002
A3		0.20 REF.			0.007 BSC	
b	0.5	1.00	1.5	0.020	0.039	0.059
D	7.90	8.00	8.10	0.311	0.315	0.319
D2	6.79	6.94	7.09	0.267	0.273	0.279
E	7.90	8.00	8.10	0.311	0.315	0.319
e		2.00 BSC			0.007 BSC	
E2	3.05	3.20	3.35	0.120	0.126	0.132
K1	1.00	-	-	0.039	-	-
K2	2.8	-	-	0.110	-	-
L	0.40	0.50	0.60	0.016	0.020	0.024

PQFN 8mm x 8mm POD (TP65HxxxG4LSGB)

transphorm