

# Future Technology Devices International Ltd

## FT4232H Quad High Speed USB to Multipurpose UART/MPSSSE IC



The FT4232H is FTDI's 5<sup>th</sup> generation of USB devices. The FT4232H is a USB 2.0 High Speed (480Mb/s) to UART/MPSSSE ICs. The device features 4 UARTs. Two of these have an option to independently configure an MPSSSE engine. This allows the FT4232H to operate as two UART/Bit-Bang ports plus two MPSSSE engines used to emulate JTAG, SPI, I<sup>2</sup>C, Bit-bang or other synchronous serial modes. The FT4232H has the following advanced features:

- Single chip USB to quad serial ports with a variety of configurations.
- Entire USB protocol handled on the chip. No USB specific firmware programming required.
- USB 2.0 High Speed (480Mbits/Second) and Full Speed (12Mbits/Second) compatible.
- Two Multi-Protocol Synchronous Serial Engine (MPSSSE) on channel A and channel B, to simplify synchronous serial protocol (USB to JTAG, I<sup>2</sup>C, SPI or bit-bang) design.
- Independent Baud rate generators.
- RS232/RS422/RS485 UART Transfer Data Rate up to 12Mbaud. (RS232 Data Rate limited by external level shifter).
- FTDI's royalty-free Virtual Com Port (VCP) and Direct (D2XX) drivers eliminate the requirement for USB driver development in most cases.
- Optional traffic TX/RX indicators can be added with LEDs and an external 74HC595 shift register.
- Adjustable receive buffer timeout.
- Support for USB suspend and resume conditions via PWREN#, SUSPEND# and RI# pins.
- Highly integrated design includes +1.8V LDO regulator for V<sub>CORE</sub>, integrated POR function and on chip clock multiplier PLL (12MHz – 480MHz).
- FTDI FT232B style, asynchronous serial UART interface option with full hardware handshaking and modem interface signals.
- Fully assisted hardware or X-On / X-Off software handshaking.
- UART Interface supports 7/8 bit data, 1/2 stop bits, and Odd/Even/Mark/Space/No Parity.
- Auto-transmit enable control for RS485 serial applications using TXDEN pin.
- Operational configuration mode and USB Description strings configurable in external EEPROM over the USB interface.
- Low operating and USB suspend current.
- Configurable I/O drive strength (4, 8, 12 or 16mA) and slew rate.
- Supports bus powered, self-powered and high-power bus powered USB configurations.
- UHCI/OHCI/EHCI host controller compatible.
- USB Bulk data transfer mode (512 byte packets in High Speed mode).
- Dedicated Windows DLLs available for USB to JTAG, USB to SPI, and USB to I<sup>2</sup>C applications.
- +1.8V (chip core) and +3.3V I/O interfacing (+5V Tolerant).
- Extended -40°C to 85°C industrial operating temperature range.
- Compact 64-LD Lead Free LQFP or QFN package
- Available in compact Pb-free 56 Pin VQFN packages (RoHS compliant)
- +3.3V single supply operating voltage range.
- ESD protection for FT4232H IO's:  
Human Body Model (HBM) ±2kV,  
Machine Mode (MM) ±200V,  
Charge Device Model (CDM) ±500V,

Latch-up free.

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## 1 Typical Applications

- Single chip USB to four channels UART (RS232, RS422 or RS485) or Bit-Bang interfaces.
- Single chip USB to 2 JTAG channels plus 2 UARTS.
- Single chip USB to 1 JTAG channel plus 3 UARTS.
- Single chip USB to 1 SPI channel plus 3 UARTS.
- Single chip USB to 2 SPI channels plus 2 UARTS.
- Single chip USB to 2 Bit-Bang channels plus 2 UARTS.
- Single chip USB to 1 SPI channel, plus 1 JTAG channel plus 2 UARTS.
- Single chip USB to 2 I<sup>2</sup>C channels plus 2 UARTS.
- Numerous combinations of 4 channels.
- Upgrading Legacy Peripheral Designs to USB
- Field Upgradable USB Products
- Cellular and cordless phone USB data transfer cables and interfaces.
- Interfacing MCU / PLD / FPGA based designs to USB
- PDA to USB data transfer
- USB Smart Card Readers
- USB Instrumentation
- USB Industrial Control
- USB MP3 Player Interface
- USB FLASH Card Reader / Writers
- Set Top Box PC - USB interface
- USB Digital Camera Interface
- USB Bar Code Readers

### 1.1 Driver Support

The FT4232H requires USB drivers (listed below), available free from <http://www.ftdichip.com>, which are used to make the FT4232H appear as a virtual COM port (VCP). This allows the user to communicate with the USB interface via a standard PC serial emulation port (for example TTY). Another FTDI USB driver, the D2XX driver, can also be used with application software to directly access the FT4232H through a DLL.

#### **Royalty free VIRTUAL COM PORT (VCP) DRIVERS for...**

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows 98, 98SE, ME, 2000, Server 2003, XP, Server 2008 and server 2012 R2
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Mac OS 8/9, OS-X
- Linux 2.4 and greater

#### **Royalty free D2XX Direct Drivers (USB Drivers + DLL S/W Interface)**

- Windows 10 32,64-bit
- Windows 8/8.1 32,64-bit
- Windows 7 32,64-bit
- Windows Vista and Vista 64-bit
- Windows XP and XP 64-bit
- Windows 98, 98SE, ME, 2000, Server 2003, XP, Server 2008 and server 2012 R2
- Windows XP Embedded
- Windows CE 4.2, 5.0 and 6.0
- Linux 2.4 and greater
- Android(J2xx)

For driver installation, please refer to the installation guides on our website:

<http://www.ftdichip.com/Support/Documents/InstallGuides.htm>

The following additional installation guides application notes and technical notes are also available:

- [AN\\_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus"](#).
- [AN\\_109 - "Programming Guide for High Speed FT232RL DLL"](#)
- [AN\\_110 - "Programming Guide for High Speed FT232RL JTAG DLL"](#)
- [AN\\_111 - "Programming Guide for High Speed FT232RL SPI DLL"](#)
- [AN\\_113 - "Interfacing FT2232H Hi-Speed Devices To I2C Bus"](#)
- [AN114 - "Interfacing FT2232H Hi-Speed Devices To SPI Bus"](#)
- [AN135 - MPSSE Basics](#)
- [AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes](#)

- [TN\\_104, "Guide to Debugging Customers Failed Driver Installation"](#)

## 1.2 Part Numbers

| Part Number      | Package     |
|------------------|-------------|
| FT4232HL-XXXX    | 64 Pin LQFP |
| FT4232HQ-XXXX    | 64 Pin QFN  |
| FT4232H-56Q-XXXX | 56 Pin VQFN |

**Note:** Packaging codes for xxxx is:

- Reel: Taped and Reel (LQFP =1000 pcs per reel, QFN-64 =4000 pcs per reel, QFN-56 = 3000 pcs per reel)

- Tray: Tray packing, (LQFP =160 pcs per tray, QFN-64 =260 pcs per tray, QFN-56 = 260 pcs per tray)

Please refer to section 8 for all package mechanical parameters.

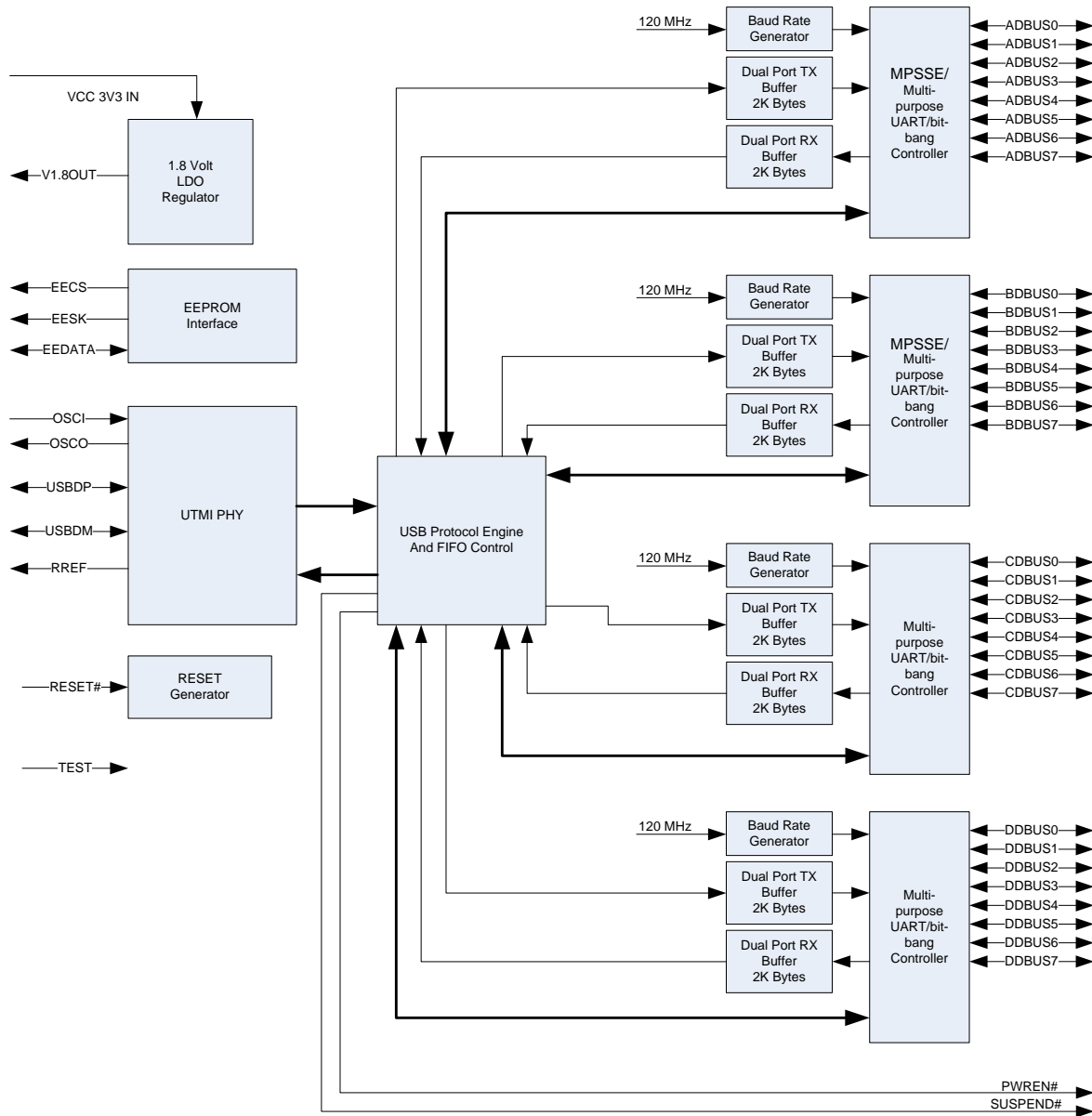
## 1.3 USB Compliant

The FT4232H is fully compliant with the USB 2.0 specification and has been given the USB-IF Test-ID (TID) 40720024.

The timing of the rise/fall time of the USB signals is not only dependant on the USB signal drivers, it is also dependant system and is affected by factors such as PCB layout, external components and any transient protection present on the USB signals. For USB compliance these may require a slight adjustment. This timing can be modified through a programmable setting stored in the same external EEPROM that is used for the USB descriptors. Timing can also be changed by adding appropriate passive components to the USB signals.



## 2 FT4232H Block Diagram



**Figure 2.1 FT4232H Block Diagram**

For a description of each function please refer to Section 4.

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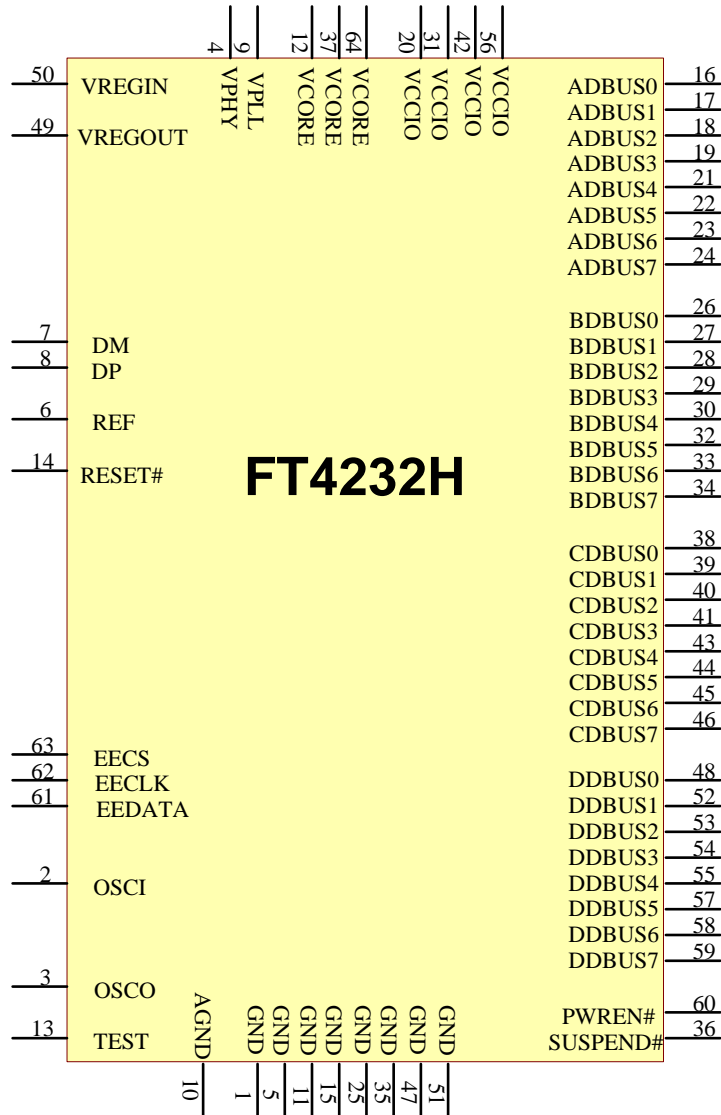
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### 3 Device Pin Out and Signal Description

#### 3.1 64-pin LQFP and QFN Package

The 64-pin LQFP and 64-pin QFN have the same pin numbering for specific functions. This pin numbering is illustrated in the schematic symbol shown in **Figure 3.1**.

##### 3.1.1 Schematic Symbol



**Figure 3.1 FT4232HL and FT4232HQ Schematic Symbol**

##### 3.1.2 Pin Descriptions

This section describes the operation of the FT4232H pins for 64-pin LQFP and 64-pin QFN. Both the 64-pin QFN and LQFP packages have the same function on each pin. The function of many pins is determined by the configuration of the FT4232H. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions is described in Table 3.1.

**Note:** The convention used throughout this document for active low signals is the signal name followed by #

| <b>FT4232HL and FT4232HQ (64-pin)</b> |           |  |                |               |                             |
|---------------------------------------|-----------|--|----------------|---------------|-----------------------------|
| <b>Pins</b>                           |           | <b>Pin functions (depend on configuration)</b> |                |               |                             |
| Pin #                                 | Pin Name  | ASYNC Serial (RS232)                           | ASYNC Bit-bang | SYNC Bit-bang | MPSSE                       |
| <b>Channel A</b>                      |           |  |                |               |                             |
| 16                                    | ADBUS0    | TXD  | D0             | D0            | TCK/SK                      |
| 17                                    | ADBUS1    | RXD  | D1             | D1            | TDI/DO                      |
| 18                                    | ADBUS2    | RTS#   | D2             | D2            | TDO/DI                      |
| 19                                    | ADBUS3    | CTS#   | D3             | D3            | TMS/CS                      |
| 21                                    | ADBUS4    | DTR#   | D4             | D4            | GPIOL0                      |
| 22                                    | ADBUS5    | DSR#   | D5             | D5            | GPIOL1                      |
| 23                                    | ADBUS6    | DCD#   | D6             | D6            | GPIOL2                      |
| 24                                    | ADBUS7    | RI#/ TXDEN*                                    | D7             | D7            | GPIOL3                      |
| <b>Channel B</b>                      |           |  |                |               |                             |
| 26                                    | BDBUS0    | TXD  | D0             | D0            | TCK/SK                      |
| 27                                    | BDBUS1    | RXD  | D1             | D1            | TDI/DO                      |
| 28                                    | BDBUS2    | RTS#   | D2             | D2            | TDO/DI                      |
| 29                                    | BDBUS3    | CTS#   | D3             | D3            | TMS/CS                      |
| 30                                    | BDBUS4    | DTR#   | D4             | D4            | GPIOL0                      |
| 32                                    | BDBUS5    | DSR#   | D5             | D5            | GPIOL1                      |
| 33                                    | BDBUS6    | DCD#   | D6             | D6            | GPIOL2                      |
| 34                                    | BDBUS7    | RI#/ TXDEN*                                    | D7             | D7            | GPIOL3                      |
| <b>Channel C</b>                      |           |  |                |               |                             |
| 38                                    | CDBUS0    | TXD  | D0             | D0            | RS232 or Bit-Bang interface |
| 39                                    | CDBUS1    | RXD  | D1             | D1            | RS232 or Bit-Bang interface |
| 40                                    | CDBUS2    | RTS#   | D2             | D2            | RS232 or Bit-Bang interface |
| 41                                    | CDBUS3    | CTS#   | D3             | D3            | RS232 or Bit-Bang interface |
| 43                                    | CDBUS4    | DTR#   | D4             | D4            | RS232 or Bit-Bang interface |
| 44                                    | CDBUS5    | DSR#   | D5             | D5            | RS232 or Bit-Bang interface |
| 45                                    | CDBUS6    | DCD#   | D6             | D6            | RS232 or Bit-Bang interface |
| 46                                    | CDBUS7    | RI#/ TXDEN*                                    | D7             | D7            | RS232 or Bit-Bang interface |
| <b>Channel D</b>                      |           |  |                |               |                             |
| 48                                    | DDBUS0    | TXD  | D0             | D0            | RS232 or Bit-Bang interface |
| 52                                    | DDBUS1    | RXD  | D1             | D1            | RS232 or Bit-Bang interface |
| 53                                    | DDBUS2    | RTS#   | D2             | D2            | RS232 or Bit-Bang interface |
| 54                                    | DDBUS3    | CTS#   | D3             | D3            | RS232 or Bit-Bang interface |
| 55                                    | DDBUS4    | DTR#   | D4             | D4            | RS232 or Bit-Bang interface |
| 57                                    | DDBUS5    | DSR#   | D5             | D5            | RS232 or Bit-Bang interface |
| 58                                    | DDBUS6    | DCD#   | D6             | D6            | RS232 or Bit-Bang interface |
| 59                                    | DDBUS7    | RI#/ TXDEN*                                    | D7             | D7            | RS232 or Bit-Bang interface |
| 60                                    | PWREN#    | PWREN#   | PWREN#         | PWREN#        | PWREN#                      |
| 36                                    | SUSPEND # | SUSPEND#                                       | SUSPEND#       | SUSPEND#      | SUSPEND#                    |
| <b>Configuration memory interface</b> |           |  |                |               |                             |



|    |        |  |
|----|--------|--|
| 63 | EECS   |  |
| 62 | EECLK  |  |
| 61 | EEDATA |  |

**Table 3.1 FT4232H Pin Configurations for 64-pin QFN and LQFP package**

\* RI#/ or TXDEN is selectable in the EEPROM. Default is RI#.

### 3.1.3 Common Pins

The operation of the following FT4232H pins are the same regardless of the configured mode:-

| Pin No.                      | Name    | Type         | Description   |
|------------------------------|---------|--------------|---|
| <b>12,37,64</b>              | VCORE   | POWER Input  | +1.8V input. Core supply voltage input.   |
| <b>20,31,42,56</b>           | VCCIO   | POWER Input  | +3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.  |
| <b>9</b>                     | VPLL    | POWER Input  | +3.3V input. Internal PHY PLL power supply input. It is recommended that this supply is filtered using an LC filter.  |
| <b>4</b>                     | VPHY    | POWER Input  | +3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter. |
| <b>50</b>                    | VREGIN  | POWER Input  | +3.3V Input. Integrated 1.8V voltage regulator input.   |
| <b>49</b>                    | VREGOUT | POWER Output | +1.8V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor.  |
| <b>10</b>                    | AGND    | POWER Input  | 0V Analog ground.   |
| <b>1,5,11,15,25,35,47,51</b> | GND     | POWER Input  | 0V Ground input.  |

**Table 3.2 Power and Ground for 64-pin QFN and LQFP package**

| Pin No.   | Name     | Type   | Description   |
|-----------|----------|--------|---|
| <b>2</b>  | OSCI     | INPUT  | Oscillator input.   |
| <b>3</b>  | OSCO     | OUTPUT | Oscillator output.  |
| <b>6</b>  | REF      | INPUT  | Current reference – connect via a 12K Ohm resistor @ 1% to GND.   |
| <b>7</b>  | DM       | I/O    | USB Data Signal Minus.  |
| <b>8</b>  | DP       | I/O    | USB Data Signal Plus.   |
| <b>13</b> | TEST     | INPUT  | IC test pin – for normal operation should be connected to GND.  |
| <b>14</b> | RESET#   | INPUT  | Reset input (active low).   |
| <b>60</b> | PWREN#   | OUTPUT | Active low power-enable output.<br>PWREN# = 0: Normal operation.<br>PWREN# =1: USB SUSPEND mode or device has not been configured. This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured. |
| <b>36</b> | SUSPEND# | OUTPUT | Active low when USB is in suspend mode.   |

**Table 3.3 Common Function pins for 64-pin QFN and LQFP Package**

| Pin No.   | Name   | Type   | Description   |
|-----------|--------|--------|---|
| <b>63</b> | EECS   | I/O    | EEPROM – Chip Select. Tri-State during device reset.  |
| <b>62</b> | EECLK  | OUTPUT | Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.                                  |
| <b>61</b> | EEDATA | I/O    | EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the |

|  |  |  |  |
|--|--|--|--|
|  |  |  | EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset. |
|--|--|--|--|

**Table 3.4 EEPROM Interface Group for 64-pin QFN and LQFP Package**

### 3.1.4 Configured Pins

The following sections describe the function of the configurable pins referred to in Table 3.1 which is determined by how the FT4232H is configured.

#### 3.1.4.1 FT4232H Pins used as an Asynchronous Serial Interface

Any of the 4 channels of the FT4232H can be configured as an asynchronous serial UART interface (RS232/422/485). When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.5**.

| Channel A Pin No. | Channel B Pin No. | Channel C Pin No. | Channel D Pin No. | Name          | Type         | RS232 Configuration Description   |
|-------------------|-------------------|-------------------|-------------------|---------------|--------------|---|
| 16                | 26                | 38                | 48                | TXD           | OUTPUT       | TXD = transmitter output  |
| 17                | 27                | 39                | 52                | RXD           | INPUT        | RXD = receiver input  |
| 18                | 28                | 40                | 53                | RTS#          | OUTPUT       | RTS# = Ready To send handshake output   |
| 19                | 29                | 41                | 54                | CTS#          | INPUT        | CTS# = Clear To Send handshake input  |
| 21                | 30                | 43                | 55                | DTR#          | OUTPUT       | DTR# = Data Transmit Ready modem signaling line   |
| 22                | 32                | 44                | 57                | DSR#          | INPUT        | DSR# = Data Set Ready modem signaling line  |
| 23                | 33                | 45                | 58                | DCD#          | INPUT        | DCD# = Data Carrier Detect modem signaling line   |
| 24                | 34                | 46                | 59                | RI#/<br>TXDEN | INPUT/OUTPUT | RI# = Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (see note 1, 2 and 3)<br>TXDEN = (TTL level). For use with RS485 level converters. |

**Table 3.5 Channel A, B, C and D Asynchronous Serial Interface Configured Pin Descriptions**

#### Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. If remote wake-up is enabled, a peripheral is allowed to draw up to 2.5mA in suspend. If remote wake-up is disabled, the peripheral must draw no more than 500uA in suspend.
3. If a Pull-down is enabled, the FT4232H will not wake up from suspend.

#### 3.1.4.2 FT4232H Pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT4232H channel A, B, C or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

When configured in any bit-bang mode (synchronous or asynchronous), the pins used and the descriptions of the signals are shown in **Table 3.6**

| Channel Number | Pin Nos.                    | Name       | Type | Synchronous or Asynchronous Bit-Bang Configuration Description |
|----------------|-----------------------------|------------|------|--|
| A              | 24,23,22,21,<br>19,18,17,16 | ADBUS[7:0] | I/O  | Channel A, D7 to D0 bidirectional bit-bang data                |

|          |                                     |            |     |   |
|----------|-------------------------------------|------------|-----|---|
| <i>B</i> | <b>34,33,32,30,<br/>29,28,27,26</b> | BDBUS[7:0] | I/O | Channel B, D7 to D0 bidirectional bit-bang data |
| <i>C</i> | <b>46,45,44,43,<br/>41,40,39,38</b> | CDBUS[7:0] | I/O | Channel C, D7 to D0 bidirectional bit-bang data |
| <i>D</i> | <b>59,58,57,55<br/>54,53,52,48</b>  | DDBUS[7:0] | I/O | Channel D, D7 to D0 bidirectional bit-bang data |

**Table 3.6 Channel A, B, C & D Synchronous/Asynchronous Bit-Bang Configured Pin Descriptions**

For a functional description of this mode, please refer to section 4.5 Synchronous & Asynchronous Bit-Bang Interface Mode Desc.

### 3.1.4.3 FT4232H pins used in an MPSSE

The FT4232H channel A and channel B, each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I<sup>2</sup>C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT4232H's channels (e.g. channel A) to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other MPSSE channel (e.g. channel B) would be available for another serial interface function while channel C and channel D can be configured as UART or bit-bang mode. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.7**

| <b>Channel A Pin No.</b> | <b>Channel B Pin No.</b> | <b>Name</b> | <b>Type</b> | <b>MPSSE Configuration Description</b>   |
|--------------------------|--------------------------|-------------|-------------|--|
| <b>16</b>                | <b>26</b>                | TCK/SK      | OUTPUT      | Clock Signal Output. For example:<br>JTAG – TCK, Test interface clock<br>SPI – SK, Serial Clock    |
| <b>17</b>                | <b>27</b>                | TDI/DO      | OUTPUT      | Serial Data Output. For example:<br>JTAG – TDI, Test Data Input<br>SPI – DO, serial data output    |
| <b>18</b>                | <b>28</b>                | TDO/DI      | INPUT       | Serial Data Input. For example:<br>JTAG – TDO, Test Data output<br>SPI – DI, Serial Data Input     |
| <b>19</b>                | <b>29</b>                | TMS/CS      | OUTPUT      | Output Signal Select. For example:<br>JTAG – TMS, Test Mode Select<br>SPI – CS, Serial Chip Select |
| <b>21</b>                | <b>30</b>                | GPIOL0      | I/O         | General Purpose input/output   |
| <b>22</b>                | <b>32</b>                | GPIOL1      | I/O         | General Purpose input/output   |
| <b>23</b>                | <b>33</b>                | GPIOL2      | I/O         | General Purpose input/output   |
| <b>24</b>                | <b>34</b>                | GPIOL3      | I/O         | General Purpose input/output   |

**Table 3.7 Channel A and Channel B MPSSE Configured Pin Descriptions**

For a functional description of this mode, please refer to section 4.4.

When either Channel A or Channel B or both channels are used in MPSSE mode, Channel C and Channel D can be configured as asynchronous serial interface (RS232/422/485) or Bit-Bang mode or a combination of both.

## 3.2 56-pin VQFN Package

The 56-pin VQFN with lower pin count and small size package is also available for the FT4232H. The differences exist on power/ground and pin number for each pin. The part number is FT4232H-56Q to distinguish it from the 64-pin package type. All the functions are supported in the 56-pin VQFN package. The pin numbering is illustrated in the schematic symbol shown in Figure 3.2.

### 3.2.1 Schematic Symbol for FT4232H-56Q

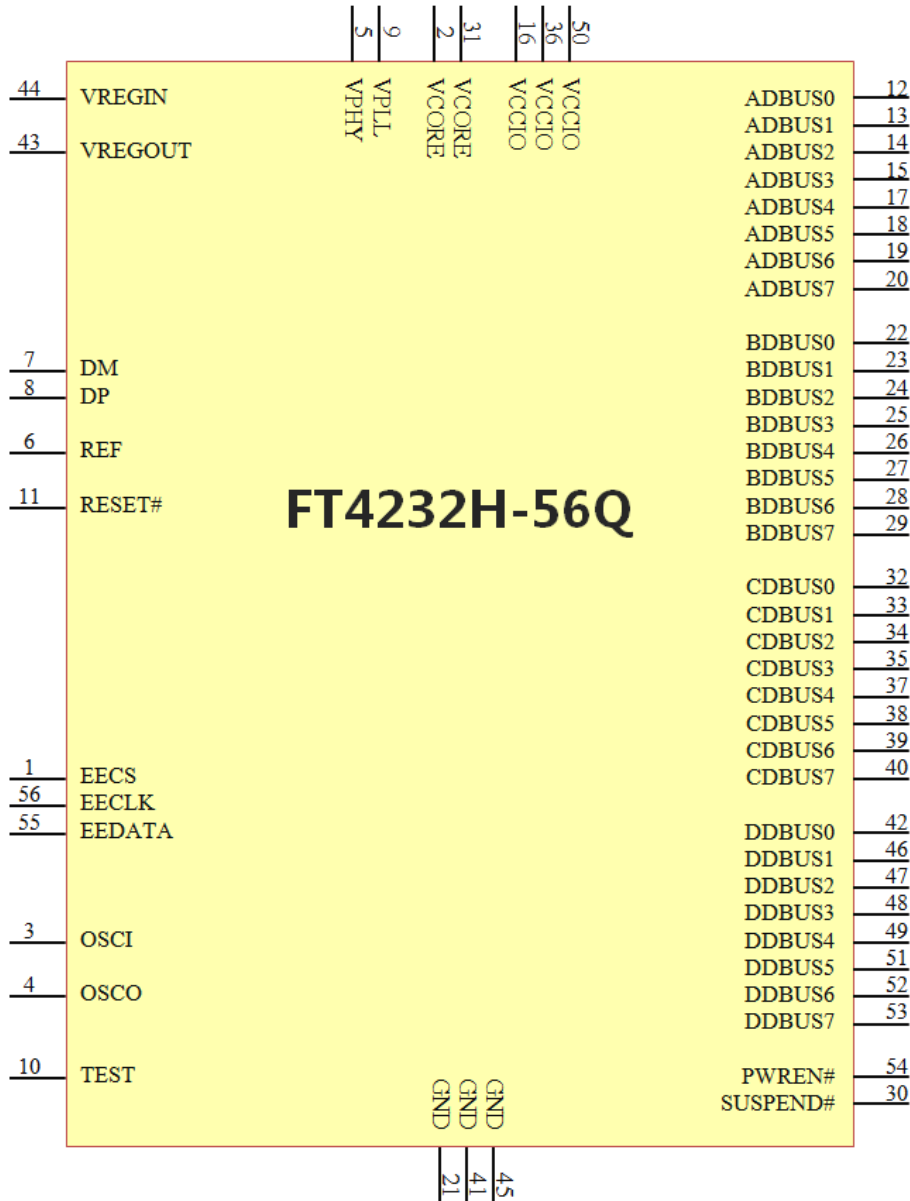


Figure 3.2 FT4232H-56Q Schematic Symbol

### 3.2.2 Pin Descriptions for FT4232H-56Q

This section describes the operation of the FT4232H-56Q pins for 56-pin VQFN package. The function of many pins is determined by the configuration of the FT4232H-56Q. The following table details the function of each pin dependent on the configuration of the interface. Each of the functions is described in Table 3.8.

**Note:** The convention used throughout this document for active low signals is the signal name followed by #

| FT4232H-56Q      |          |   |                |               |        |
|------------------|----------|---|----------------|---------------|--------|
| Pins             |          | Pin functions (depend on configuration) |                |               |        |
| Pin #            | Pin Name | ASYNC Serial (RS232)                    | ASYNC Bit-bang | SYNC Bit-bang | MP SSE |
| <b>Channel A</b> |          |   |                |               |        |
| 12               | ADBUS0   | TXD                                     | D0             | D0            | TCK/SK |
| 13               | ADBUS1   | RXD                                     | D1             | D1            | TDI/DO |

|                                       |          |             |          |          |                             |
|---------------------------------------|----------|-------------|----------|----------|-----------------------------|
| 14                                    | ADBUS2   | RTS#        | D2       | D2       | TDO/DI                      |
| 15                                    | ADBUS3   | CTS#        | D3       | D3       | TMS/CS                      |
| 17                                    | ADBUS4   | DTR#        | D4       | D4       | GPIOL0                      |
| 18                                    | ADBUS5   | DSR#        | D5       | D5       | GPIOL1                      |
| 19                                    | ADBUS6   | DCD#        | D6       | D6       | GPIOL2                      |
| 20                                    | ADBUS7   | RI#/ TXDEN* | D7       | D7       | GPIOL3                      |
| <b>Channel B</b>                      |          |             |          |          |                             |
| 22                                    | BDBUS0   | TXD         | D0       | D0       | TCK/SK                      |
| 23                                    | BDBUS1   | RXD         | D1       | D1       | TDI/DO                      |
| 24                                    | BDBUS2   | RTS#        | D2       | D2       | TDO/DI                      |
| 25                                    | BDBUS3   | CTS#        | D3       | D3       | TMS/CS                      |
| 26                                    | BDBUS4   | DTR#        | D4       | D4       | GPIOL0                      |
| 27                                    | BDBUS5   | DSR#        | D5       | D5       | GPIOL1                      |
| 28                                    | BDBUS6   | DCD#        | D6       | D6       | GPIOL2                      |
| 29                                    | BDBUS7   | RI#/ TXDEN* | D7       | D7       | GPIOL3                      |
| <b>Channel C</b>                      |          |             |          |          |                             |
| 32                                    | CDBUS0   | TXD         | D0       | D0       | RS232 or Bit-Bang interface |
| 33                                    | CDBUS1   | RXD         | D1       | D1       | RS232 or Bit-Bang interface |
| 34                                    | CDBUS2   | RTS#        | D2       | D2       | RS232 or Bit-Bang interface |
| 35                                    | CDBUS3   | CTS#        | D3       | D3       | RS232 or Bit-Bang interface |
| 37                                    | CDBUS4   | DTR#        | D4       | D4       | RS232 or Bit-Bang interface |
| 38                                    | CDBUS5   | DSR#        | D5       | D5       | RS232 or Bit-Bang interface |
| 39                                    | CDBUS6   | DCD#        | D6       | D6       | RS232 or Bit-Bang interface |
| 40                                    | CDBUS7   | RI#/ TXDEN* | D7       | D7       | RS232 or Bit-Bang interface |
| <b>Channel D</b>                      |          |             |          |          |                             |
| 42                                    | DDBUS0   | TXD         | D0       | D0       | RS232 or Bit-Bang interface |
| 46                                    | DDBUS1   | RXD         | D1       | D1       | RS232 or Bit-Bang interface |
| 47                                    | DDBUS2   | RTS#        | D2       | D2       | RS232 or Bit-Bang interface |
| 48                                    | DDBUS3   | CTS#        | D3       | D3       | RS232 or Bit-Bang interface |
| 49                                    | DDBUS4   | DTR#        | D4       | D4       | RS232 or Bit-Bang interface |
| 51                                    | DDBUS5   | DSR#        | D5       | D5       | RS232 or Bit-Bang interface |
| 52                                    | DDBUS6   | DCD#        | D6       | D6       | RS232 or Bit-Bang interface |
| 53                                    | DDBUS7   | RI#/ TXDEN* | D7       | D7       | RS232 or Bit-Bang interface |
| 54                                    | PWREN#   | PWREN#      | PWREN#   | PWREN#   | PWREN#                      |
| 30                                    | SUSPEND# | SUSPEND#    | SUSPEND# | SUSPEND# | SUSPEND#                    |
| <b>Configuration memory interface</b> |          |             |          |          |                             |
| 1                                     | EECS     |             |          |          |                             |
| 56                                    | EECLK    |             |          |          |                             |
| 55                                    | EEDATA   |             |          |          |                             |

**Table 3.8 FT4232H Pin Configurations for 56-Pin VQFN Package**

\* RI#/ or TXDEN is selectable in the EEPROM. Default is RI#.

### 3.2.3 Common Pins for FT4232H-56Q

The operation of the following FT4232H-56Q pins are the same regardless of the configured mode:-

| Pin No.         | Name    | Type         | Description   |
|-----------------|---------|--------------|---|
| <b>2,31</b>     | VCORE   | POWER Input  | +1.8V input. Core supply voltage input.   |
| <b>16,36,50</b> | VCCIO   | POWER Input  | +3.3V input. I/O interface power supply input. Failure to connect all VCCIO pins will result in failure of the device.  |
| <b>9</b>        | VPLL    | POWER Input  | +3.3V input. Internal PHY PLL power supply input. It is recommended that this supply is filtered using an LC filter.  |
| <b>5</b>        | VPHY    | POWER Input  | +3.3V Input. Internal USB PHY power supply input. Note that this cannot be connected directly to the USB supply. A +3.3V regulator must be used. It is recommended that this supply is filtered using an LC filter. |
| <b>44</b>       | VREGIN  | POWER Input  | +3.3V Input. Integrated 1.8V voltage regulator input.   |
| <b>43</b>       | VREGOUT | POWER Output | +1.8V Output. Integrated voltage regulator output. Connect to VCORE with 3.3uF filter capacitor.  |
| <b>21,41,45</b> | GND     | POWER Input  | 0V Ground input.  |

**Table 3.9 Power and Ground for 56-pin VQFN package**

| Pin No.   | Name     | Type   | Description   |
|-----------|----------|--------|---|
| <b>3</b>  | OSCI     | INPUT  | Oscillator input.   |
| <b>4</b>  | OSCO     | OUTPUT | Oscillator output.  |
| <b>6</b>  | REF      | INPUT  | Current reference – connect via a 12K Ohm resistor @ 1% to GND.   |
| <b>7</b>  | DM       | INPUT  | USB Data Signal Minus.  |
| <b>8</b>  | DP       | INPUT  | USB Data Signal Plus.   |
| <b>10</b> | TEST     | INPUT  | IC test pin – for normal operation should be connected to GND.  |
| <b>11</b> | RESET#   | INPUT  | Reset input (active low).   |
| <b>54</b> | PWREN#   | OUTPUT | Active low power-enable output.<br>PWREN# = 0: Normal operation.<br>PWREN# = 1: USB SUSPEND mode or device has not been configured.<br>This can be used by external circuitry to power down logic when device is in USB suspend or has not been configured. |
| <b>30</b> | SUSPEND# | OUTPUT | Active low when USB is in suspend mode.   |

**Table 3.10 Common Function pins for 56-pin VQFN Package**

| Pin No.   | Name   | Type   | Description  |
|-----------|--------|--------|--|
| <b>1</b>  | EECS   | I/O    | EEPROM – Chip Select. Tri-State during device reset.   |
| <b>56</b> | EECLK  | OUTPUT | Clock signal to EEPROM. Tri-State during device reset. When not in reset, this outputs the EEPROM clock.   |
| <b>55</b> | EEDATA | I/O    | EEPROM – Data I/O Connect directly to Data-In of the EEPROM and to Data-Out of the EEPROM via a 2.2K resistor. Also, pull Data-Out of the EEPROM to VCC via a 10K resistor for correct operation. Tri-State during device reset. |

**Table 3.11 EEPROM Interface Group for 56-pin VQFN Package**

### 3.2.4 Configured Pins for FT4232H-56Q

The following sections describe the function of the configurable pins referred to in Table 3.8 which is determined by how the FT4232H-56Q is configured.

#### 3.2.4.1 FT4232H-56Q pins used as an asynchronous serial interface

Any of the 4 channels of the FT4232H-56Q can be configured as an asynchronous serial UART interface (RS232/422/485). When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.12**.

| Channel A Pin No. | Channel B Pin No. | Channel C Pin No. | Channel D Pin No. | Name          | Type         | RS232 Configuration Description   |
|-------------------|-------------------|-------------------|-------------------|---------------|--------------|---|
| 12                | 22                | 32                | 42                | TXD           | OUTPUT       | TXD = transmitter output  |
| 13                | 23                | 33                | 46                | RXD           | INPUT        | RXD = receiver input  |
| 14                | 24                | 34                | 47                | RTS#          | OUTPUT       | RTS# = Ready To send handshake output   |
| 15                | 25                | 35                | 48                | CTS#          | INPUT        | CTS# = Clear To Send handshake input  |
| 17                | 26                | 37                | 49                | DTR#          | OUTPUT       | DTR# = Data Transmit Ready modem signaling line   |
| 18                | 27                | 38                | 51                | DSR#          | INPUT        | DSR# = Data Set Ready modem signaling line  |
| 19                | 28                | 39                | 52                | DCD#          | INPUT        | DCD# = Data Carrier Detect modem signaling line   |
| 20                | 29                | 40                | 53                | RI#/<br>TXDEN | INPUT/OUTPUT | RI# = Ring Indicator Control Input. When the Remote Wake up option is enabled in the EEPROM, taking RI# low can be used to resume the PC USB Host controller from suspend. (see note 1, 2 and 3)<br>TXDEN = (TTL level). For use with RS485 level converters. |

**Table 3.12 Channel A, B, C & D Asynchronous Serial Interface Configured Pin Desc. for FT4232H-56Q**

#### Notes

1. When using remote wake-up, ensure the resistors are pulled-up in suspend. Also ensure peripheral designs do not allow any current sink paths that may partially power the peripheral.
2. If remote wake-up is enabled, a peripheral is allowed to draw up to 2.5mA in suspend. If remote wake-up is disabled, the peripheral must draw no more than 500uA in suspend.
3. If a Pull-down is enabled, the FT4232H will not wake up from suspend.

#### 3.2.4.2 FT4232H-56Q pins used in a Synchronous or Asynchronous Bit-Bang Interface

The FT4232H channel A, B, C or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous. When configured in any bit-bang mode (synchronous or asynchronous), the pins used and the descriptions of the signals are shown in **Table 3.13**

| Channel Number | Pin Nos.                | Name        | Type | Synchronous or Asynchronous Bit-Bang Configuration Description |
|----------------|-------------------------|-------------|------|--|
| A              | 20,19,18,17,15,14,13,12 | ADBUSB[7:0] | I/O  | Channel A, D7 to D0 bidirectional bit-bang data                |
| B              | 29,28,27,26,25,24,23,22 | BDBUSB[7:0] | I/O  | Channel B, D7 to D0 bidirectional bit-bang data                |
| C              | 40,39,38,37,            | CDBUSB[7:0] | I/O  | Channel C, D7 to D0 bidirectional bit-bang data                |

|          |                                    |            |     |   |
|----------|------------------------------------|------------|-----|---|
|          | <b>35,34,33,32</b>                 |            |     |   |
| <i>D</i> | <b>53,52,51,49<br/>48,47,46,42</b> | DDBUS[7:0] | I/O | Channel D, D7 to D0 bidirectional bit-bang data |

**Table 3.13 Channel A, B, C & D Synchronous/Asynchronous Bit-Bang Configured Pin Desc. for FT4232H-56Q**

For a functional description of this mode, please refer to section 4.5 Synchronous & Asynchronous Bit-Bang Interface Mode Desc.

### 3.2.4.3 FT4232H-56Q pins used in an MPSSE

The FT4232H channel A and channel B, each have a Multi-Protocol Synchronous Serial Engine (MPSSE). Each MPSSE can be independently configured to a number of industry standard serial interface protocols such as JTAG, I2C or SPI, or it can be used to implement a proprietary bus protocol. For example, it is possible to use one of the FT4232H's channels (e.g. channel A) to connect to an SRAM configurable FPGA such as supplied by Altera or Xilinx. The FPGA device would normally be un-configured (i.e. have no defined function) at power-up. Application software on the PC could use the MPSSE to download configuration data to the FPGA over USB. This data would define the hardware function on power up. The other MPSSE channel (e.g. channel B) would be available for another serial interface function while channel C and channel D can be configured as UART or bit-bang mode. Alternatively each MPSSE can be used to control a number of GPIO pins. When configured in this mode, the pins used and the descriptions of the signals are shown in **Table 3.14**

| Channel A Pin No. | Channel B Pin No. | Name   | Type   | MPSSE Configuration Description  |
|-------------------|-------------------|--------|--------|--|
| <b>12</b>         | <b>22</b>         | TCK/SK | OUTPUT | Clock Signal Output. For example:<br>JTAG – TCK, Test interface clock<br>SPI – SK, Serial Clock    |
| <b>13</b>         | <b>23</b>         | TDI/DO | OUTPUT | Serial Data Output. For example:<br>JTAG – TDI, Test Data Input<br>SPI – DO, serial data output    |
| <b>14</b>         | <b>24</b>         | TDO/DI | INPUT  | Serial Data Input. For example:<br>JTAG – TDO, Test Data output<br>SPI – DI, Serial Data Input     |
| <b>15</b>         | <b>25</b>         | TMS/CS | OUTPUT | Output Signal Select. For example:<br>JTAG – TMS, Test Mode Select<br>SPI – CS, Serial Chip Select |
| <b>17</b>         | <b>26</b>         | GPIOL0 | I/O    | General Purpose input/output   |
| <b>18</b>         | <b>27</b>         | GPIOL1 | I/O    | General Purpose input/output   |
| <b>19</b>         | <b>28</b>         | GPIOL2 | I/O    | General Purpose input/output   |
| <b>20</b>         | <b>29</b>         | GPIOL3 | I/O    | General Purpose input/output   |

**Table 3.14 Channel A and Channel B MPSSE Configured Pin Descriptions for FT4232H-56Q**

For a functional description of this mode, please refer to section 4.4.

When either Channel A or Channel B or both channels are used in MPSSE mode, Channel C and Channel D can be configured as asynchronous serial interface (RS232/422/485) or Bit-Bang mode or a combination of both.



## 4 Function Description

The FT4232H is FTDI's 5<sup>th</sup> generation of USB devices. The FT4232H is a USB 2.0 High Speed (480Mb/s) to UART/MPSSE ICs. It has the capability of being configured in a variety of industry standard serial interfaces.

The FT4232H has four independent configurable interfaces. Two of these interfaces can be configured as UART, JTAG, SPI, I<sup>2</sup>C or bit-bang mode, using an MPSSE, with independent baud rate generators. The remaining two interfaces can be configured as UART or bit-bang.

### 4.1 Key Features

**USB High Speed to Quad Interface.** The FT4232H is a USB 2.0 High Speed (480Mbits/s) to four independent flexible/configurable serial interfaces.

**Functional Integration.** The FT4232H integrates a USB protocol engine which controls the physical Universal Transceiver Macrocell Interface (UTMI) and handles all aspects of the USB 2.0 High Speed interface. The FT4232H includes an integrated +1.8V Low Drop-Out (LDO) regulator and 12MHz to 480MHz PLL. It also includes 2kbytes Tx and Rx data buffers per channel. The FT4232H effectively integrates the entire USB protocol on a chip.

**MPSSE.** Multi-Purpose Synchronous Serial Engines (MPSSE), capable of speeds up to 30 Mbits/s, provides flexible synchronous interface configurations.

**Data Transfer Rate.** The FT4232H supports a data transfer rate up to 12 Mbit/s when configured as an RS232/RS422/RS485 UART interface. Please note the FT4232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

**Latency Timer.** This is really a feature of the driver and is used to as a timeout to flush short packets of data back to the PC. The default is 16ms, but it can be altered between 0ms and 256ms. At 0ms latency you get a packet transfer on every high speed micro frame.

### 4.2 Functional Block Descriptions

**Quad Multi-Purpose UART/MPSSE Controllers.** The FT4232H has four independent UART/MPSSE Controllers. These blocks control the UART data or control the Bit-Bang mode if selected by the SETUP command. The blocks used on channel A and channel B also contain a MPSSE (Multi-Protocol Synchronous Serial Engine) in each of them which can be used independently of each other and the remaining UART channels. Using this it can be configured under software command to have 1 MPSSE + 3 UARTS (each UART can be set to Bit Bang mode to gain extra I/O if required) or 2 MPSSE + 2 UARTS.

**USB Protocol Engine and FIFO control.** The USB Protocol Engine controls and manages the interface between the UTMI PHY and the FIFOs of the chip. It also handles power management and the USB protocol specification.

**Dual Port FIFO TX Buffer (2Kbytes per channel).** Data from the Host PC is stored in these buffers to be used by the Multi-purpose UART/FIFO controllers. This is controlled by the USB Protocol Engine and FIFO control block.

**Dual Port FIFO RX Buffer (2Kbytes per channel).** Data from the Multi-purpose UART/FIFO controllers is stored in these blocks to be sent back to the Host PC when requested. This is controlled by the USB Protocol Engine and FIFO control block.

**RESET Generator** - The integrated Reset Generator Cell provides a reliable power-on reset to the device internal circuitry at power up. The RESET# input pin allows an external device to reset the FT4232H. RESET# should be tied to VCCIO (+3.3v) if not being used.

**Independent Baud Rate Generators** - The Baud Rate Generators provides an x16 or an x10 clock input to the UART's from a 120MHz reference clock and consists of a 14 bit pre-scaler and 4 register bits which provide fine tuning of the baud rate (used to divide by a number plus a fraction). This determines the Baud Rate of the UART which is programmable from 183 baud to 12 million baud. The FT2232H does not support the baud rates of 7 Mbaud 9 Mbaud, 10 Mbaud and 11 Mbaud.

See FTDI application note [AN232B0-5](#) for more details.

**+1.8V LDO Regulator.** The +1.8V LDO regulator generates the +1.8 volts for the core and the USB transceiver cell. Its input (VREGIN) must be connected to a +3.3V external power source. It is also recommended to add an external filtering capacitor to the VREGIN. There is no direct connection from the +1.8V output (VREGOUT) and the internal functions of the FT4232H. The PCB must be routed to connect VREGOUT to the pins that require the +1.8V including VREGIN.

**UTMI PHY.** The Universal Transceiver Macrocell Interface (UTMI) physical interface cell. This block handles the Full speed / High Speed SERDES (serialise – de-serialise) function for the USB TX/RX data. It also provides the clocks for the rest of the chip. A 12 MHz crystal should be connected to the OSCI and OSCO pins. A 12K Ohm resistor should be connected between REF and GND on the PCB.

The UTMI PHY functions include:

- Supports 480 Mbit/s "High Speed" (HS)/ 12 Mbit/s "Full Speed" (FS), FS Only and "Low Speed" (LS).
- SYNC/EOP generation and checking.
- Data and clock recovery from serial stream on the USB.
- Bit-stuffing/unstuffing; bit stuff error detection.
- Manages USB Resume, Wake Up and Suspend functions.
- Single parallel data clock output with on-chip PLL to generate higher speed serial data clocks.

**EEPROM Interface.** When used without an external EEPROM the FT4232H defaults to a quad USB to an asynchronous serial port device. Adding an external 93C46 (93C56 or 93C66) EEPROM allows customization of USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4232H for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

The EEPROM must be a 16 bit wide configuration such as a Microchip 93LC46B or equivalent capable of a 1Mbit/s clock rate at VCC = +3.00V to 3.6V. The EEPROM is programmable in-circuit over USB using a utility program called [FT\\_PROG](#) available from FTDI's web site ([www.ftdichip.com](http://www.ftdichip.com)). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process.

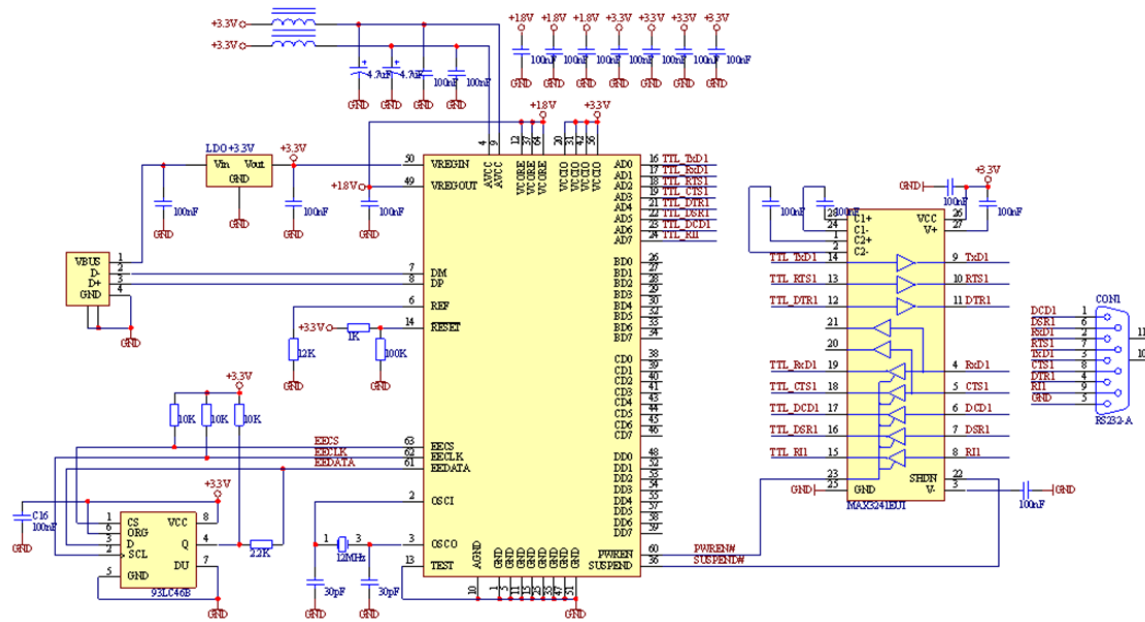
If no EEPROM is connected (or the EEPROM is blank), the FT4232H will default to serial ports. The device uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

## 4.3 FT232 UART Interface Mode Description

The FT4232H can be configured in similar UART modes as the FTDI FT232 devices (an asynchronous serial interface). The following examples illustrate how to configure the FT4232H with an RS232, RS422 or RS485 interfaces. The FT4232 can be configured as a mixture of these interfaces.

### 4.3.1 RS232 Configuration

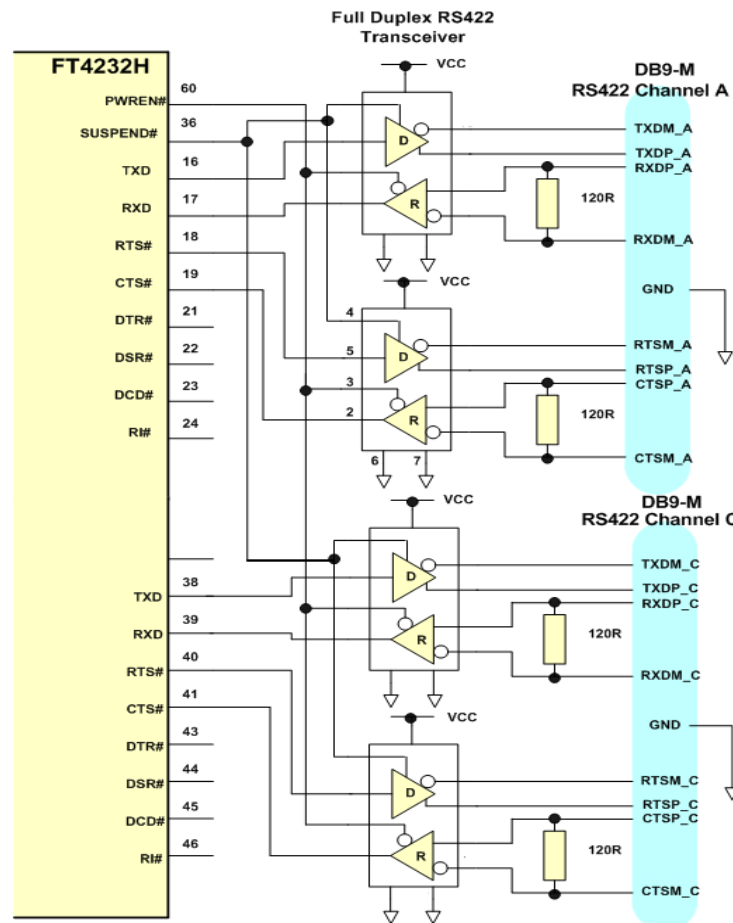
Figure 4.1 illustrates how the FT4232H channel A can be configured with an RS232 UART interface. This can be repeated for channels B, C and D to provide a quad RS232, but has been omitted for clarity.



**Figure 4.1 RS232 Configuration**

### 4.3.2 RS422 Configuration

Figure 4.2 illustrates how the FT4232H can be configured as a dual RS422 interface. The FT4232H can have all 4 channels connected as RS422, but only channel A and channel C are shown for clarity.

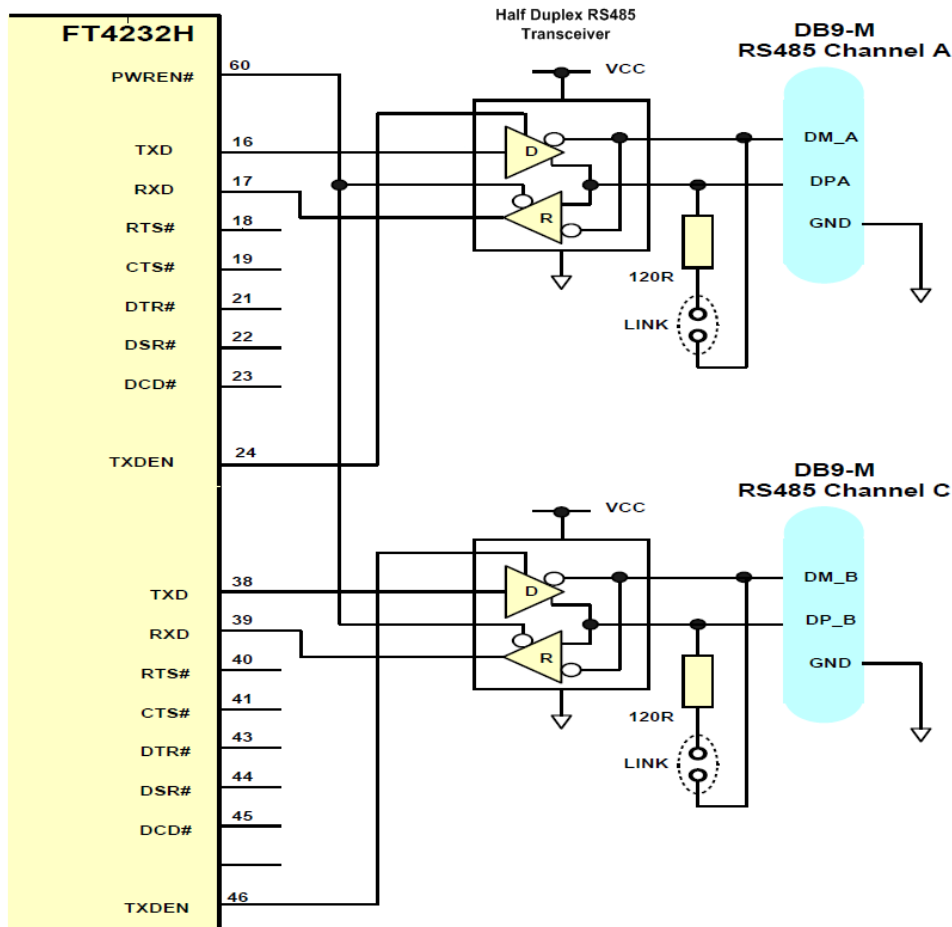


**Figure 4.2 Dual RS422 Configurations**

In this case both channel A and channel C are configured as UART operating at TTL levels and a level converter device (full duplex RS485 transceiver) is used to convert the TTL level signals from the FT4232H to RS422 levels. The PWREN# signal is used to power down the level shifters such that they operate in a low quiescent current when the USB interface is in suspend mode.

### 4.3.3 RS485 Configuration

Figure 4.3 illustrates how the FT4232H can be configured as a dual RS485 interface. The FT4232H can have all 4 channels connected as RS485, but only channel A and channel C are shown for clarity.



**Figure 4.3 Dual RS485 Configurations**

In this case both channel A and channel C are configured as RS485 operating at TTL levels and a level converter device (half duplex RS485 transceiver) is used to convert the TTL level signals from the FT232H to RS485 levels. It has separate enables on both the transmitter and receiver. With RS485, the transmitter is only enabled when a character is being transmitted from the UART. The TXDEN pins on the FT4232H are provided for exactly that purpose, and so the transmitter enables are wired to the TXDEN's. The receiver enable is active low, so it is wired to the PWREN# pin to disable the receiver when in USB suspend mode.

RS485 is a multi-drop network – i.e. many devices can communicate with each other over a single two wire cable connection. The RS485 cable requires to be terminated at each end of the cable. Links are provided to allow the cable to be terminated if the device is physically positioned at either end of the cable.

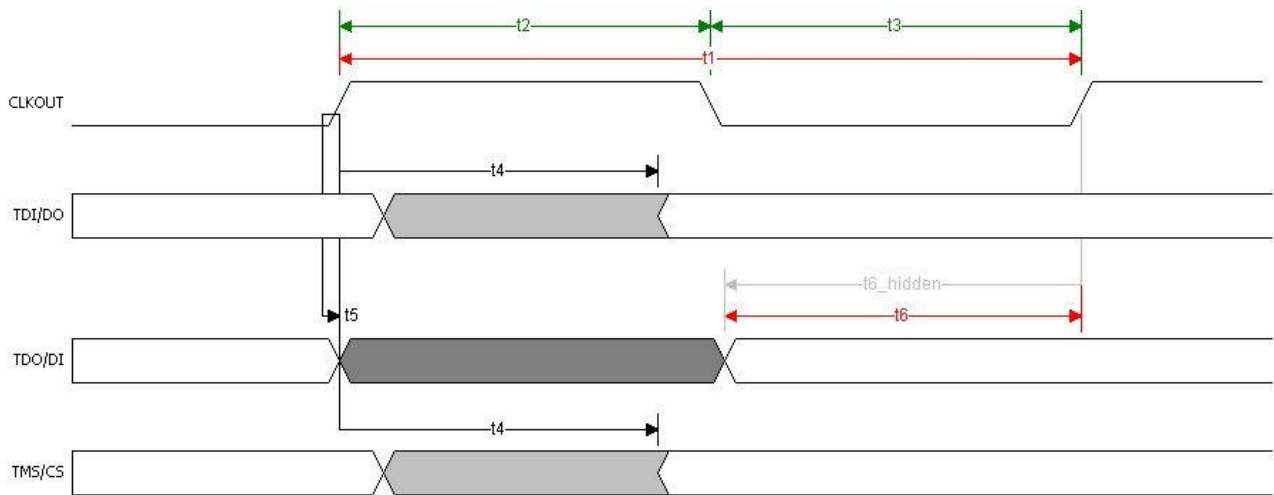
In this example the data transmitted by the FT4232H is also received by the device that is transmitting. This is a common feature of RS485 and requires the application software to remove the transmitted data from the received data stream. With the FT4232H it is possible to do this entirely in hardware – simply modify the schematic so that RXD of the FT4232H is the logical OR of the level converter device receiver output with TXDEN using an HC32 or similar logic gate.

## 4.4 MPSSE Interface Mode Description

MPSSE Mode is designed to allow the FT4232H to interface efficiently with synchronous serial protocols such as JTAG, I2C and SPI Bus. It can also be used to program SRAM based FPGA's over USB. The MPSSE interface is designed to be flexible so that it can be configured to allow any synchronous serial protocol (industry standard or proprietary) to be implemented using the FT4232H. MPSSE is only available on channel A and channel B.

MPSSE is fully configurable, and is programmed by sending commands down the data stream. These can be sent individually or more efficiently in packets. MPSSE is capable of a maximum sustained data rate of 30 Mbits/s.

When a channel is configured in MPSSE mode, the IO timing and signals used are shown in Figure 4.4 and Table 4.1. These show timings for CLKOUT=30MHz. CLKOUT can be divided internally to be provide a slower clock.



**Figure 4.4 MPSSE Signal Waveforms**

| NAME | MIN | NOM   | MAX  | Units | COMMENT                |
|------|-----|-------|------|-------|------------------------|
| t1   |     | 33.33 |      | ns    | CLKOUT period          |
| t2   | 15  | 16.67 |      | ns    | CLKOUT high period     |
| t3   | 15  | 16.67 |      | ns    | CLKOUT low period      |
| t4   | 1   |       | 7.15 | ns    | CLKOUT to TDI/DO delay |
| t5   | 0   |       |      | ns    | TDO/DI hold time       |
| t6   | 11  |       |      |       | TDO/DI setup time      |

**Table 4.1 MPSSE Signal Timings**

MPSSE mode is enabled using Set Bit Bang Mode driver command. A hex value of 2 will enable it, and a hex value of 0 will reset the device. See application note [AN2232-02, "Bit Mode Functions for the FT2232"](#) for more details and examples.

The MPSSE command set is fully described in application note [AN\\_108 – "Command Processor for MPSSE and MCU Host Bus Emulation Modes"](#).

The following additional application notes are available for configuring the MPSSE:

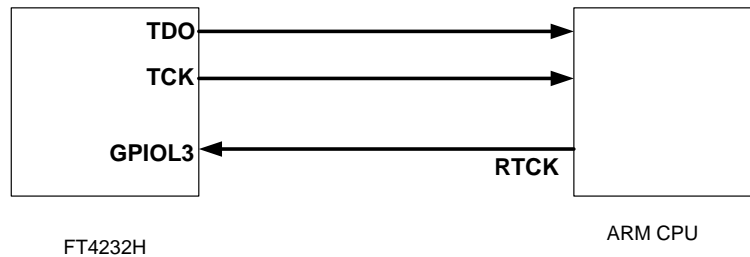
- [AN\\_109 – "Programming Guide for High Speed FTCI2C DLL"](#)
- [AN\\_110 – "Programming Guide for High Speed FTCJTAG DLL"](#)
- [AN\\_111 – "Programming Guide for High Speed FTCSPI DLL"](#)

### 4.4.1 MPSSE Adaptive Clcking

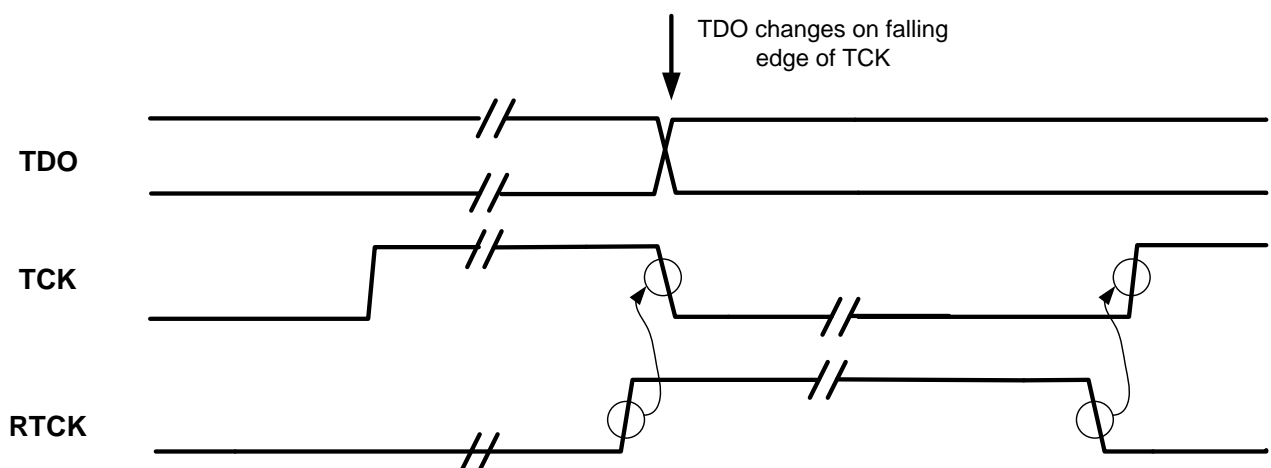
Adaptive clcking is a new MPSSE feature added to the FT24232H MPSSE engine.

The mode is effectively handshaking the CLK signal with a return clock RTCK. This is a technique used by ARM processors.

The FT4232H will assert the CLK line and wait for the RTCK to be returned from the target device to GPIOL3 line before changing the TDO (data out line).



**Figure 4.5 Adaptive Clcking Interconnect**



**Figure 4.6: Adaptive Clcking waveform**

Adaptive clcking is not enabled by default.

See: [AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes.](#)

## 4.5 Synchronous & Asynchronous Bit-Bang Interface Mode Desc.

The FT4232H channel A, B, C or channel D can be configured as a bit-bang interface. There are two types of bit-bang modes: synchronous and asynchronous.

### 4.5.1 Asynchronous Bit-Bang Mode

Asynchronous Bit-Bang mode is the same as BM-style Bit-Bang mode. On any channel configured in asynchronous bit-bang mode, data written to the device in the normal manner will be self-clocked onto the parallel I/O data pins (those which have been configured as outputs). Each I/O pin can be independently set as an input or an output. The rate that the data is clocked out at is controlled by the baud rate generator.

For the data to change there has to be new data written, and the baud rate clock has to tick. If no new data is written to the channel, the pins will hold the last value written.

### 4.5.2 Synchronous Bit-Bang Mode

The synchronous Bit-Bang mode will only update the output parallel I/O port pins whenever data is sent from the USB interface to the parallel interface. When this is done, data is read from the USB Rx FIFO buffer and written out on the pins. Data can only be received from the parallel pins (to the USB Tx FIFO interface) when the parallel interface has been written to.

With Synchronous Bit-Bang mode, data will only be sent out by the FT4232H if there is space in the FT4232H USB TXFIFO for data to be read from the parallel interface pins. This Synchronous Bit-Bang mode will read the data bus parallel I/O pins first, before it transmits data from the USB Rx FIFO. It is therefore 1 byte behind the output, and so to read the inputs for the byte that you have just sent, another byte must be sent.

For example:-

(1) Pins start at 0xFF  
Send 0x55,0xAA  
Pins go to 0x55 and then to 0xAA  
Data read = 0xFF,0x55

(2) Pins start at 0xFF  
Send 0x55,0xAA,0xAA  
(repeat the last byte sent)  
Pins go to 0x55 and then to 0xAA

Data read = 0xFF,0x55,0xAA

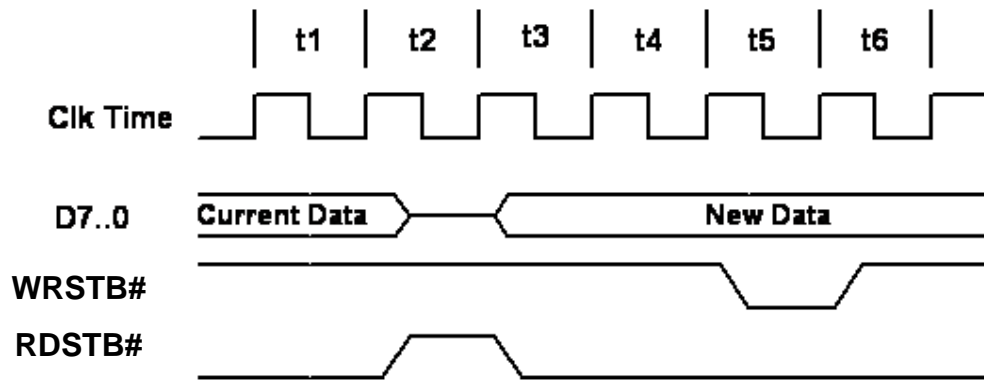
Synchronous Bit-Bang Mode differs from Asynchronous Bit-Bang mode in that the device parallel output is only read when the parallel output is written to by the USB interface. This makes it easier for the controlling program to measure the response to a USB output stimulus as the data returned to the USB interface is synchronous to the output data.

Asynchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 1 will enable Asynchronous Bit-Bang mode.

Synchronous Bit-Bang mode is enabled using Set Bit Bang Mode driver command. A hex value of 4 will enable Synchronous Bit-Bang mode.

See application note [AN2232-02, "Bit Mode Functions for the FT2232"](#) for more details and examples of using the bit-bang modes.

An example of the synchronous bi-bang mode timing is shown in Figure 4.7 and Table 4.2.



**Figure 4.7 Synchronous Bit-Bang Mode Timing Interface Example**

It should be noted that the FT4232H does not output the WRSTB# or RDSTB# signals when configured in bit-bang mode. Figure 4.7 and Table 4.2 show these signals for **illustration** purposes only.

| NAME | Description   |
|------|---|
| t1   | Current pin state is read   |
| t2   | RDSTB# is set inactive and data on the parallel I/O pins is read and sent to the USB host.        |
| t3   | RDSTB# is set active again, and any pins that are output will change to their new data            |
| t4   | 1 clock cycle to allow for data setup   |
| t5   | WRSTB# goes active. This indicates that the host PC has written new data to the I/O parallel data |
| t6   | WRSTB# goes inactive  |

**Table 4.2 Synchronous Bit-Bang Mode Timing Interface Example Timings**

WRSTB# = this output indicates when new data has been written to the I/O pins from the Host PC (via the USB interface).

RDSTB# = this output rising edge indicates when data has been read from the I/O pins and sent to the Host PC (via the USB interface).

## 4.6 FT4232H Mode Selection

The 4 channels of the FT4232H reset to 4 asynchronous serial UART interfaces. Following a reset, the required mode can be configured by sending the **FT\_SetBitMode** command (refer to [D2XX Programmers Guide](#)) to the USB driver software.

The EEPROM contents have no effect on the selected mode with the exception of selecting the TXDEN for RS485 mode when asynchronous serial interface has been selected in software. If the device is reset, then the 4 channels must be reconfigured into the required mode.

Note that the mode of each of the 4 channels is independent of the other channels.

The MPSSE can be configured directly using the D2XX commands. Refer to [D2XX Programmers Guide](#) for more details.

Also the MPSSE command set is fully described in application note [AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes](#)



## 5 Devices Characteristics and Ratings

### 5.1 Absolute Maximum Ratings

The absolute maximum ratings for the FT4232H devices are as follows. These are in accordance with the Absolute Maximum Rating System (IEC 60134). Exceeding these values may cause permanent damage to the device.

| Parameter   | Value  | Unit      |
|---|--|-----------|
| Storage Temperature   | -65°C to 150°C   | Degrees C |
| Floor Life (Out of Bag) At Factory Ambient (30°C / 60% Relative Humidity) | 168 Hours<br>(IPC/JEDEC J-STD-033A MSL Level 3 Compliant)* | Hours     |
| Ambient Operating Temperature (Power Applied)                             | -40°C to 85°C  | Degrees C |
| MTTF FT4232HL   | TBD  | hours     |
| MTTF FT4232HQ   | TBD  | hours     |
| VCORE Supply Voltage  | -0.3 to +2.0   | V         |
| VCCIO IO Voltage  | -0.3 to +4.0   | V         |
| DC Input Voltage – USBDP and USBDM  | -0.5 to +3.63  | V         |
| DC Input Voltage – High Impedance Bi-directional (powered from VCCIO)     | -0.3 to +5.8   | V         |
| DC Input Voltage – All Other Inputs                                       | -0.5 to + (VCCIO +0.5)                                     | V         |
| DC Output Current – Outputs   | 16   | mA        |

**Table 5.1 Absolute Maximum Ratings**

\* If devices are stored out of the packaging beyond this time limit the devices should be baked before use. The devices should be ramped up to a temperature of +125°C and baked for up to 17 hours.

### 5.2 DC Characteristics

DC Characteristics (Ambient Temperature = -40°C to +85°C)

| Parameter | Description                       | Minimum | Typical | Maximum | Units | Conditions                              |
|-----------|-----------------------------------|---------|---------|---------|-------|---|
| VCORE     | VCC Core Operating Supply Voltage | 1.62    | 1.80    | 1.98    | V     |   |
| VCCIO*    | VCCIO Operating Supply Voltage    | 2.97    | 3.30    | 3.63    | V     | Cells are 5V tolerant                   |
| VREGIN    | VREGIN Voltage regulator Input    | 3.00    | 3.30    | 3.60    | V     |   |
| VREGOUT   | Voltage regulator Output          | 1.71    | 1.80    | 1.89    | V     |   |
| Ireg      | Regulator Current                 |         |         | 150     | mA    | VREGIN +3.3V                            |
| Icc1      | Core Operating Supply Current     | ---     | 70      | ---     | mA    | VCORE = +1.8V<br>Normal Operation       |
| Icc1r     | Core Reset Supply Current         | ---     | 5       | ---     | mA    | VCORE = +1.8V<br>Device in reset state. |
| Icc1s     | Core Suspend Supply Current       |         | 500     |         | µA    | VCORE = +1.8V<br>USB Suspend            |

**Table 5.2 Operating Voltage and Current**

**Note:** Failure to connect all VCCIO pins will result in failure of the device.

The I/O pins are +3.3v cells, which are +5V tolerant (except the USB PHY pins).

| Parameter | Description                                      | Minimum | Typical | Maximum | Units | Conditions                                |
|-----------|--|---------|---------|---------|-------|---|
| Voh       | Output Voltage High                              | 2.40    | 3.14    |         | V     | Ioh = +/-2mA<br>I/O Drive strength* = 4mA |
|           |  |         | 3.20    |         | V     | I/O Drive strength* = 8mA                 |
|           |  |         | 3.22    |         | V     | I/O Drive strength* = 12mA                |
|           |  |         | 3.22    |         | V     | I/O Drive strength* = 16mA                |
| Vol       | Output Voltage Low                               |         | 0.18    | 0.40    | V     | Iol = +/-2mA<br>I/O Drive strength* = 4mA |
|           |  |         | 0.12    |         | V     | I/O Drive strength* = 8mA                 |
|           |  |         | 0.08    |         | V     | I/O Drive strength* = 12mA                |
|           |  |         | 0.07    |         | V     | I/O Drive strength* = 16mA                |
| Vil       | Input low Switching Threshold                    |         | -       | 0.80    | V     | LVTTTL                                    |
| Vih       | Input High Switching Threshold                   | 2.0     | -       |         | V     | LVTTTL                                    |
| Vt        | Switching Threshold                              |         | 1.50    |         | V     | LVTTTL                                    |
| Vt-       | Schmitt trigger negative going threshold voltage | 0.80    | 1.10    | -       | V     |   |
| Vt+       | Schmitt trigger positive going threshold voltage |         | 1.60    | 2.0     | V     |   |
| Rpu       | Input pull-up resistance                         | 40      | 75      | 190     | KΩ    | Vin = 0                                   |
| Rpd       | Input pull-down resistance                       | 40      | 75      | 190     | KΩ    | Vin = VCCIO                               |
| Iin       | Input Leakage Current                            | 15      | 45      | 85      | μA    | Vin = 0                                   |
| Ioz       | Tri-state output leakage current                 |         | +/-10   |         | μA    | Vin = 5.5V or 0                           |

**Table 5.3 I/O Pin Characteristics (except USB PHY pins)**

\*The I/O drive strength and slow slew-rate are configurable in the EEPROM.

DC Characteristics (Ambient Temperature = -40°C to +85°C)

| Parameter     | Description                  | Minimum | Typical | Maximum | Units | Conditions                      |
|---------------|------------------------------|---------|---------|---------|-------|---------------------------------|
| VPHY, VPLL    | PHY Operating Supply Voltage | 3.0     | 3.3     | 3.6     | V     | 3.3V I/O                        |
| Iccphy        | PHY Operating Supply Current | ---     | 30      | 60      | mA    | High-speed operation at 480 MHz |
| Iccphy (susp) | PHY Operating Supply Current | ---     | 10      | 50      | μA    | USB Suspend                     |

**Table 5.4 PHY Operating Voltage and Current**

| Parameter | Description                    | Minimum                | Typical | Maximum | Units | Conditions |
|-----------|--------------------------------|------------------------|---------|---------|-------|------------|
| Voh       | Output Voltage High            | V <sub>CORE</sub> -0.2 |         |         | V     |            |
| Vol       | Output Voltage Low             |                        |         | 0.2     | V     |            |
| Vil       | Input low Switching Threshold  |                        | -       | 0.8     | V     |            |
| Vih       | Input High Switching Threshold | 2.0                    | -       |         | V     |            |

**Table 5.5 PHY I/O Pin Characteristics**

### 5.3 ESD Tolerance

ESD protection for FT4232H IO's

| Parameter                 | Reference                           | Minimum | Typical | Maximum | Units |
|---------------------------|-------------------------------------|---------|---------|---------|-------|
| Human Body Model (HBM)    | JEDEC EIA/JESD22-A114-B, Class 2    |         | ±2kV    |         | kV    |
| Machine Mode (MM)         | JEDEC EIA/JESD22-A115-A, Class B    |         | ±200V   |         | V     |
| Charge Device Model (CDM) | JEDEC EIA/ JESD22-C101-D, Class-III |         | ±500V   |         | V     |
| Latch-up                  | JESD78, Trigger Class-II            |         | ±200mA  |         | mA    |

**Table 5.6 ESD Tolerance**

### 5.4 Thermal Characteristics

| Parameter                          | Minimum | Typical | Maximum | Units |
|------------------------------------|---------|---------|---------|-------|
| θ <sub>JA</sub> (FT4232HL)         |         | 37.66   |         | °C/W  |
| θ <sub>JC</sub> (FT4232HL)         |         | 8.39    |         | °C/W  |
| θ <sub>JA</sub> (FT4232HQ)         |         | 29.67   |         | °C/W  |
| θ <sub>JC</sub> (FT4232HQ)         |         | 14.12   |         | °C/W  |
| T <sub>J</sub> (FT4232HL/FT4232HQ) | -40     | 25      | 125     | °C    |

**Table 5.7 Thermal Characteristics**

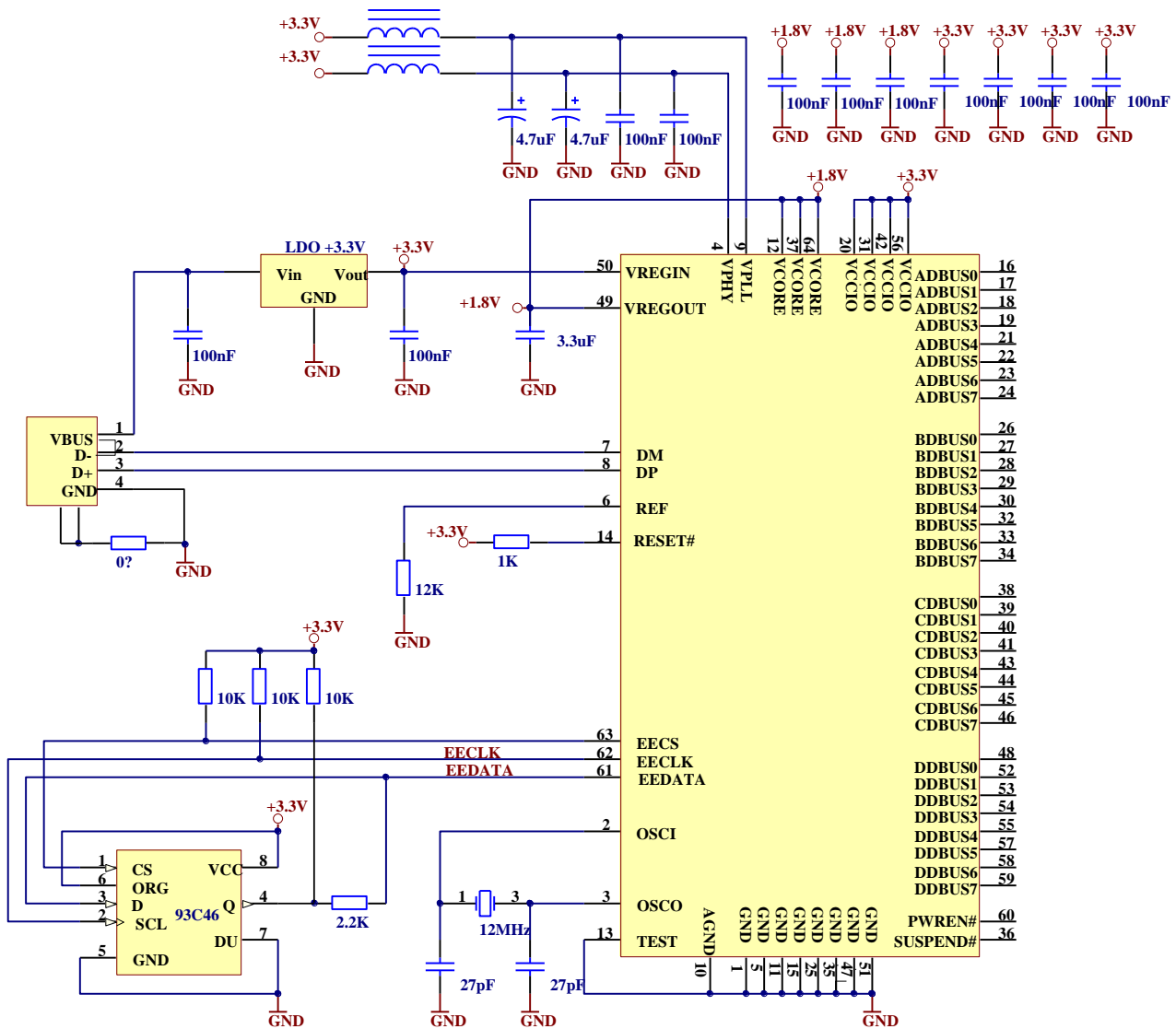
## 6 FT4232H Configurations

The following sections illustrate possible USB power configurations for the FT4232H.

All USB power configurations illustrated apply to both package options for the FT4232H device.

### 6.1 USB Bus Powered Configuration

Bus Powered Application example 1: Bus powered configuration

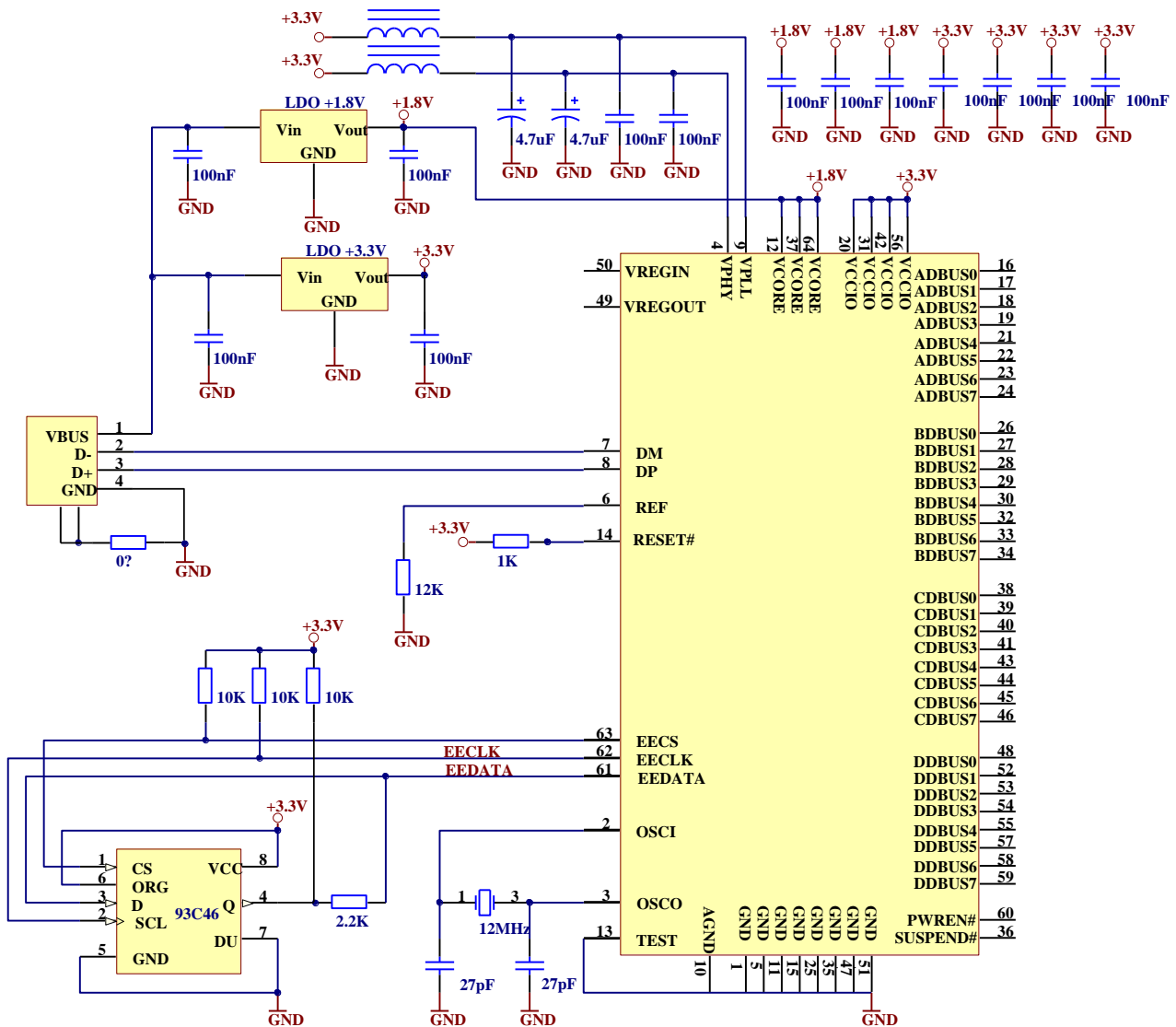


**Figure 6.1 Bus Powered Configuration Example 1**

Figure 6.1 illustrates the FT4232H in a typical USB bus powered design configuration. A USB bus powered device gets its power from the USB bus. In this application, the FT4232H requires that the VBUS (USB +5V) is regulated down to +3.3V (using an LDO) to supply the VCCIO, VPLL, VPHY and VREGIN.

VREGIN is the +3.3V input to the on chip +1.8V regulator. The output of the on chip LDO regulator (+1.8V) drives the FT4232H core supply (VCORE). This requires a minimum of a 3.3uF filter capacitor.

Bus Powered Application example 2: Bus powered configuration (with additional 1.8V LDO voltage regulator for VCORE).

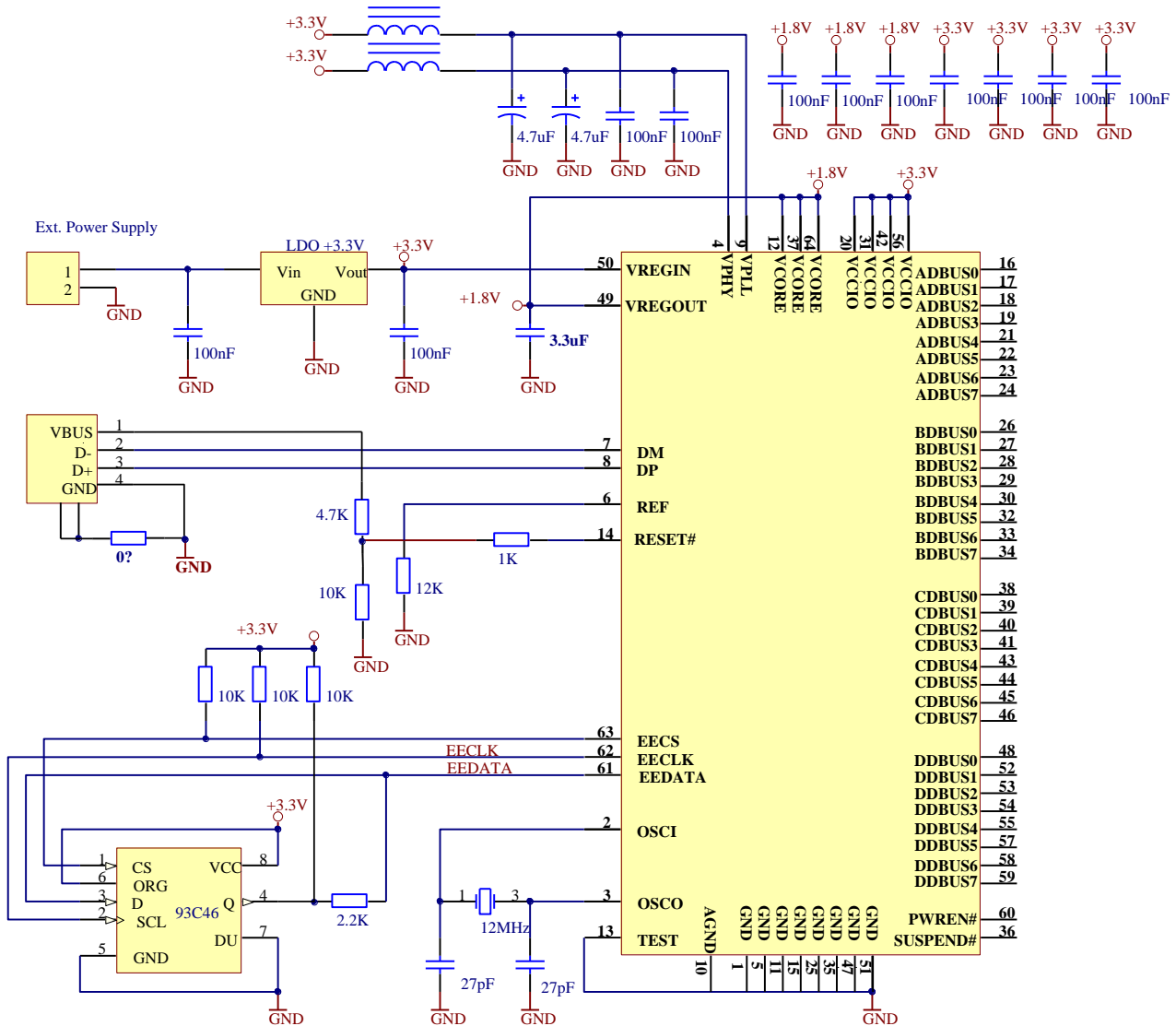


**Figure 6.2 Bus Powered Configuration Example 2**

Figure 6.2 illustrate the FT4232H in a typical USB bus powered configuration similar to Figure 6.1. The difference here is that the +1.8V for the FT4232H core (VCORE) has been regulated from the VBUS as well as the +3.3V supply to the VPLL, VPHY, VCCIO and VREGIN.

## 6.2 USB Self Powered Configuration

Self-Powered application example 1: Self-powered configuration

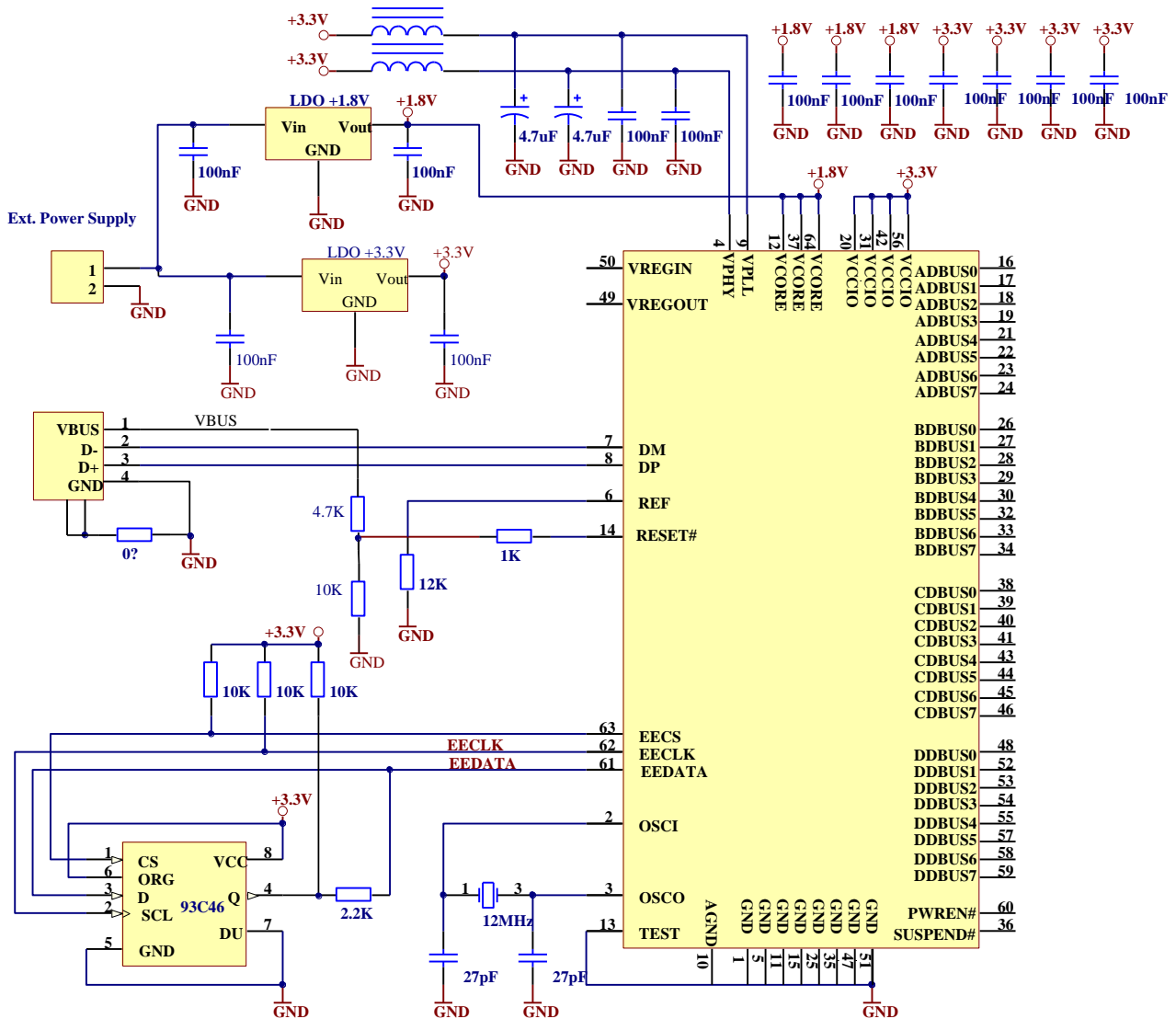


**Figure 6.3 Self-Powered Configuration Example 1**

Figure 6.3 illustrate the FT4232H in a typical USB self-powered configuration. A USB self-powered device gets its power from its own power supply and does not draw current from the USB bus. In this example an external power supply is used. This external supply is regulated to +3.3V.

Note that in this set-up, the EEPROM should be configured for self-powered operation.

Self-Powered application example 2: Self-powered configuration (with additional 1.8V LDO voltage regulator for VCORE).

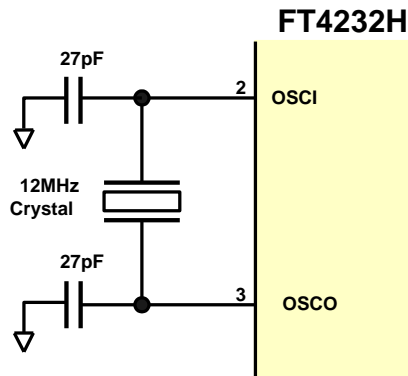


**Figure 6.4 Self-Powered Configuration Example 2**

Figure 6.4 illustrates the FT4232H in a typical USB self-powered configuration similar to Figure 6.3. The difference here is that the +1.8V for the FT4232H core has been regulated from the external power supply.

Note that in this set-up, the EEPROM should be configured for self-powered operation.

### 6.3 Oscillator Configuration



**Figure 6.5 Recommended FT4232H Crystal Oscillator Configuration.**

Figure 6.5 Illustrates how to connect the FT4232H with a 12MHz  $\pm$  0.003% crystal. In this case loading capacitors should be added between OSCI, OSCO and GND as shown. A value of 27pF is shown as the capacitor in the example – this will be good for many crystals but it is recommended to select the loading capacitor value based on the manufacturer’s recommendations wherever possible. It is recommended to use a parallel cut type crystal.

It is also possible to use a 12 MHz oscillator with the FT4232H. In this case the output of the oscillator would drive OSCI, and OSCO should be left unconnected. The oscillator must have a CMOS output drive capability.

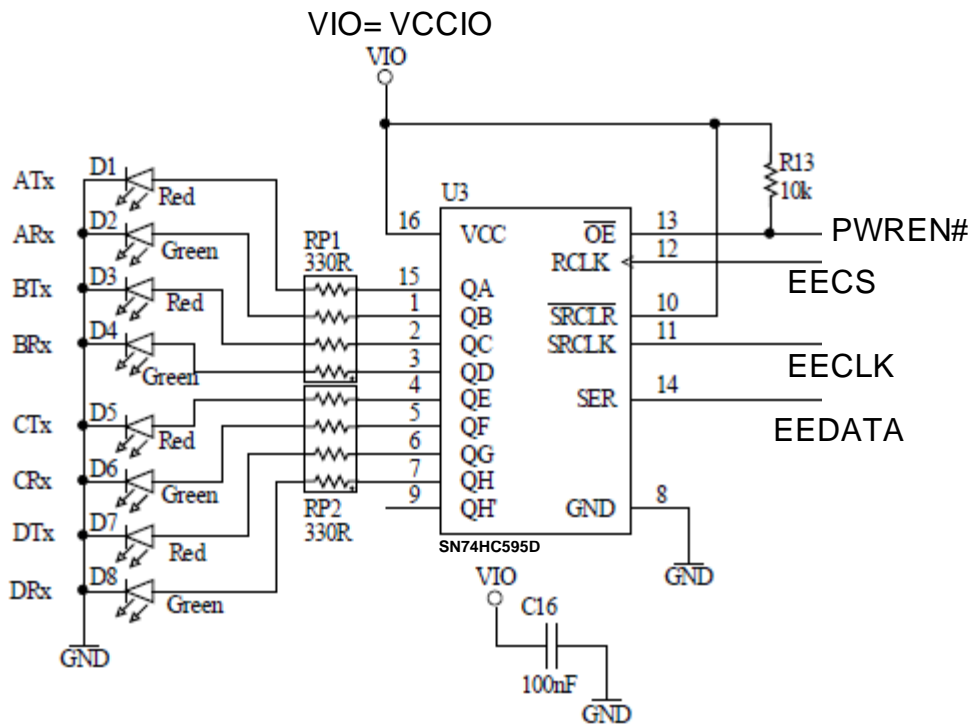
| Parameter | Description           | Minimum | Typical | Maximum | Units | Conditions |
|-----------|-----------------------|---------|---------|---------|-------|------------|
| OSCI Vin  | Input Voltage         | 2.97    | 3.30    | 3.63    | V     |            |
| FIn       | Input Frequency       |         | 12      |         | MHz   | +/- 30ppm  |
| Ji        | Cycle to cycle jitter |         | < 150   |         | pS    |            |

**Table 6.1 OSCI Input characteristics**



## 6.4 4 Channel Transmit and Receiver LED Indication Example

The following example illustrates how a 74HCT595 can be used to decode the EEDATA data to indicate Tx and Rx on each of the channels. The associated LED will light when the Channel is transmitting or receiving data.



**Figure 6.6 Using 74HC595 to Indicate Tx and Rx Data**

In this configuration, the LEDs will flash when the EEPROM is accessed e.g. during enumeration.

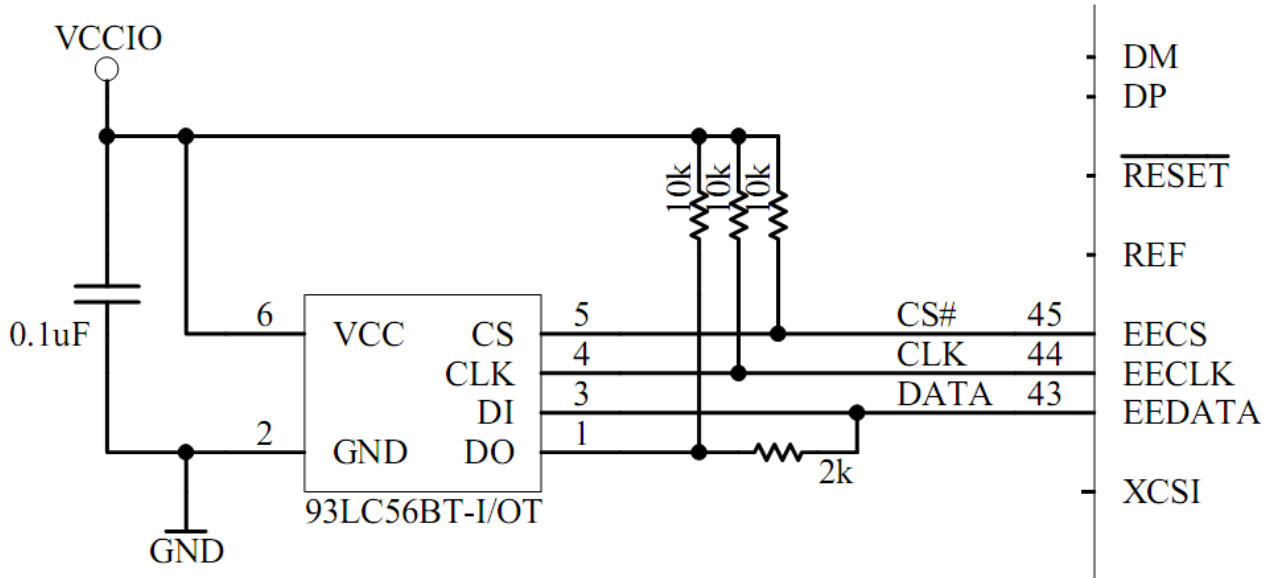
Under normal operation, the EECS is held low to disable access to the EEPROM. In this special case, the EECCLK (frequency = 1.56 $\mu$ S) will clock the EEDATA into the 74HC595 shift register (with EECCLK low, therefore EEPROM ignores the EEDATA). Then EECCLK will pulse high. The rising edge of the EECCLK latches the data into a storage register of the 74HC595 which drives the LEDs.

Please refer to the [74HC595 datasheet](#) for further explanation.

## 7 EEPROM Configuration

If an external EEPROM is fitted (93LC46/56/66) it can be programmed over USB using [FT\\_PROG](#). The EEPROM must be 16 bits wide and capable of working at a VCC supply of +3.0 to +3.6 volts.

Adding an external EEPROM allows selecting the TXDEN for RS485 mode when asynchronous serial interface has been selected.



**Figure 7.1 EEPROM Interface**

The external EEPROM can also be used to customise the USB VID, PID, Serial Number, Product Description Strings and Power Descriptor value of the FT4232H for OEM applications. Other parameters controlled by the EEPROM include Remote Wake Up, Soft Pull Down on Power-Off and I/O pin drive strength.

If no EEPROM is connected (or the EEPROM is blank), the FT4232H uses its built-in default VID (0403), PID (6011) Product Description and Power Descriptor Value. In this case, the device will not have a serial number as part of the USB descriptor.

### 7.1 Default EEPROM Configuration

The external EEPROM (if it's fitted) can be programmed over USB using [FT\\_PROG](#). This allows a blank part to be soldered onto the PCB and programmed as part of the manufacturing and test process. Users who do not have their own USB Vendor ID but who would like to use a unique Product ID in their design can apply to FTDI for a free block of unique PIDs.

See TN\_100 [USB Vendor ID/Product ID Guidelines](#) for more information.

| Parameter                         | Value         | Notes  |
|-----------------------------------|---------------|--|
| USB Vendor ID (VID)               | 0403h         | FTDI default VID (hex)   |
| USB Product UD (PID)              | 6011h         | FTDI default PID (hex)   |
| bcd Device                        | 0800h         |  |
| Serial Number Enabled?            | Yes           |  |
| Serial Number                     | None          |  |
| Pull down I/O Pins in USB Suspend | Disabled      | Enabling this option will make the device pull down on the UART interface lines when in USB suspend mode (PWREN# is high). |
| Manufacturer Name                 | FTDI          |  |
| Product Description               | Quad RS232-HS |  |
| Max Bus Power Current             | 500mA         |  |

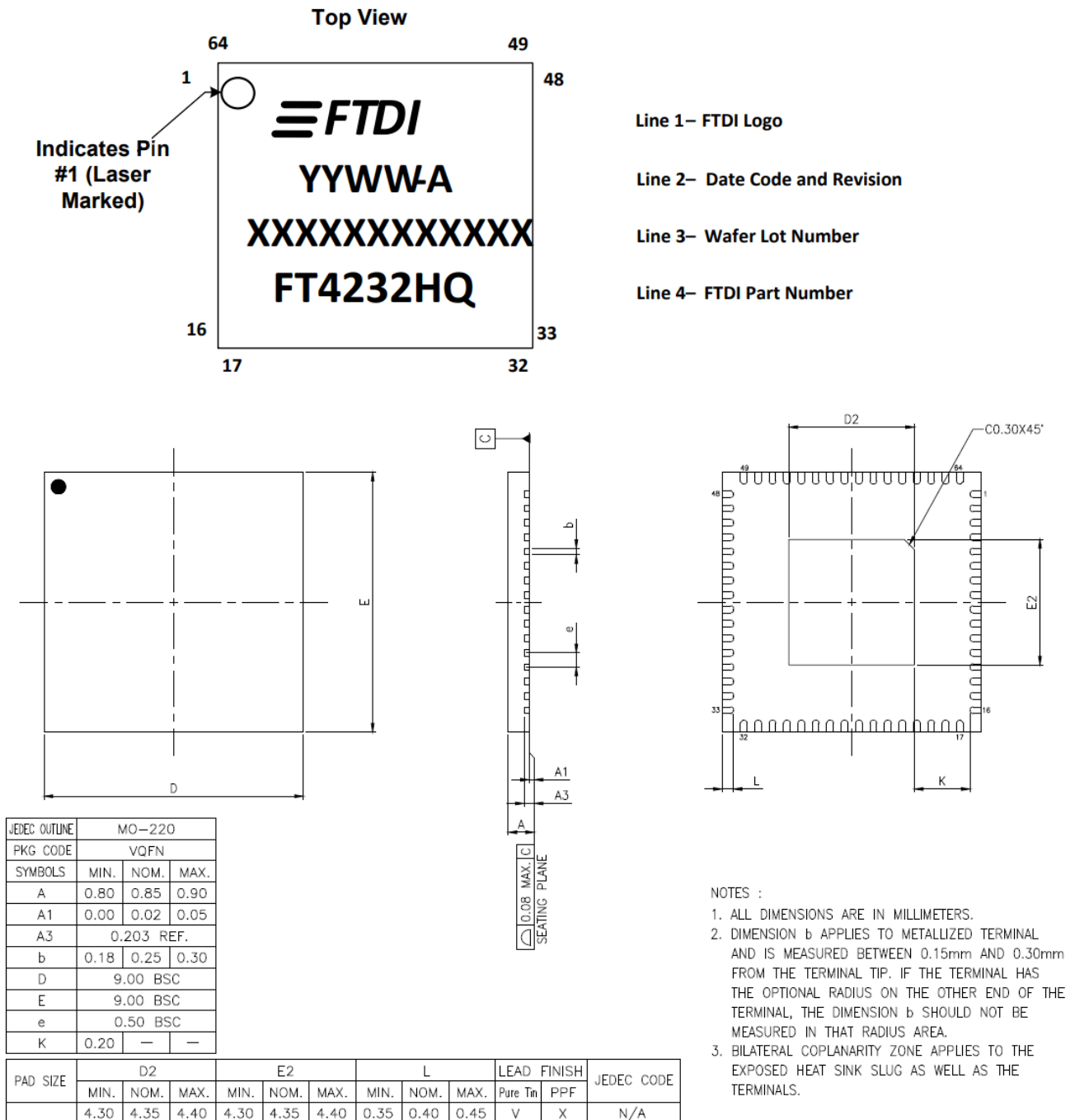
| Parameter         | Value       | Notes  |
|-------------------|-------------|--|
| Power Source      | Bus Powered |  |
| Device Type       | FT4232H     |  |
| USB Version       | 0200h       | Returns USB 2.0 device description to the host.  |
| Remote Wake Up    | Disabled    | Taking RI# low will wake up the USB host controller from suspend in approximately 20 ms. If enabled. |
| RI RS485          | Disabled    | Enables TXDEN signal for RS485 buses.  |
| High Current I/Os | Disabled    | Enables the high drive level on the UART and ACBUS I/O pins.   |
| Load VCP Driver   | Enabled     | Makes the device load the VCP driver interface for the device.                                       |

**Table 7.1 Default Configuration with a blank/no EEPROM**

## 8 Package Parameters

The FT4232H is available in three different packages. The FT4232HL is the LQFP-64 option, the FT4232HQ is the QFN-64 package option and the FT4232H-56Q is the VQFN-56 package option. The solder reflow profile for all packages is described in **Section 8.4**. See TN\_166 [FTDI Example IC Footprints](#) for PCB footprint guidelines.

### 8.1 FT4232HQ, QFN-64 Package Dimensions

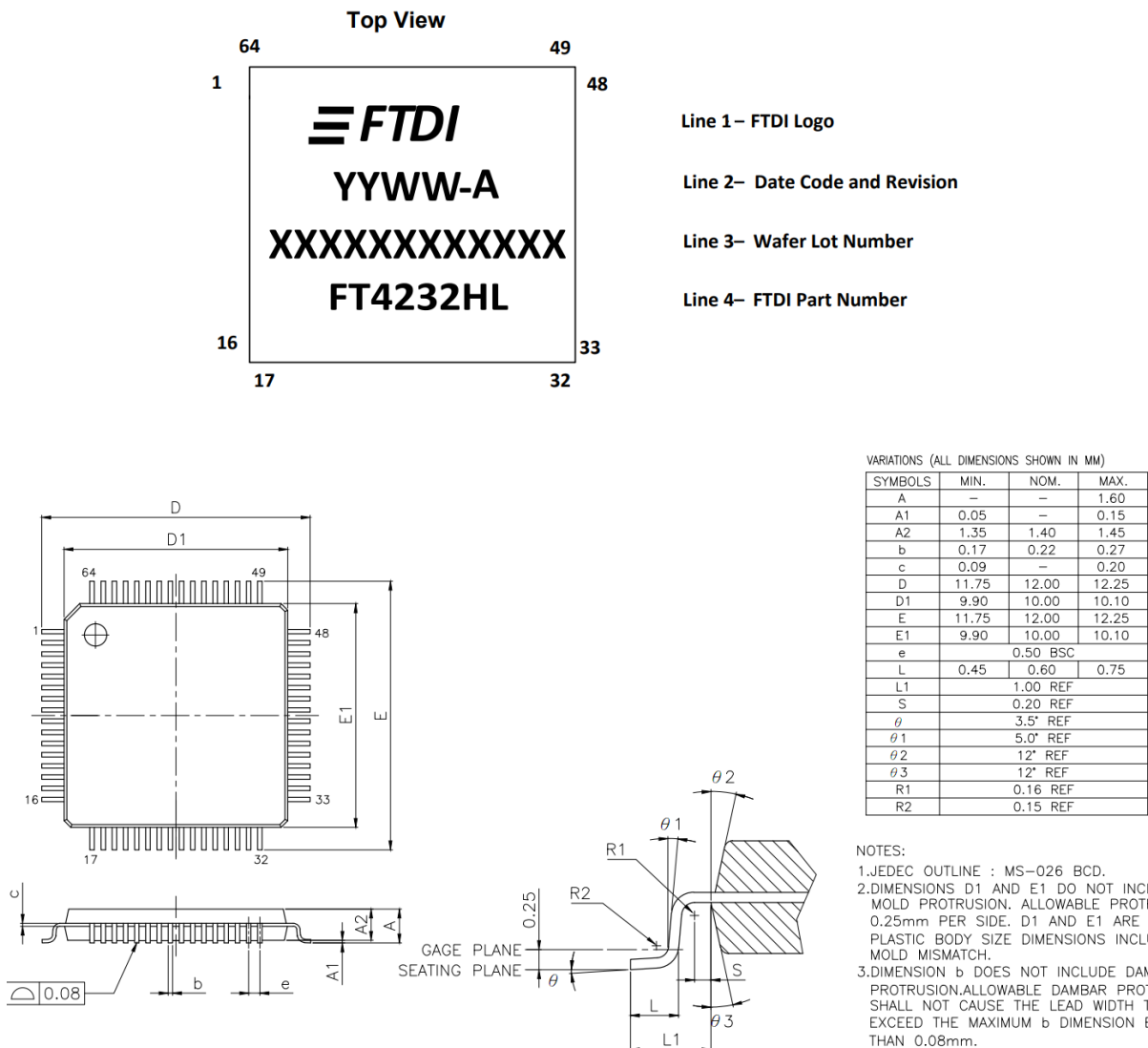


**Figure 8.1 64 pin QFN Package Details**

**Notes:**

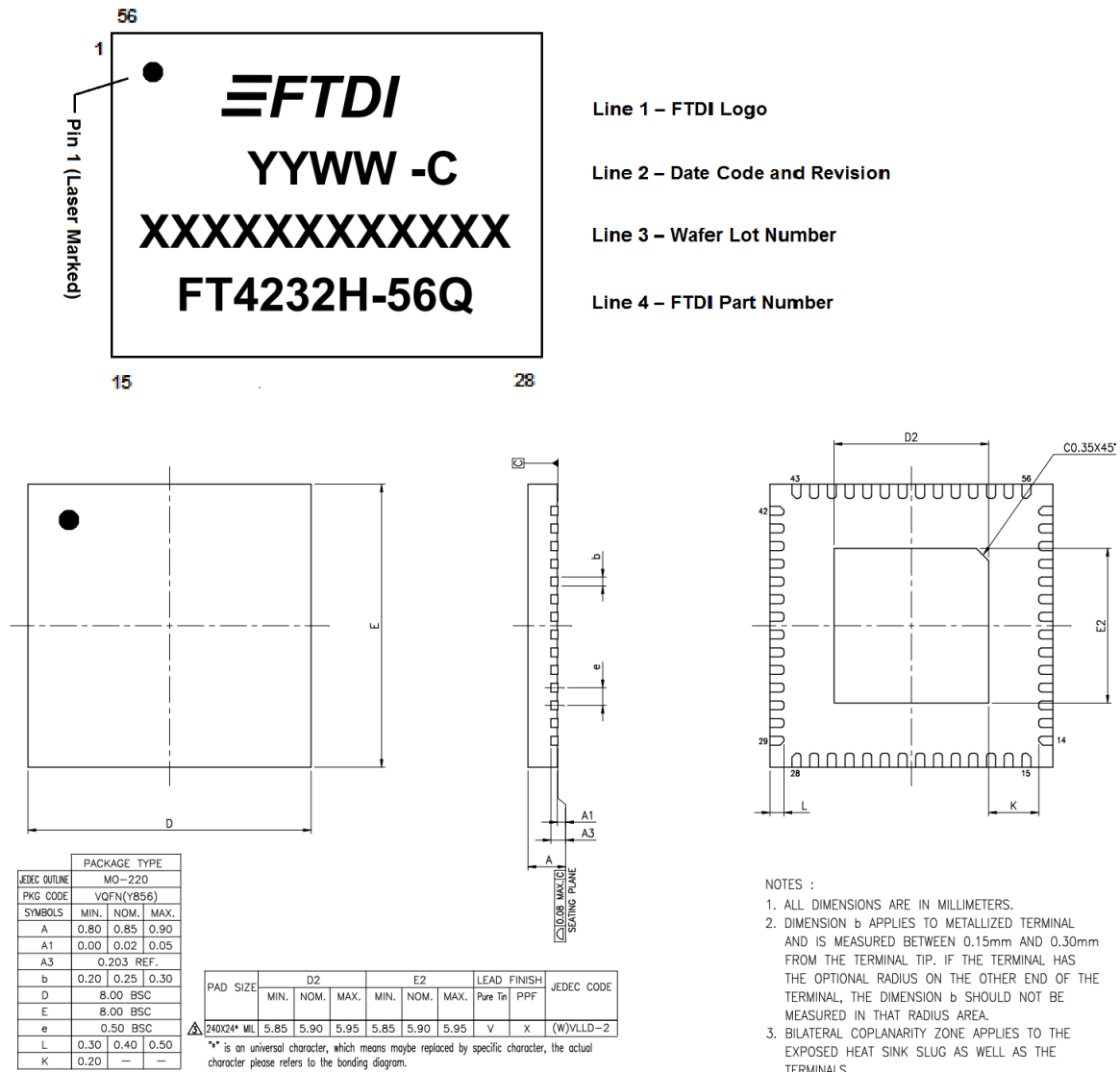
- All dimensions are in mm.
- The bottom side central solder pad must be connected to the ground of the system.

## 8.2 FT4232HL, LQFP-64 Package Dimensions



**Figure 8.2 64 pin LQFP Package Details**

### 8.3 FT4232H-56Q, VQFN-56 Package Dimensions

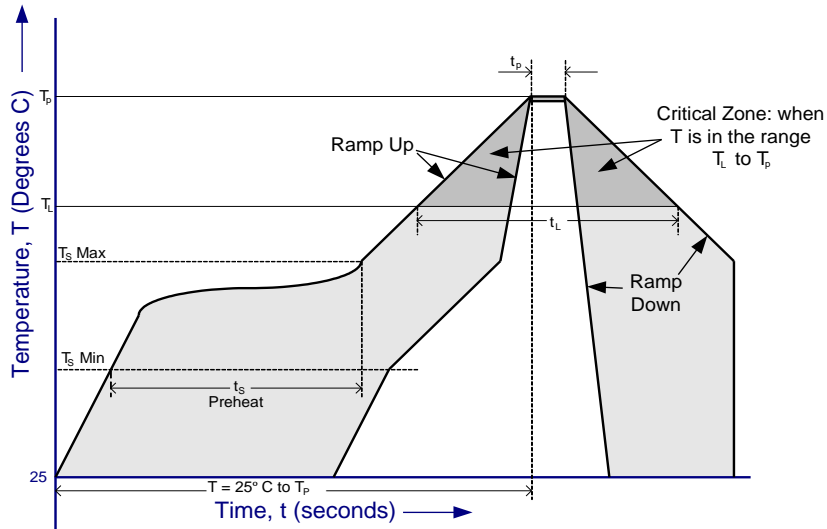


**Figure 8.3 56-pin VQFN Package Details for FT4232H-56Q**

**Notes:**

- The internal ground of the device is connected to the bottom side central solder pad whose dimension is 5.90 x 5.90mm. This central solder pad must be connected to the ground of the system.

## 8.4 Solder Reflow Profile



**Figure 8.4 FT4232H Solder Reflow Profile**

| Profile Feature   | Pb Free Solder Process (green material) | SnPb Eutectic and Pb free (non green material) Solder Process |
|---|---|---|
| Average Ramp Up Rate ( $T_s$ to $T_p$ )   | 3°C / second Max.                       | 3°C / Second Max.   |
| Preheat<br>- Temperature Min ( $T_s$ Min.)<br>- Temperature Max ( $T_s$ Max.)<br>- Time ( $t_s$ Min to $t_s$ Max) | 150°C<br>200°C<br>60 to 120 seconds     | 100°C<br>150°C<br>60 to 120 seconds                           |
| Time Maintained Above Critical Temperature $T_L$ :<br>- Temperature ( $T_L$ )<br>- Time ( $t_L$ )                 | 217°C<br>60 to 150 seconds              | 183°C<br>60 to 150 seconds                                    |
| Peak Temperature ( $T_p$ )  | 260°C                                   | see Table 8.2   |
| Time within 5°C of actual Peak Temperature ( $t_p$ )  | 30 to 40 seconds                        | 20 to 40 seconds  |
| Ramp Down Rate  | 6°C / second Max.                       | 6°C / second Max.   |
| Time for $T = 25^\circ\text{C}$ to Peak Temperature, $T_p$  | 8 minutes Max.                          | 6 minutes Max.  |

**Table 8.1 Reflow Profile Parameter Values**

| SnPb Eutectic and Pb free (non green material)    |                              |                              |
|---|------------------------------|------------------------------|
| Package Thickness                                 | Volume mm <sup>3</sup> < 350 | Volume mm <sup>3</sup> ≥ 350 |
| < 2.5 mm  | 235 +5/-0 deg C              | 220 +5/-0 deg C              |
| ≥ 2.5 mm  | 220 +5/-0 deg C              | 220 +5/-0 deg C              |
| <b>Pb Free (green material) = 260 +5/-0 deg C</b> |                              |                              |

**Table 8.2 Package Reflow Peak Temperature**

## 9 Contact Information

### Head Office – Glasgow, UK

Future Technology Devices International Limited  
Unit 1, 2 Seaward Place, Centurion Business Park  
Glasgow G41 1HH  
United Kingdom  
Tel: +44 (0) 141 429 2777  
Fax: +44 (0) 141 429 2758

E-mail (Sales) [sales1@ftdichip.com](mailto:sales1@ftdichip.com)  
E-mail (Support) [support1@ftdichip.com](mailto:support1@ftdichip.com)  
E-mail (General Enquiries) [admin1@ftdichip.com](mailto:admin1@ftdichip.com)

### Branch Office – Tigard, Oregon, USA

Future Technology Devices International Limited (USA)  
7130 SW Fir Loop  
Tigard, OR 97223-8160  
USA  
Tel: +1 (503) 547 0988  
Fax: +1 (503) 547 0987

E-mail (Sales) [us.sales@ftdichip.com](mailto:us.sales@ftdichip.com)  
E-mail (Support) [us.support@ftdichip.com](mailto:us.support@ftdichip.com)  
E-mail (General Enquiries) [us.admin@ftdichip.com](mailto:us.admin@ftdichip.com)

### Branch Office – Taipei, Taiwan

Future Technology Devices International Limited (Taiwan)  
2F, No. 516, Sec. 1, NeiHu Road  
Taipei 114  
Taiwan, R.O.C.  
Tel: +886 (0) 2 8797 1330  
Fax: +886 (0) 2 8751 9737

E-mail (Sales) [tw.sales1@ftdichip.com](mailto:tw.sales1@ftdichip.com)  
E-mail (Support) [tw.support1@ftdichip.com](mailto:tw.support1@ftdichip.com)  
E-mail (General Enquiries) [tw.admin1@ftdichip.com](mailto:tw.admin1@ftdichip.com)

### Branch Office – Shanghai, China

Future Technology Devices International Limited (China)  
Room 1103, No. 666 West Huaihai Road,  
Shanghai, 200052  
China  
Tel: +86 21 62351596  
Fax: +86 21 62351595

E-mail (Sales) [cn.sales@ftdichip.com](mailto:cn.sales@ftdichip.com)  
E-mail (Support) [cn.support@ftdichip.com](mailto:cn.support@ftdichip.com)  
E-mail (General Enquiries) [cn.admin@ftdichip.com](mailto:cn.admin@ftdichip.com)

### Web Site

<http://ftdichip.com>

### Distributor and Sales Representatives

Please visit the Sales Network page of the [FTDI Web site](#) for the contact details of our distributor(s) and sales representative(s) in your country.

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## Appendix A – References

### Document References

[AN\\_113, "Interfacing FT2232H Hi-Speed Devices To I2C Bus](#)

[AN\\_109 – "Programming Guide for High Speed FT232RL DLL"](#)

[AN\\_110 – "Programming Guide for High Speed FT232RL DLL"](#)

[AN\\_111 – "Programming Guide for High Speed FT232RL DLL"](#)

[AN\\_113 – "Interfacing FT2232H Hi-Speed Devices To I2C Bus](#)

[AN114 – "Interfacing FT2232H Hi-Speed Devices To SPI Bus](#)

[AN135 – MPSSE Basics](#)

[AN108 - Command Processor For MPSSE and MCU Host Bus Emulation Modes](#)

[TN\\_104, "Guide to Debugging Customers Failed Driver Installation](#)

[TN\\_100 USB Vendor ID/Product ID Guidelines](#)

[TN\\_166 FTDI Example IC Footprints](#)

[AN2232-02, "Bit Mode Functions for the FT2232](#)

[74HC595 datasheet](#)

[FT\\_PROG](#) EEPROM Programming Utility

### Acronyms and Abbreviations

| Terms            | Description   |
|------------------|---|
| CDM              | Charge Device Model                                 |
| CMOS             | Complementary Metal Oxide Semiconductor             |
| ESD              | Electrostatic Discharge                             |
| EHCI             | Extensible Host Controller Interface                |
| EEPROM           | Electrically Erasable Programmable Read-Only Memory |
| FIFO             | First In First Out                                  |
| FPGA             | Field-Programmable Gate Array                       |
| HBM              | Human Body Model                                    |
| IC               | Integrated Circuit                                  |
| I <sup>2</sup> C | Inter Integrated Circuit                            |
| JTAG             | Joint Test Action Group                             |
| LDO              | Low Drop Out  |
| LED              | Light Emitting Diode                                |

|       |   |
|-------|---|
| LQFP  | Low profile Quad Flat Package               |
| MM    | Machine Mode                                |
| MCU   | Microcontroller Unit                        |
| MPSSE | Multi-Protocol Synchronous Serial Engine    |
| OHCI  | Open Host Controller Interface              |
| PLD   | Programmable Logic Device                   |
| QFN   | Quad Flat No-Lead                           |
| SPI   | Serial Peripheral Interface                 |
| USB   | Universal Serial Bus                        |
| UART  | Universal Asynchronous Receiver/Transmitter |
| UHCI  | Universal Host Controller Interface         |
| UTMI  | Universal Transceiver Macrocell Interface   |
| VCP   | Virtual COM Ports                           |
| VQFN  | Very Thin Quad Flat Non-Leaded Package      |

## Appendix B - List of Figures and Tables

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## Appendix C - Revision History

Document Title: FT4232H QUAD HIGH SPEED USB TO MULTIPURPOSE UART/MPSSE IC Datasheet  
 Document Reference No.: FT\_000060  
 Clearance No.: FTDI#78  
 Product Page: <http://www.ftdichip.com/FTProducts.htm>  
 Document Feedback: [Send Feedback](#)

| Revision | Changes   | Date       |
|----------|---|------------|
| 1.0      | Initial Release   | 2008-11-04 |
| 2.0      | Revised Release   | 2009-01-05 |
| 2.01     | Updated description for bit-bang mode   | 2009-02-05 |
| 2.02     | Corrected QFN Tray Numbers from 160 to 260 per tray   | 2009-03-10 |
| 2.03     | Corrected signal names in Fig2.1; Added reference to AN_109, AN_110, AN_111 & AN_113; Corrected default of RI#/TXDEN in Table 3.1   | 2009-05-19 |
| 2.04     | Added latency timer description to Section 4.1  | 2009-06-03 |
| 2.05     | Corrected Figures 6.2, 6.3 and 6.4 – missing regulators and better way of holding self-powered designs in reset if not connected to USB; Corrected Max DC inputs on “DC Input Voltage – “All Other Inputs” pins from VCORE+0.5V to VCCIO+0.5V           | 2009-09-21 |
| 2.06     | Added description for MPSSE Adaptive Clocking (Section 4.4.1); Corrected 12MHz crystal specification  | 2009-10-21 |
| 2.07     | Corrected Section 4.2 – EEPROM description  | 2009-12-18 |
| 2.08     | Added TID number (Section 1.3); Added ESD specifications  | 2010-05-24 |
| 2.09     | Added USB certified Logo in Section 1.3; Clarified unsupported baud rates of 7,9,10 and 11 Mbaud; Added clarifications about Wake up in Section 3.4.1; Replaced 74HCT595 with 74HC595 in Section 6.4; Edited Fig 4.1 (removed TXLED & RXLED references) | 2010-09-02 |
| 2.10     | Edited Section 4.3.2, 4.3.3 / Fig 4.2 & 4.3   | 2010-11-17 |
| 2.11     | Updated Installation guide/App Notes & Technical Notes links  | 2012-01-09 |
| 2.2      | Updated Fig 4.1; Added feedback links   | 2012-02-11 |
| 2.3      | Updated information for new package 56-pin VQFN   | 2016-04-04 |
| 2.4      | Added section Default EEPROM Configuration  | 2016-06-03 |
| 2.5      | Added section 5.4 Thermal Characteristics based on customer enquiry. Taken from FT2232H Datasheet. These characteristics are the same for each device. No information on FT4232H-56Q.   | 2017-11-07 |
| 2.6      | Updated the following pictures – Figure 8.1, 8.2 and 8.3;<br>Removed table 8.1 (as is now part of the figure);<br>Updated the notes under fig.8.1; Updated the notes under fig.8.3  | 2019-05-27 |