VN5E010AFH-E

10 mΩ high-side driver with analog current sense for automotive applications

Features

Max supply voltage	V_{CC}	41 V
Operating voltage range	V_{CC}	4.5 V to 28 V
Typ. ON-state resistance	R_{ON}	10 mΩ
Current limitation (typ)	I_{LIMH}	85 A
OFF-state supply current	I_S	2 µA(1)

1. Typical value with all loads connected

- General
  - Very low standby current
  - 3 V CMOS compatible inputs
  - Optimized electromagnetic emissions
  - Very low electromagnetic susceptibility
  - Compliance with European directive 2002/95/EC
  - Very low current sense leakage
- Diagnostic functions
  - Proportional load current sense
  - High current sense precision for wide current range
  - Current sense disable
  - OFF-state open-load detection
  - Output short to V_{CC} detection
  - Overload and short to ground (power limitation) indication
  - Thermal shutdown indication
- Protection
  - Undervoltage shutdown
  - Overvoltage clamp
  - Load current limitation
  - Self limiting of fast thermal transients
  - Protection against loss of ground and loss of V_{CC}
  - Overtemperature shutdown with autorestart (thermal shutdown)
  - Inrush current active management by power limitation

  - Reverse battery protection with self switch on of the Power MOSFET
  - Electrostatic discharge protection

Applications

- All types of resistive, inductive and capacitive loads
- Suitable as LED driver

Description

The VN5E010AFH-E is a single-channel high-side driver manufactured using ST proprietary VIPower™ M0-5 technology and housed in HPAK package. The device is designed to drive 12 V automotive grounded loads, and to provide protection and diagnostics. It also implements a 3 V and 5 V CMOS compatible interface for use with any microcontroller.

The device integrates advanced protective functions such as load current limitation, inrush and overload active management by power limitation, overtemperature shut-off with auto-restart and overvoltage active clamp. A dedicated analog current sense pin is associated with every output channel providing ehnanced diagnostic functions including fast detection of overload and short-circuit to ground through power limitation indication, overtemperature indication, short-circuit to V_{CC} diagnosis and ON-state and OFF-state open-load detection.

The current sensing and diagnostic feedback of the whole device can be disabled by pulling the CS_DIS pin high to share the external sense resistor with similar devices.

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1 Block diagram and pin configuration

Figure 1. Block diagram

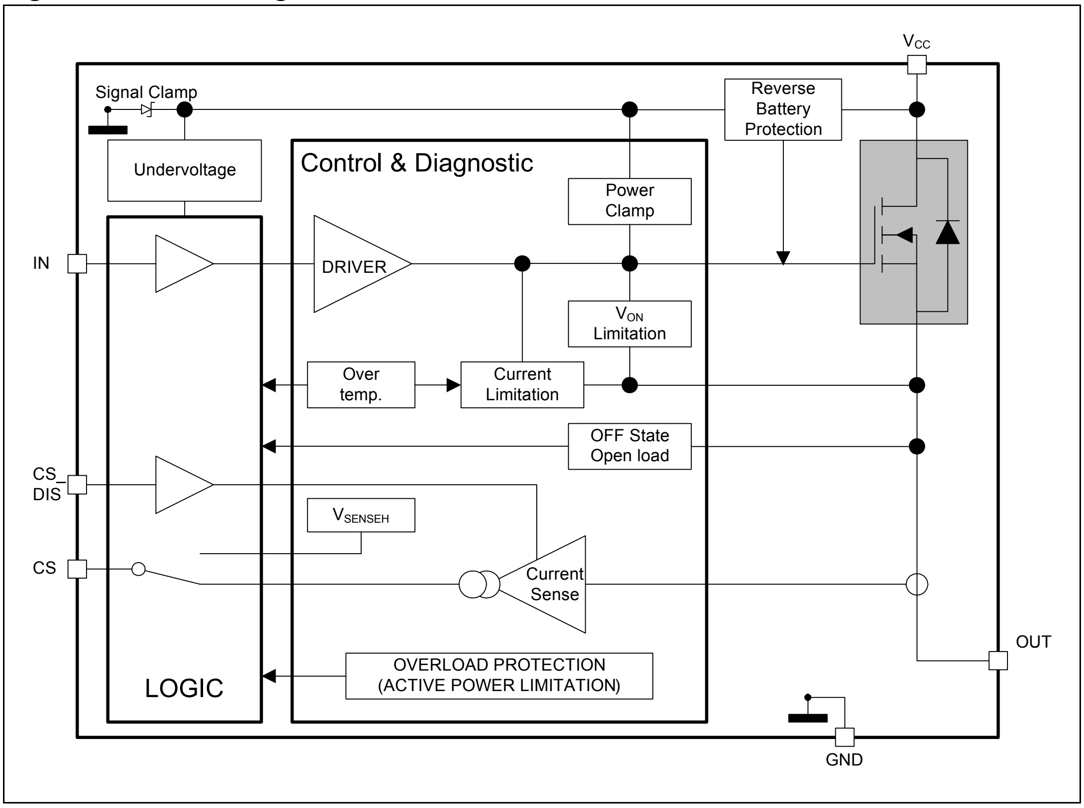


Table 1. Pin functions

Name	Function
V_{CC}	Battery connection
OUT	Power output (1)
GND	Ground connection
IN	Voltage controlled input pin with hysteresis, CMOS compatible. Controls output switch state
CS	Analog CS pin, delivers a current proportional to the load current
CS_DIS	Active high CMOS compatible pin, to disable the CS pin

1. Pins 1 and 7 must be externally tied together.

Figure 2. Configuration diagram (top view) not in scale

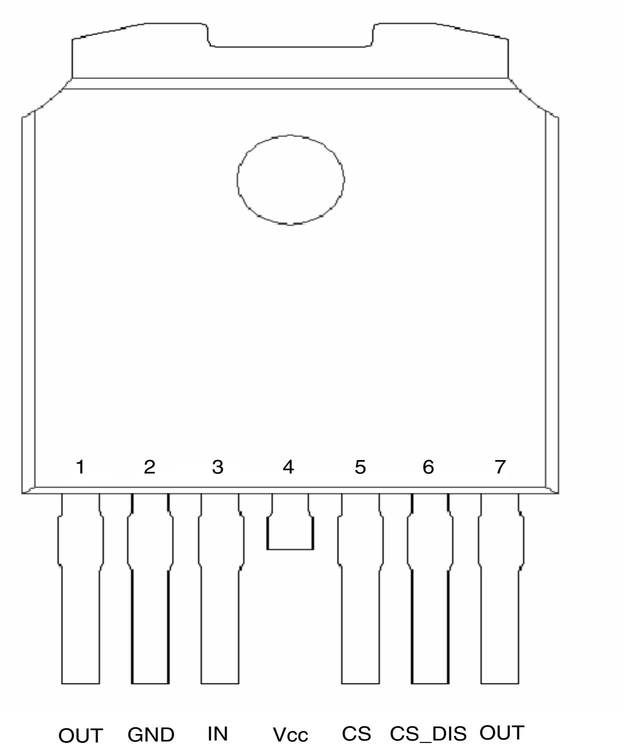
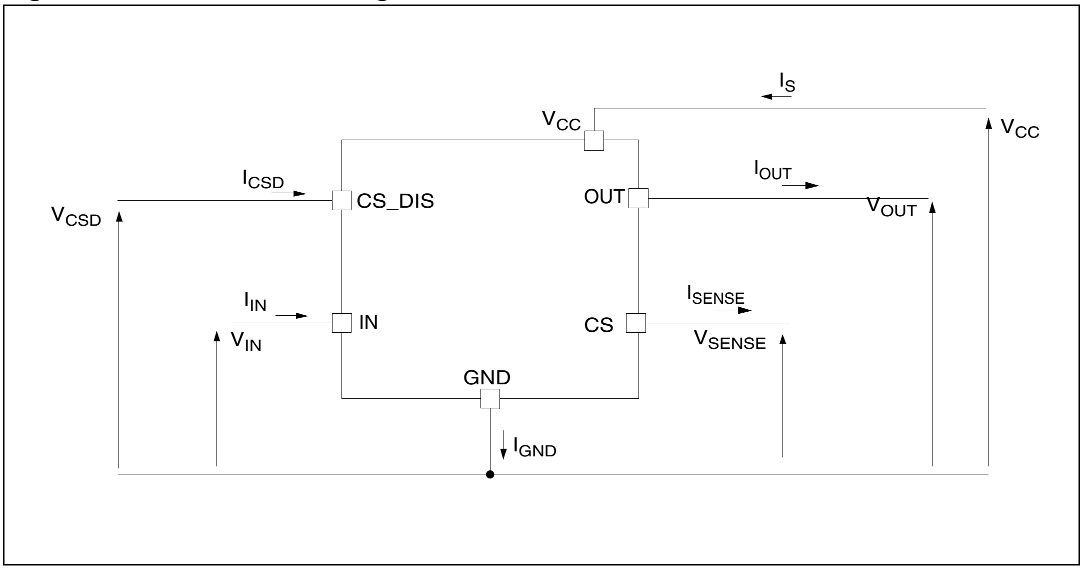


Table 2. Suggested connections for unused and not connected pins

Connection / pin	CS	OUT	IN	CS_DIS
Floating	Not allowed	X	X	X
To ground	Through 1 kΩ resistor	Through 22 kΩ resistor	Through 10 kΩ resistor	Through 10 kΩ resistor

2 Electrical specifications

Figure 3. Current and voltage conventions



2.1 Absolute maximum ratings

Stressing the device above the rating listed in the *Table 3: Absolute maximum ratings* may cause permanent damage to the device . These are stress ratings only and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE program and other relevant quality document.

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
V_{CC}	DC supply voltage	41	V
$-V_{CC}$	Reverse DC supply voltage	16	V
I_{OUT}	DC output current	Internally limited	A
$-I_{OUT}$	Reverse DC output current	20	A
I_{IN}	DC input current	-1 to 10	mA
I_{CSD}	DC current sense disable input current	-1 to 10	mA
V_{CSENSE}	Current sense maximum voltage ($V_{CC} > 0$)	V_{CC} - 41 $+V_{CC}$	V V
E_{MAX}	Maximum switching energy (single pulse) ($L = 2.2$ mH; $R_L = 0\ \Omega$; $V_{BAT} = 13.5$ V; $T_{jstart} = 150$ °C; $I_{OUT} = I_{limL}$ *(Typ.)*)	645	mJ

Table 3. Absolute maximum ratings (continued)

Symbol	Parameter	Value	Unit
V_{ESD}	Electrostatic discharge (human body model: R = 1.5 kΩ; C = 100 pF) – IN – CS – CS_DIS – OUT – V_{CC}	 4000 2000 4000 5000 5000	 V V V V V
V_{ESD}	Charge device model (CDM-AEC-Q100-011)	750	V
T_j	Junction operating temperature	-40 to 150	°C
T_{stg}	Storage temperature	-55 to 150	°C

2.2 Thermal data

Table 4. Thermal data

Symbol	Parameter	Max. value	Unit
$R_{thj-case}$	Thermal resistance junction-case	0.55	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient	67.7	°C/W

2.3 Electrical characteristics

Values specified in this section are for 8 V < V_{CC} < 28 V, -40 °C < T_j < 150 °C, unless otherwise specified.

Table 5. Power section

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{CC}	Operating supply voltage		4.5	13	28	V
V_{USD}	Undervoltage shutdown			3.5	4.5	V
$V_{USDhyst}$	Undervoltage shutdown hysteresis			0.5		V
R_{ON}	ON-state resistance	I_{OUT} = 6 A; T_j = 25 °C		10		mΩ
		I_{OUT} = 6 A; T_j = 150 °C			20	
		I_{OUT} = 6 A; V_{CC} = 5 V; T_j = 25 °C			13	
R_{ON-Rev}	R_{DSON} in reverse battery condition	V_{CC} = -13 V; I_{OUT} = -6 A; T_j = 25 °C		10		mΩ
V_{clamp}	Clamp voltage	I_{CC} = 20 mA; I_{OUT} = 0 A	41	46	52	V
I_S	Supply current	OFF-state: V_{CC} = 13 V; T_j = 25 °C; V_{IN} = V_{OUT} = V_{SENSE} = 0 V		2	5	µA
		ON-state: V_{CC} = 13 V; V_{IN} = 5 V; I_{OUT} = 0 A		1.5	3	mA
$I_{L(off)}$	OFF-state output current	V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 25 °C	0	0.01	3	µA
		V_{IN} = V_{OUT} = 0 V; V_{CC} = 13 V; T_j = 125 °C	0		5	

Table 6. Switching (V_{CC} = 13 V, T_j = 25 °C)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	R_L = 2.2 Ω (see *Figure 6*)	—	40	—	µs
$t_{d(off)}$	Turn-off delay time	R_L = 2.2 Ω (see *Figure 6*)	—	28	—	µs
$(dV_{OUT}/dt)_{on}$	Turn-on voltage slope	R_L = 2.2 Ω	—	(see *Figure 26*)	—	V/µs
$(dV_{OUT}/dt)_{off}$	Turn-off voltage slope	R_L = 2.2 Ω	—	(see *Figure 28*)	—	V/µs
W_{ON}	Switching energy losses at turn-on (t_{won})	R_L = 2.2 Ω (see *Figure 6*)	—	2	—	mJ
W_{OFF}	Switching energy losses at turn-off (t_{woff})	R_L = 2.2 Ω (see *Figure 6*)	—	0.6	—	mJ

Table 7. Logic inputs

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{IL}	Low-level input voltage				0.9	V
I_{IL}	Low-level input current	V_{IN} = 0.9 V	1			µA
V_{IH}	High-level input voltage		2.1			V
I_{IH}	High-level input current	V_{IN} = 2.1 V			10	µA
$V_{I(hyst)}$	Input hysteresis voltage		0.25			V
V_{ICL}	Input clamp voltage	I_{IN} = 1 mA	5.5		7	V
		I_{IN} = -1 mA		-0.7		
V_{CSDL}	Low-level CS_DIS voltage				0.9	V
I_{CSDL}	Low-level CS_DIS current	V_{CSD} = 0.9 V	1			µA
V_{CSDH}	High-level CS_DIS voltage		2.1			V
I_{CSDH}	High-level CS_DIS current	V_{CSD} = 2.1 V			10	µA
$V_{CSD(hyst)}$	CS_DIS hysteresis voltage		0.25			V
V_{CSCL}	CS_DIS clamp voltage	I_{CSD} = 1 mA	5.5		7	V
		I_{CSD} = -1 mA		-0.7		

Table 8. Protection and diagnostics(1)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
I_{limH}	Short-circuit current	V_{CC} = 13 V	60	85	120	A
		5 V < V_{CC} < 28 V			120	
I_{limL}	Short-circuit current during thermal cycling	V_{CC} =13 V; $T_R < T_j < T_{TSD}$		21		A
T_{TSD}	Shutdown temperature		150	175	200	°C
T_R	Reset temperature		T_{RS} + 1	T_{RS} + 5		°C
T_{RS}	Thermal reset of status		135			°C
T_{HYST}	Thermal hysteresis (T_{TSD} - T_R)			7		°C
V_{DEMAG}	Turn-off output voltage clamp	I_{OUT} = 2 A; V_{IN} = 0; L = 6 mH	V_{CC} - 41	V_{CC} - 46	V_{CC} - 52	V
V_{ON}	Output voltage drop limitation	I_{OUT} = 0.5 A; T_j = -40 °C to 150 °C		25		mV

1. To ensure long term reliability under heavy overload or short-circuit conditions, protection and related diagnostic signals must be used together with a proper software strategy. If the device is subjected to abnormal conditions, this software must limit the duration and number of activation cycles

Table 9. Current sense (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
K_0	I_{OUT}/I_{SENSE}	I_{OUT} = 0.25 A; V_{SENSE} = 0.5 V T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	2600 2600	6400 6400	10400 10000	
K_1	I_{OUT}/I_{SENSE}	I_{OUT} = 6 A; V_{SENSE} = 0.5 V T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	4900 5500	6800 6800	9500 7950	
dK_1/K_1(1)	Current sense ratio drift	I_{OUT} = 6 A; V_{SENSE} = 0.5 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-15		15	%
K_2	I_{OUT}/I_{SENSE}	I_{OUT} = 10 A; V_{SENSE} = 4 V T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	5700 5900	6700 6700	8350 7400	
dK_2/K_2(1)	Current sense ratio drift	I_{OUT} = 10 A; V_{SENSE}= 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-11		11	%
K_3	I_{OUT}/I_{SENSE}	I_{OUT} = 25 A; V_{SENSE} = 4 V T_j = -40 °C to 150 °C T_j = 25 °C to 150 °C	6000 6000	6600 6600	7350 6950	
dK_3/K_3(1)	Current sense ratio drift	I_{OUT} = 25 A; V_{SENSE}= 4 V; V_{CSD} = 0 V; T_j = -40 °C to 150 °C	-8		8	%
I_{SENSE0}	Analog sense leakage current	I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} =0 V; T_j = -40 °C to 150 °C	0		1	µA
		I_{OUT} = 0 A; V_{SENSE} = 0 V; V_{CSD} = 0 V; V_{IN} = 5 V; T_j = -40 °C to 150 °C	0		2	
		I_{OUT} = 2 A; V_{SENSE} = 0 V; V_{CSD} = 5 V; V_{IN} = 5 V; T_j = -40 °C to 150 °C			1	
I_{OL}	Open load ON-state current detection threshold	V_{IN} = 5 V; 8 V < V_{CC} < 18 V; I_{SENSE} = 5 µA	5		80	mA
V_{SENSE}	Max analog sense output voltage	I_{OUT} = 18 A; R_{SENSE} = 3.9 kΩ	5			V
V_{SENSEH}(2)	Analog sense output voltage in fault condition	V_{CC} = 13 V; R_{SENSE} = 3.9 kΩ		8		V
I_{SENSEH}(2)	Analog sense output current in fault condition	V_{CC} = 13 V; V_{SENSE} = 5 V		9		mA
$t_{DSENSE1H}$	Delay response time from falling edge of CS_DIS pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A I_{SENSE} = 90% of $I_{SENSE\ max}$ (see *Figure 4*)		50	100	µs

Table 9. Current sense (8 V < V_{CC} < 18 V) (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{DSENSE1L}$	Delay response time from rising edge of CS_DIS pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4*)		5	20	µs
$t_{DSENSE2H}$	Delay response time from rising edge of IN pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A I_{SENSE}=90% of $I_{SENSE\ max}$ (see *Figure 4*)		270	600	µs
$\Delta t_{DSENSE2H}$	Delay response time between rising edge of output current and rising edge of current sense	V_{SENSE} < 4V; I_{SENSE} = 90% of $I_{SENSEMAX}$, I_{OUT} = 90% of I_{OUTMAX} I_{OUTMAX}= 3A (see *Figure 7*)			310	µs
$t_{DSENSE2L}$	Delay response time from falling edge of IN pin	V_{SENSE} < 4 V; 1.5 A < I_{OUT} < 25 A I_{SENSE}=10% of $I_{SENSE\ max}$ (see *Figure 4*)		100	250	µs

1. Parameter guaranteed by design, it is not tested.
2. Fault condition includes: power limitation, over-temperature and open load OFF-state detection.

Table 10. Open-load detection (8 V < V_{CC} < 18 V)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V_{OL}	Open-load OFF-state voltage detection threshold	V_{IN} = 0 V	2	See *Figure 5*	4	V
t_{DSTKON}	Output short-circuit to V_{CC} detection delay at turn-off	See *Figure 5*	180		1200	µs
$I_{L(off2)r}$	OFF-state output current at V_{OUT} = 4 V	V_{IN} = 0 V; V_{SENSE} = 0 V V_{OUT} rising from 0 V to 4 V	-120		90	µA
$I_{L(off2)f}$	OFF-state output current at V_{OUT} = 2 V	V_{IN} = 0 V; V_{SENSE} = V_{SENSEH}; V_{OUT} falling from V_{CC} to 2 V	-50		90	µA
t_{d_vol}	Delay response from output rising edge to V_{SENSE} rising edge in open-load	V_{OUT} = 4 V; V_{IN} = 0 V V_{SENSE} = 90% of V_{SENSEH}			20	µs

Figure 4. Current sense delay characteristics

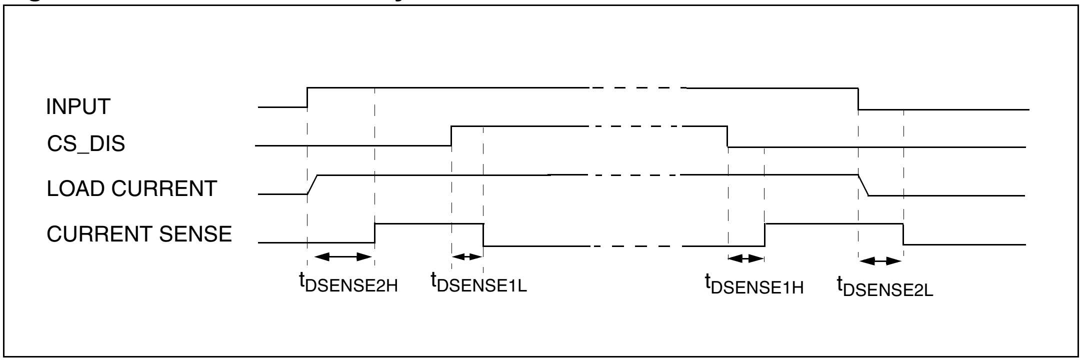


Figure 5. Open-load OFF-state delay timing

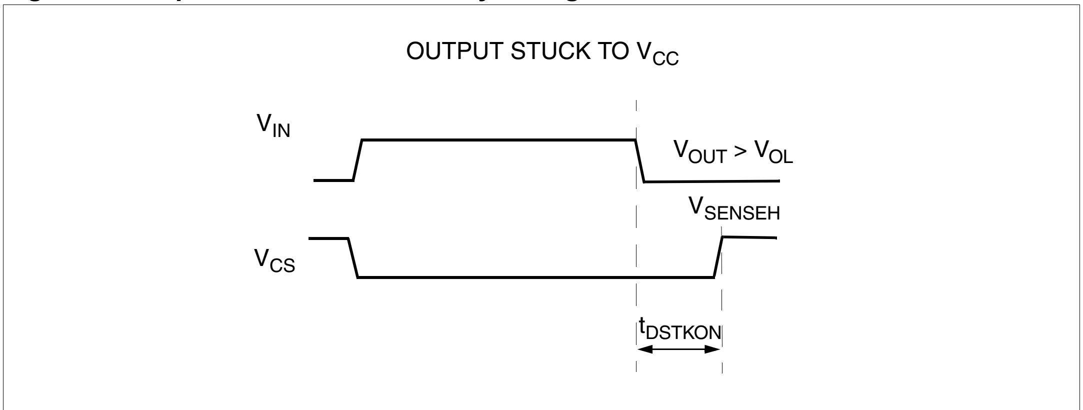


Figure 6. Switching characteristics

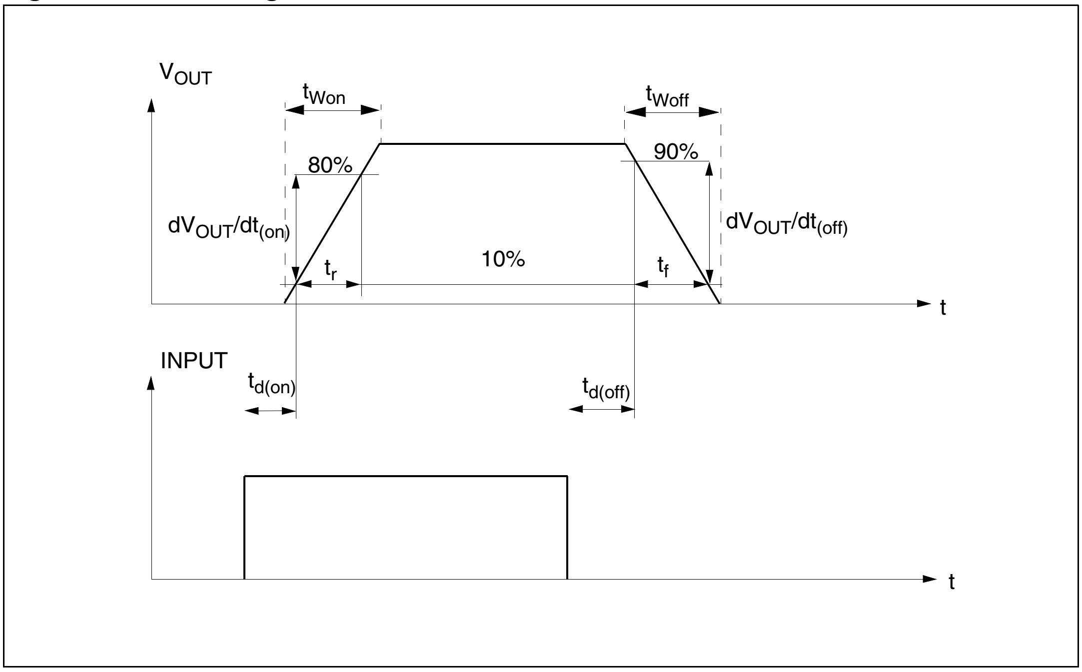


Figure 7. Delay response time between rising edge of ouput current and rising edge of current sense (CS enabled)

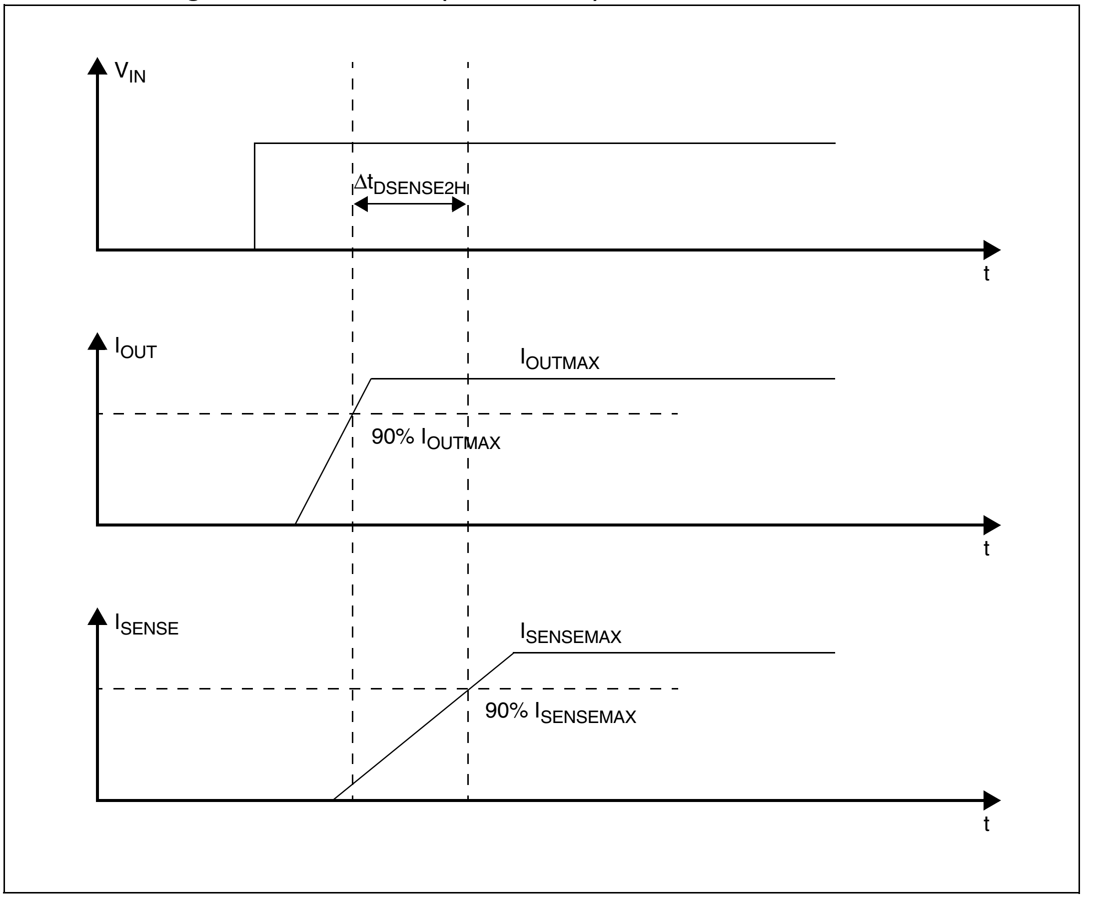


Figure 8. Output voltage drop limitation

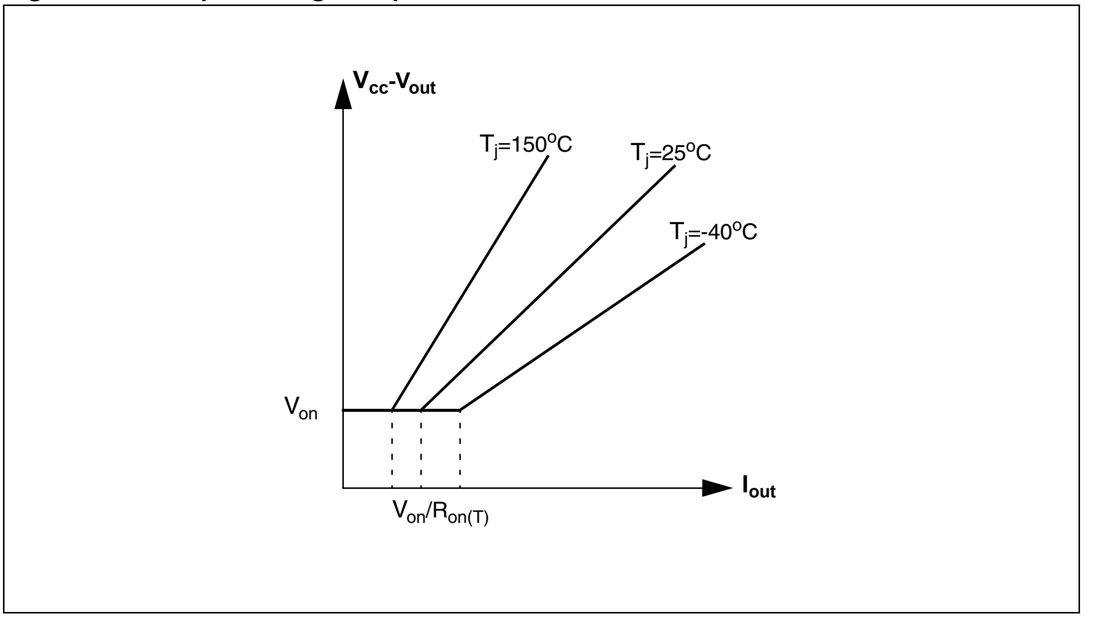


Figure 9. I_{OUT}/I_{SENSE} vs I_{OUT}

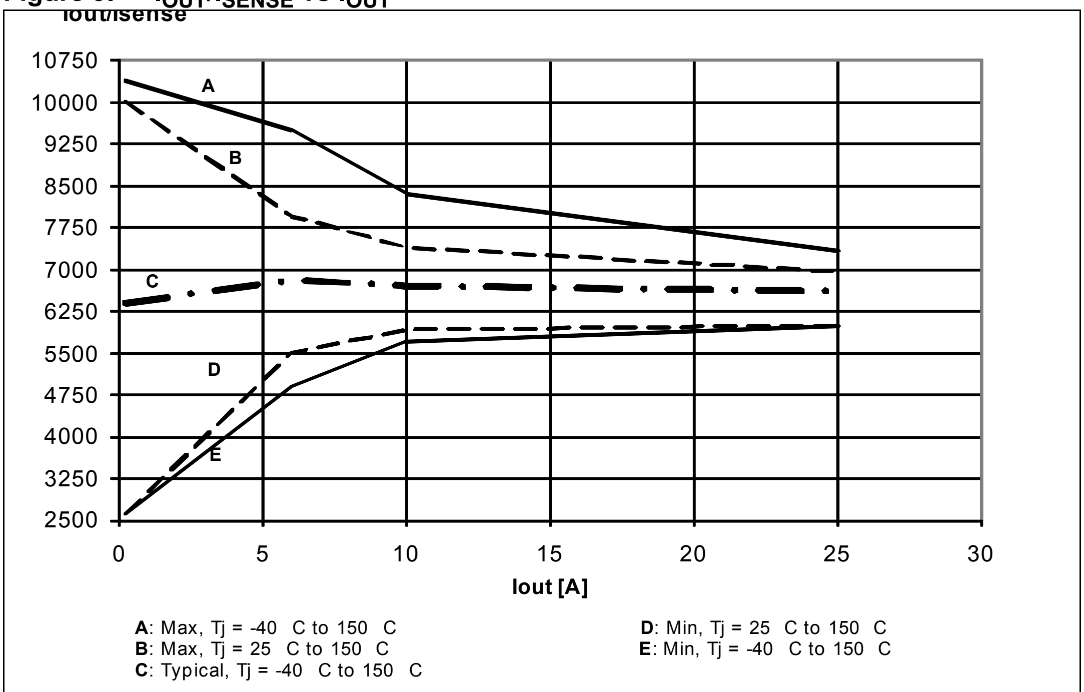
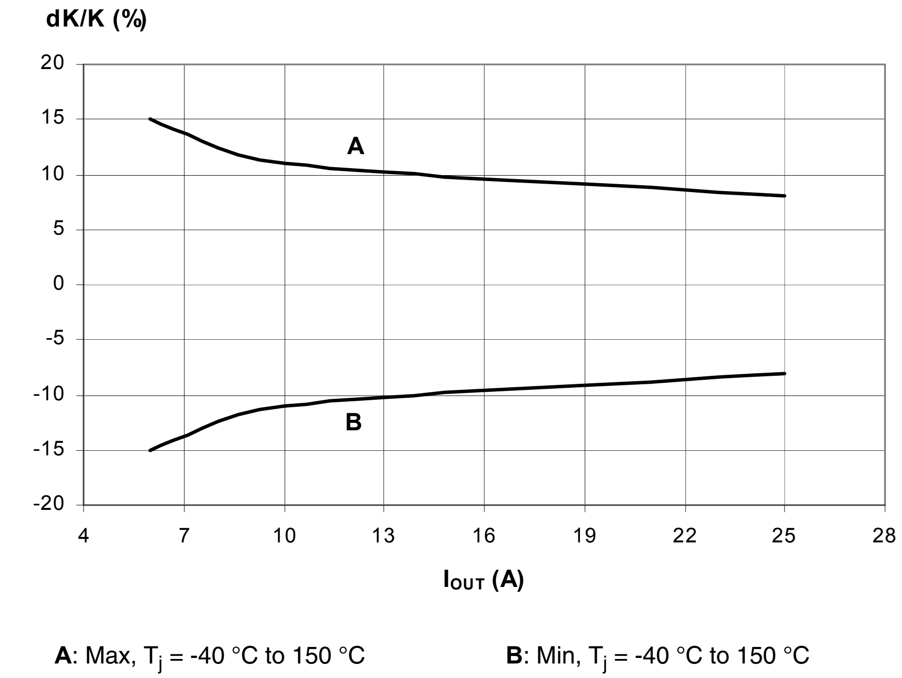


Figure 10. Maximum current sense ratio drift vs load current



Note: Parameter guaranteed by design; it is not tested.

Table 11. Truth table

Conditions	Input	Output	SENSE (V_{CSD} = 0 V)(1)
Normal operation	L H	L H	0 Nominal
Overtemperature	L H	L L	0 V_{SENSEH}
Undervoltage	L H	L L	0 0
Overload	H H	X (no power limitation) Cycling (power limitation)	Nominal V_{SENSEH}
Short-circuit to GND (power limitation)	L H	L L	0 V_{SENSEH}
Open load OFF-state (with external pull-up)	L	H	V_{SENSEH}
Short-circuit to V_{CC} (external pull-up disconnected)	L H	H H	V_{SENSEH} < Nominal
Negative output voltage clamp	L	L	0

1. If the V_{CSD} is high, the SENSE output is at a high-impedance, its potential depends on leakage currents and external circuit.

Table 12. Electrical transient requirements (part 1)

ISO 7637-2: 2004(E) Test pulse	Test levels[1]		Number of pulses or test times	Burst cycle/pulse repetition time		Delays and Impedance
	III	IV		Min.	Max.	
1	-75 V	-100 V	5000 pulses	0.5 s	5 s	2 ms, 10 Ω
2a	+37 V	+50 V	5000 pulses	0.2 s	5 s	50 µs, 2 Ω
3a	-100 V	-150 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
3b	+75 V	+100 V	1h	90 ms	100 ms	0.1 µs, 50 Ω
4	-6 V	-7 V	1 pulse			100 ms, 0.01 Ω
5b[2]	+65 V	+87 V	1 pulse			400 ms, 2 Ω

1. The above test levels must be considered referred to V_{CC} = 13.5 V except for pulse 5b.
2. Valid in case of external load dump clamp: 40 V maximum referred to ground.

Table 13. Electrical transient requirements (part 2)

ISO 7637-2: 2004(E) Test pulse	Test level results	
	III	IV
1	C	C
2a	C	C
3a	C	C
3b	C	C
4	C	C
5b[1]	C	C

1. Valid in case of external load dump clamp: 40V maximum referred to ground.

Table 14. Electrical transient requirements (part 3)

Class	Contents
C	All functions of the device are performed as designed after exposure to disturbance.
E	One or more functions of the device are not performed as designed after exposure to disturbance and cannot be returned to proper operation without replacing the device.

2.4 Waveforms

Figure 11. Normal operation

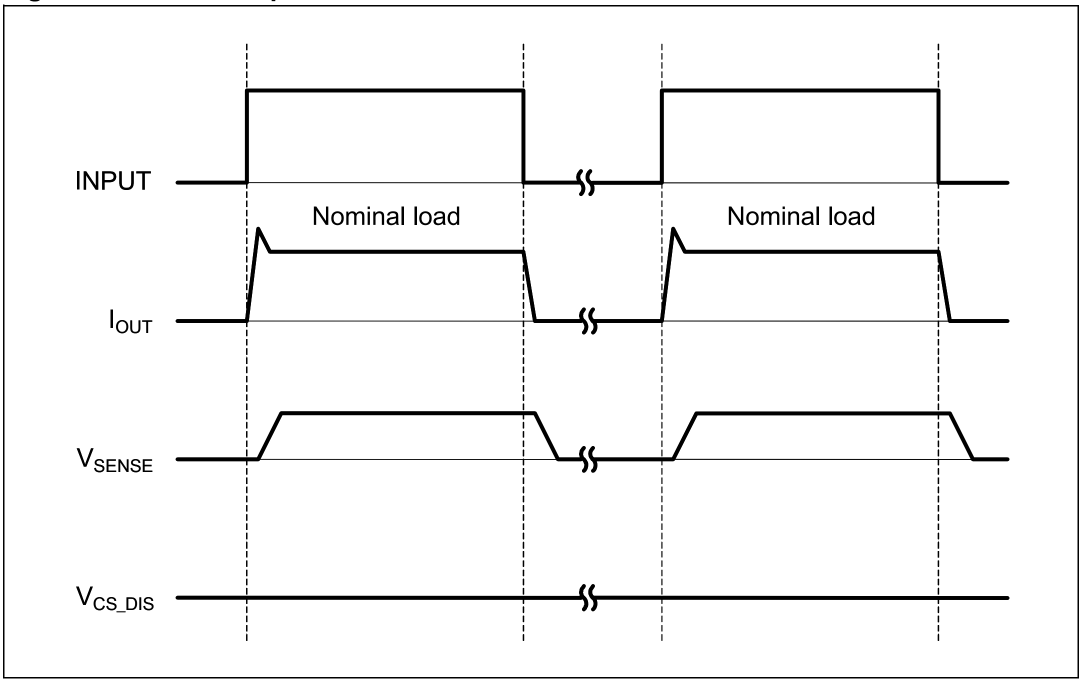


Figure 12. Overload or short to GND

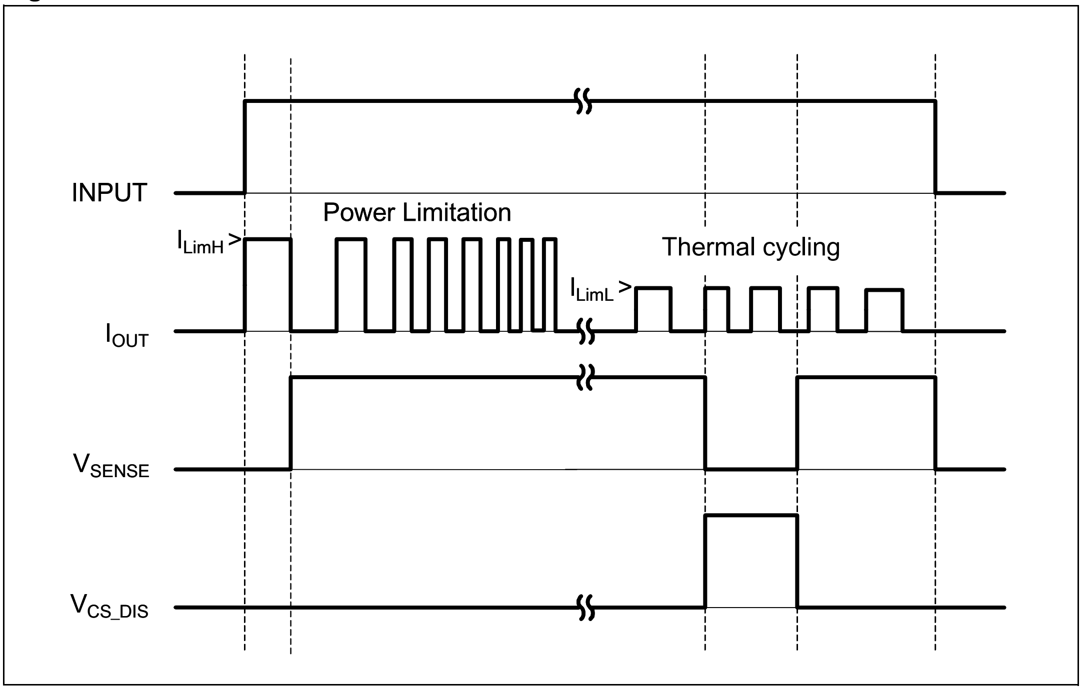


Figure 13. Intermittent overload

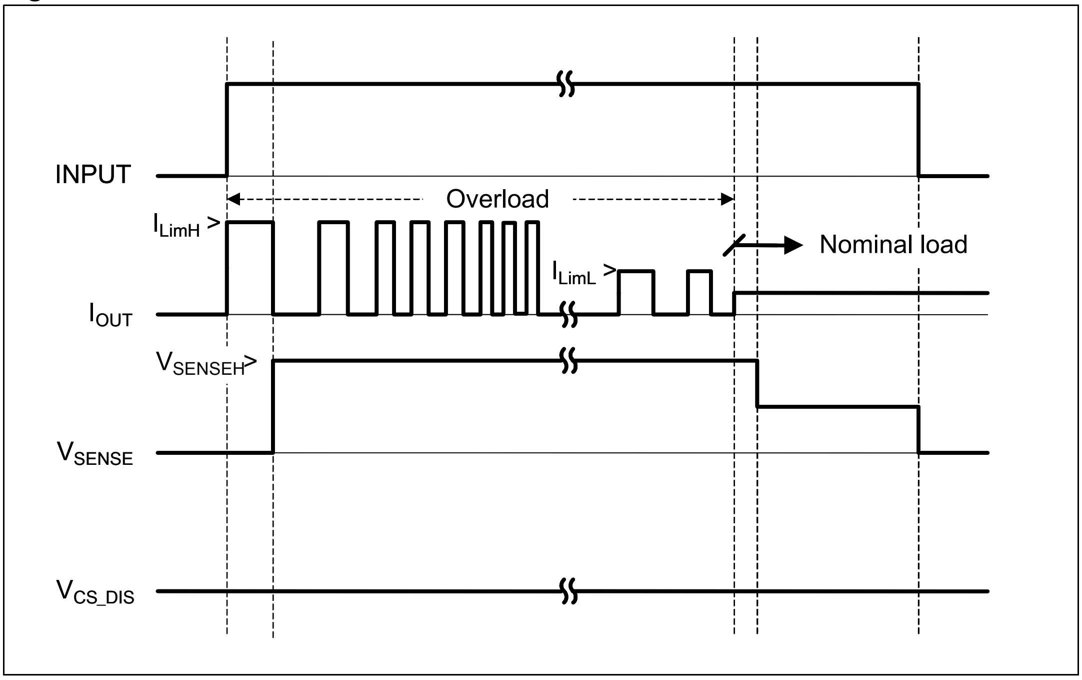


Figure 14. OFF-state open-load with external circuitry

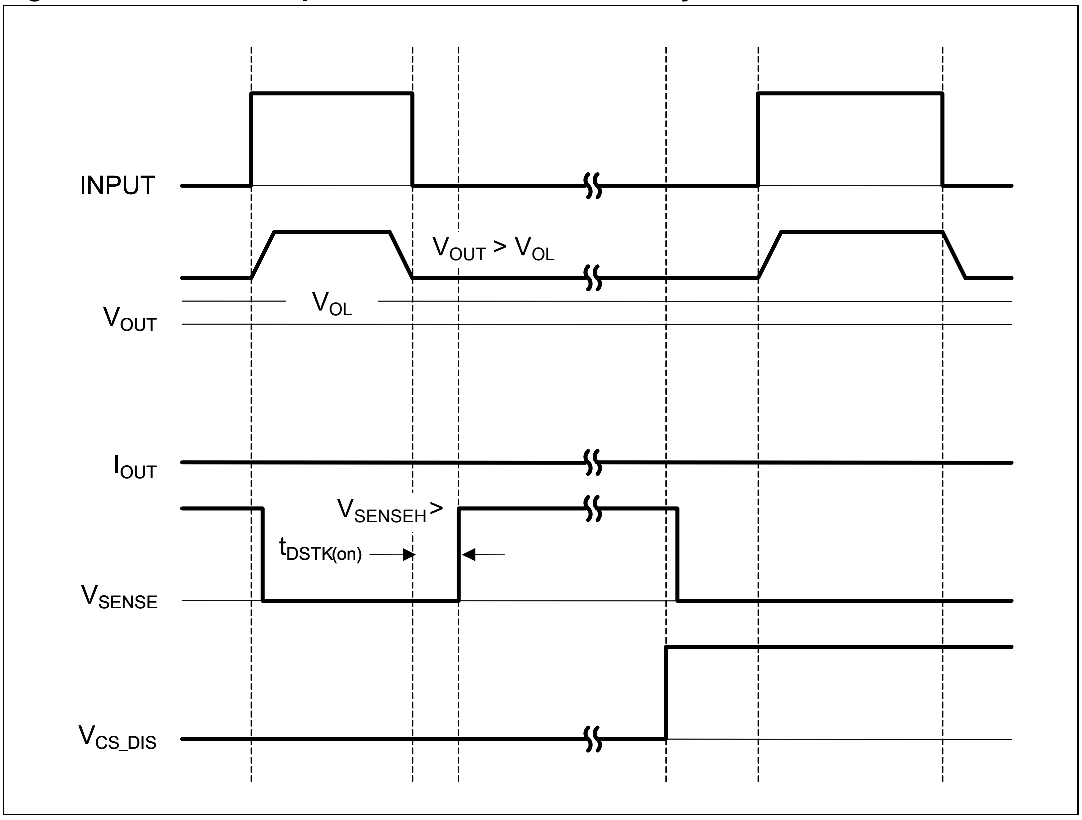


Figure 15. Short to V_{CC}

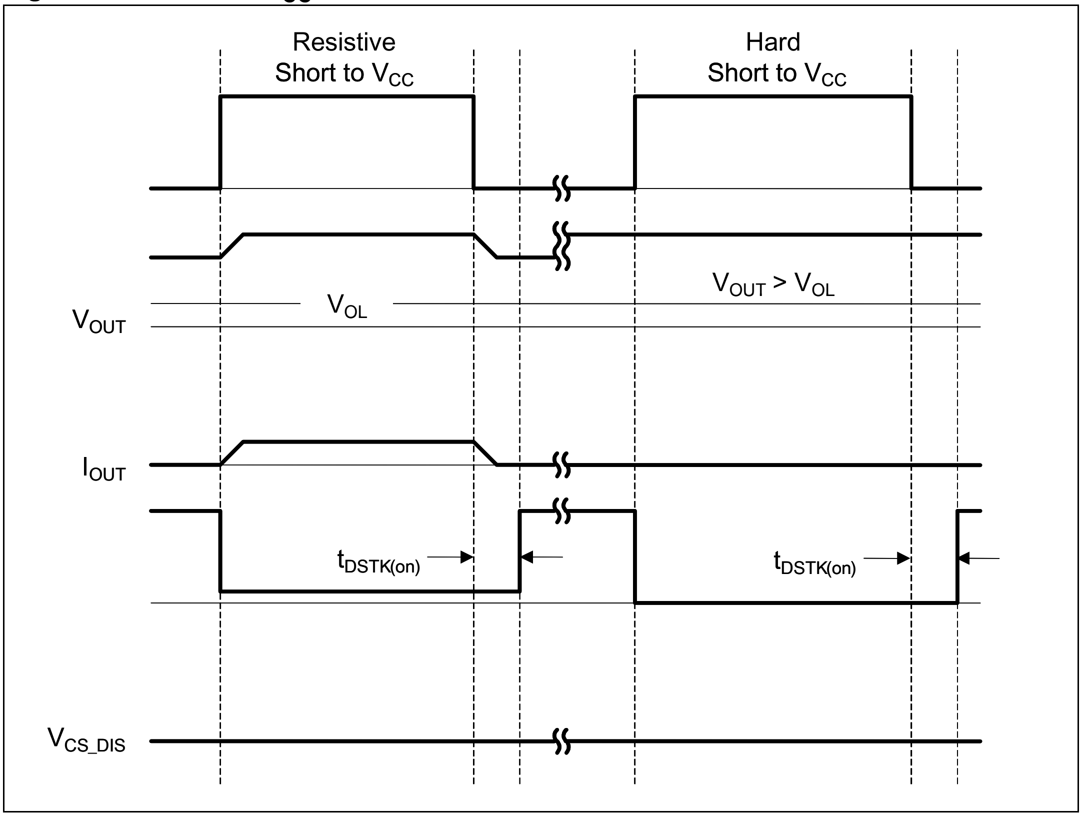
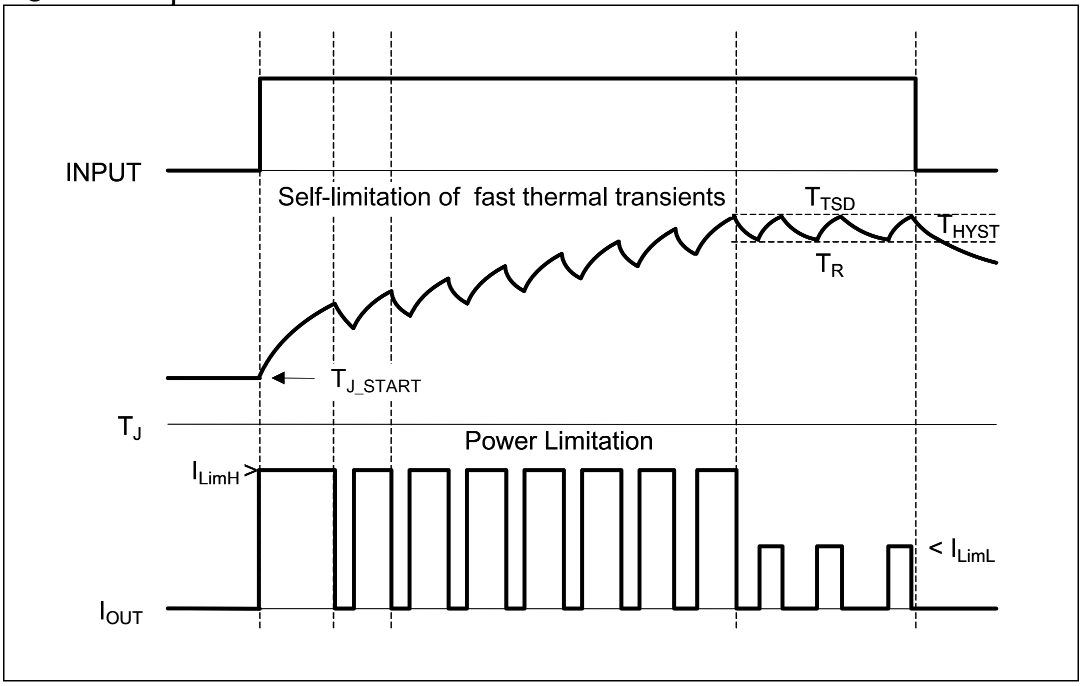


Figure 16. T_j evolution in overload or short to GND



2.5 Electrical characteristics curves

Figure 17. OFF-state output current

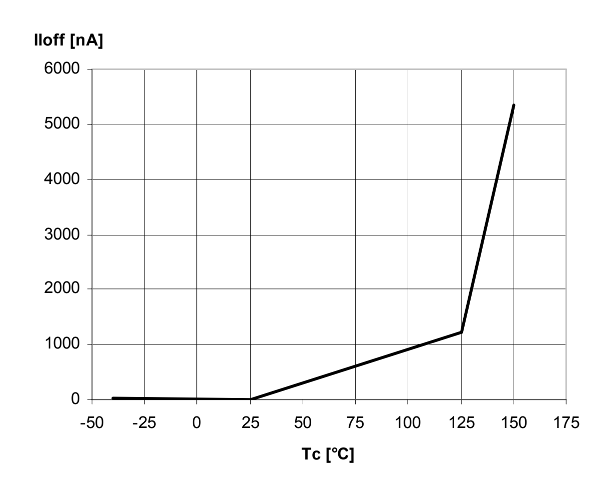


Figure 18. High-level input current

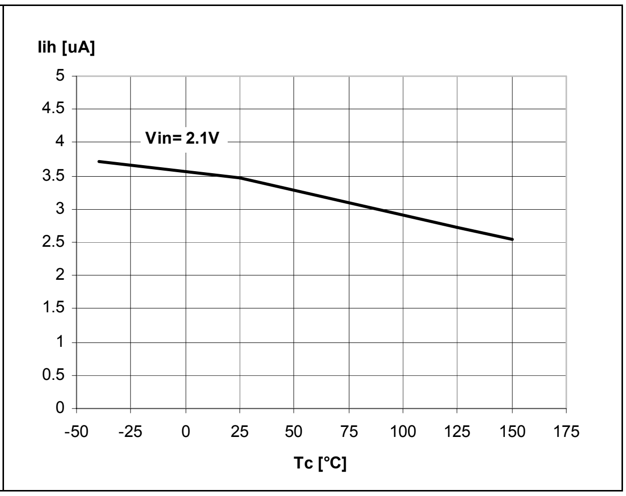


Figure 19. Input clamp voltage

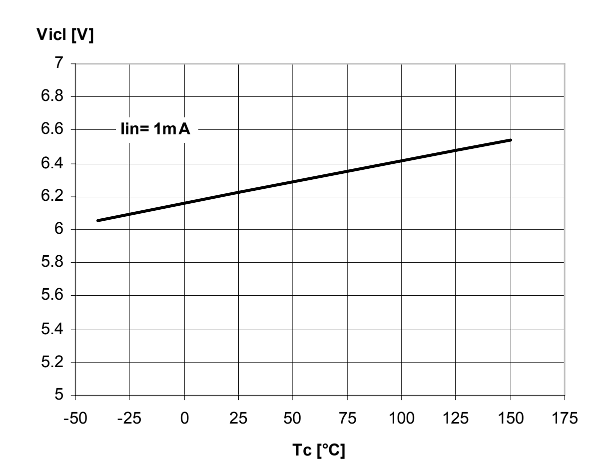


Figure 20. Low-level input voltage

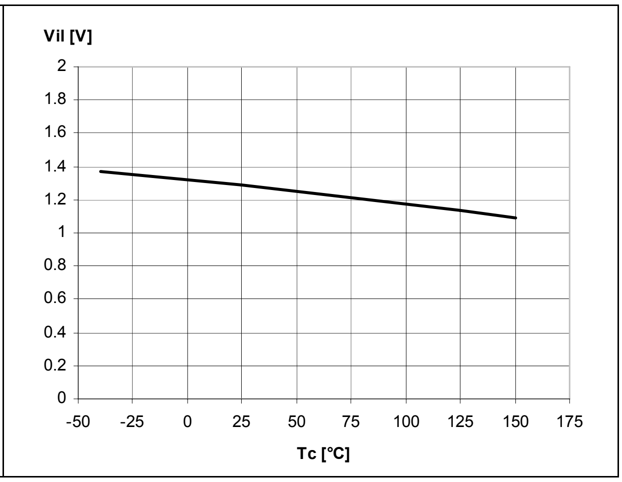


Figure 21. High-level input voltage

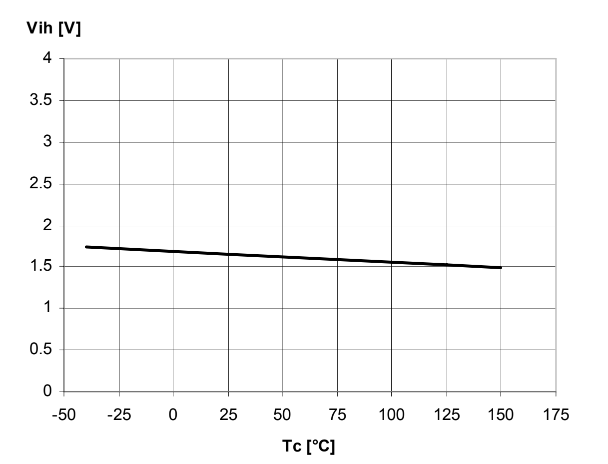


Figure 22. Input hysteresis voltage

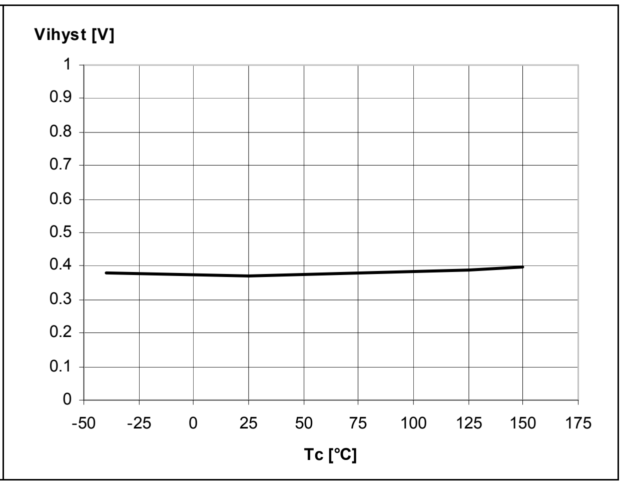


Figure 23. ON-state resistance vs T_{case}

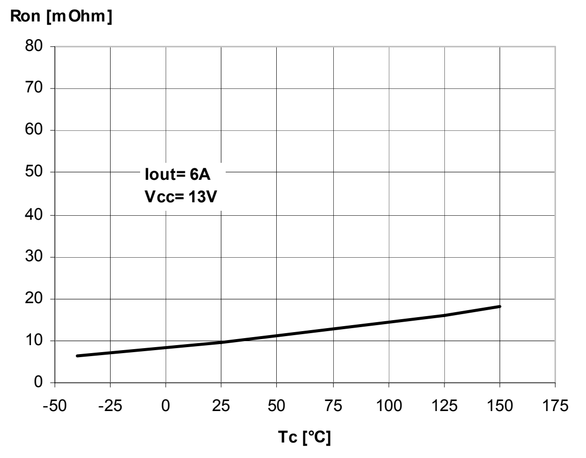


Figure 24. ON-state resistance vs V_{CC}

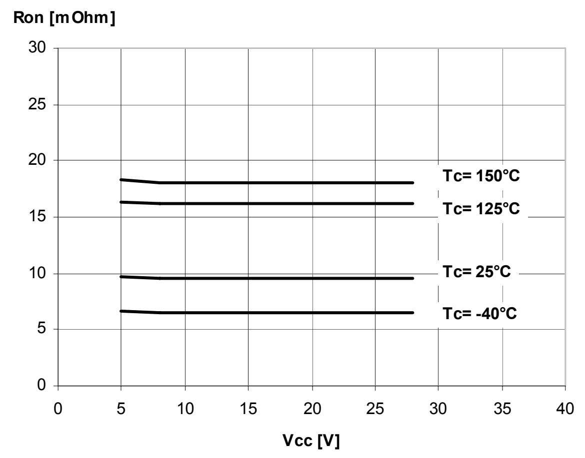


Figure 25. Undervoltage shutdown

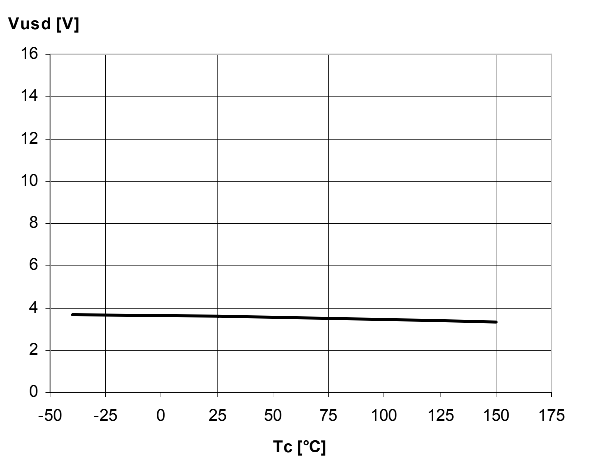


Figure 26. Turn-on voltage slope

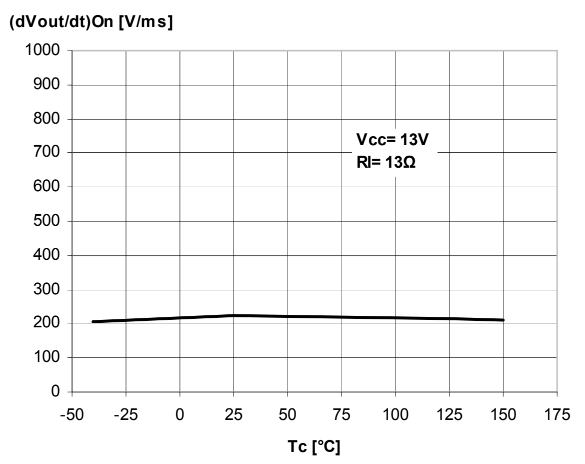


Figure 27. I_{LIMH} vs T_{case}

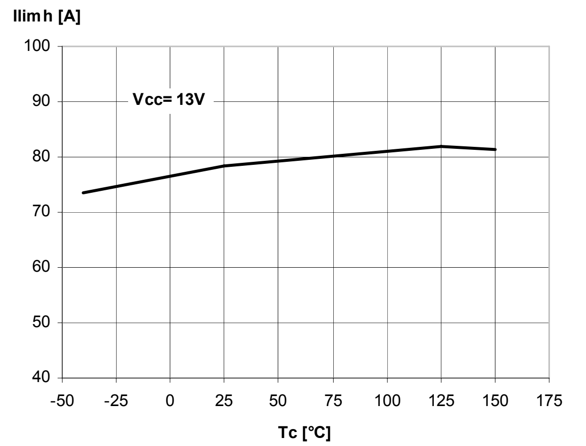


Figure 28. Turn-off voltage slope

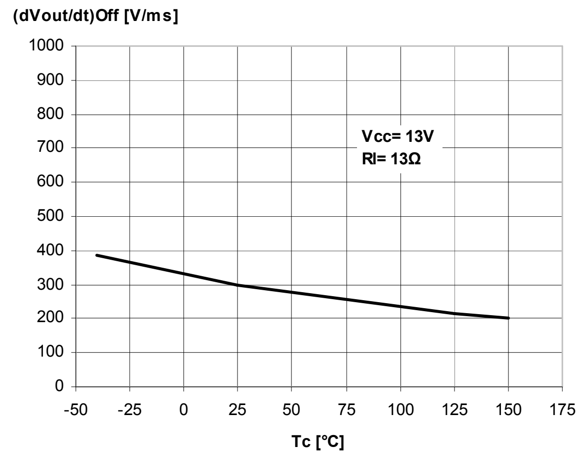


Figure 29. High-level CS_DIS voltage

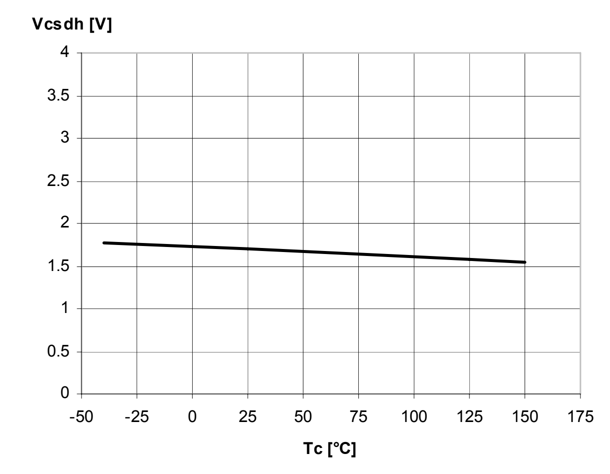


Figure 30. CS_DIS clamp voltage

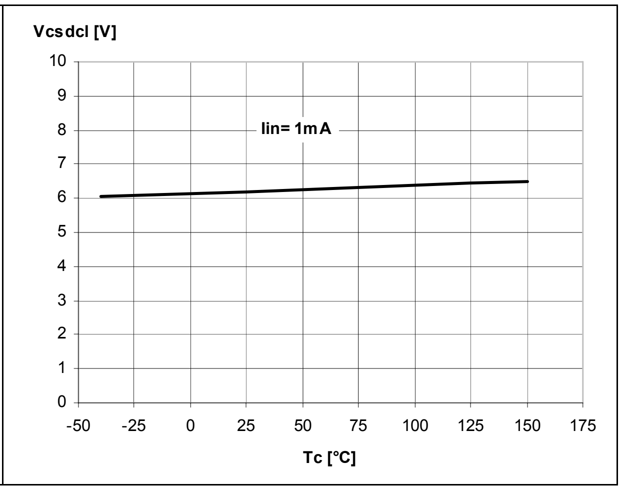
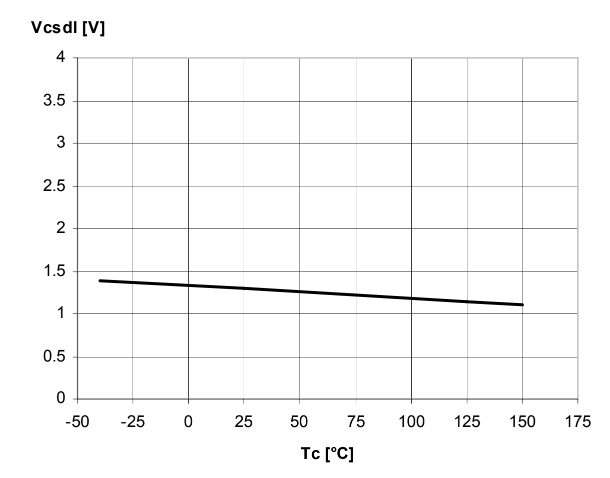
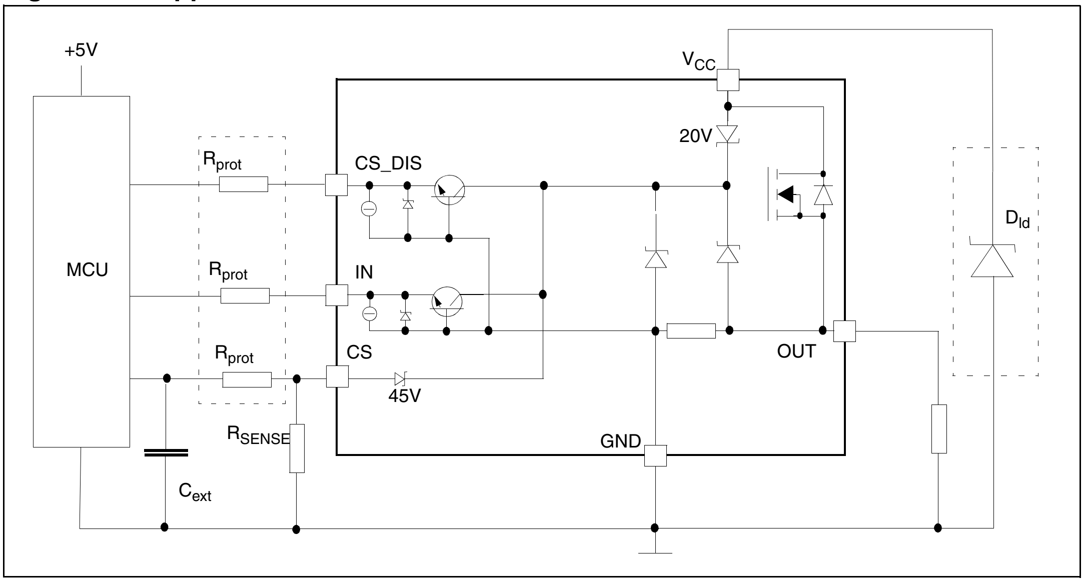


Figure 31. Low-level CS_DIS voltage



3 Application information

Figure 32. Application schematic



3.1 Load dump protection

D_{ld} is necessary (voltage transient suppressor) if the load dump peak voltage exceeds the V_{CC} max DC rating. The same applies if the device is subject to transients on the V_{CC} line that are greater than the ones shown in the ISO 7637-2 2004 (E) table.

3.2 MCU I/Os protection

When negative transients are present on the V_{CC} line, the control pins is pulled negative to approximatly -1.5 V. ST suggests to insert a resistor (R_{prot}) in line to prevent the microcontroller I/Os pins to latch-up.

The value of these resistors is a compromise between the leakage current of microcontroller and the current required by the HSD I/Os (input levels compatibility) with the latch-up limit of microcontroller I/Os.

Equation 1

$$-V_{CCpeak} / I_{latchup} \le R_{prot} \le (V_{OH\mu C} - V_{IH}) / I_{IHmax}$$

Calculation example:

For V_{CCpeak} = - 1.5 V; $I_{latchup} \ge$ 20 mA; $V_{OH\mu C} \ge$ 4.5 V

$75\ \Omega \le R_{prot} \le 240\ k\Omega$.

Recommended values: R_{prot} =10 kΩ, C_{EXT} =10 nF.

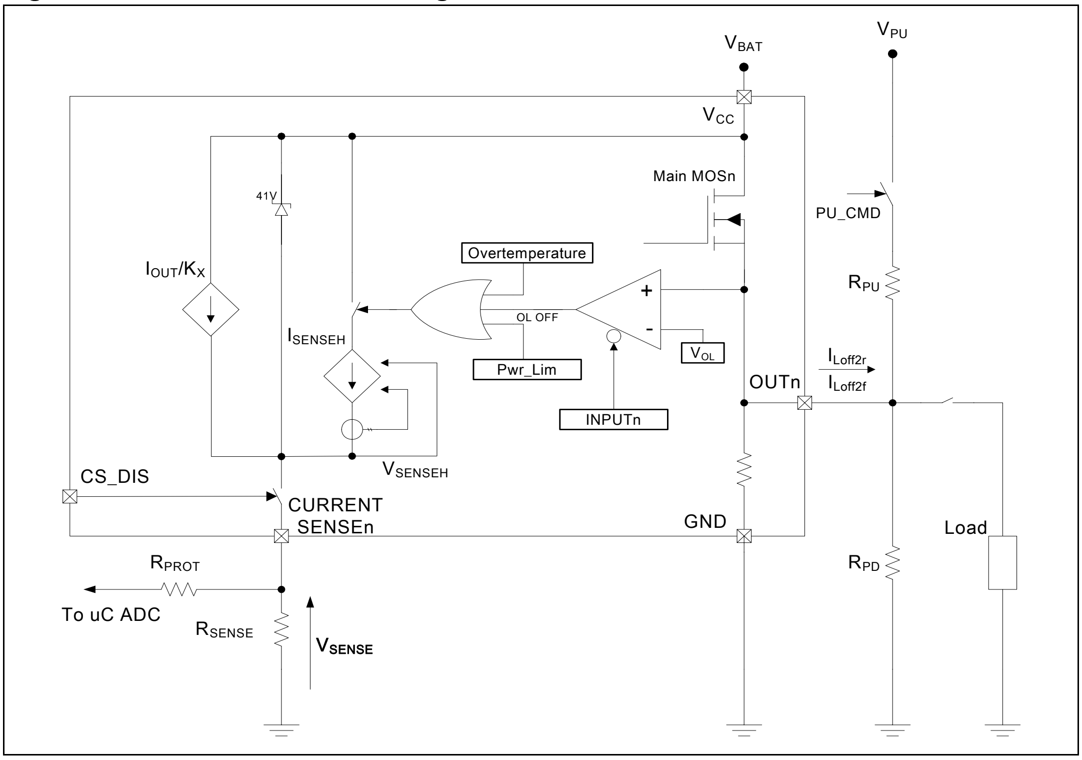
3.3 Current sense and diagnostic

The current sense pin performs a double function (see *Figure 33: Current sense and diagnostic*):

- **Current mirror of the load current in normal operation,** delivering a current proportional to the load one according to a known ratio $\mathbf{K_X}$.
  The current I_{SENSE} can be easily converted to a voltage V_{SENSE} by means of an external resistor R_{SENSE}. Linearity between I_{OUT} and V_{SENSE} is ensured up to 5 V minimum (see parameter V_{SENSE} in *Table 9: Current sense (8 V < V_{CC} < 18 V)*). The current sense accuracy depends on the output current (refer to current sense electrical characteristics *Table 9: Current sense (8 V < V_{CC} < 18 V)*).
- **Diagnostic flag in fault conditions**, delivering a fixed voltage V_{SENSEH} up to a maximum current I_{SENSEH} in case of the following fault conditions (refer to *Table 11: Truth table*):
  - Power limitation activation
  - Overtemperature
  - Short to V_{CC} in OFF-state
  - Open load in OFF-state with additional external components.

A logic level high on CS_DIS pin sets at the same time all the current sense pins of the device in a high-impedance state, thus disabling the current monitoring and diagnostic detection. This feature allows multiplexing of the microcontroller analog inputs by sharing of sense resistance and ADC line among different devices.

Figure 33. Current sense and diagnostic



3.3.1 Short to V_{CC} and OFF-state open-load detection

Short to V_{CC}

A short-circuit between V_{CC} and output is indicated by the relevant current sense pin set to V_{SENSEH} during the device OFF-state. Small or no current is delivered by the current sense during the ON-state depending on the nature of the short-circuit.

OFF-state open-load with external circuitry

Detection of an open load in off mode requires an external pull-up resistor R_{PU} connecting the output to a positive supply voltage V_{PU}.

It is preferable V_{PU} to be switched off during the module standby mode in order to avoid the overall standby current consumption to increase in normal conditions, i.e. when load is connected.

An external pull-down resistor R_{PD} connected between output and GND is mandatory to avoid misdetection in case of floating outputs in OFF-state (see *Figure 33: Current sense and diagnostic*).

R_{PD} must be selected in order to ensure $V_{OUT} < V_{OLmin}$ unless pulled-up by the external circuitry:

Equation 2

$$V_{OUT}\Big|_{Pull-up\_OFF} = R_{PD} \cdot I_{L(off2)f} < V_{OLmin} = 2\ V$$

$R_{PD} \leq 22\ k\Omega$ is recommended.

For proper open load detection in OFF-state, the external pull-up resistor must be selected according to the following formula:

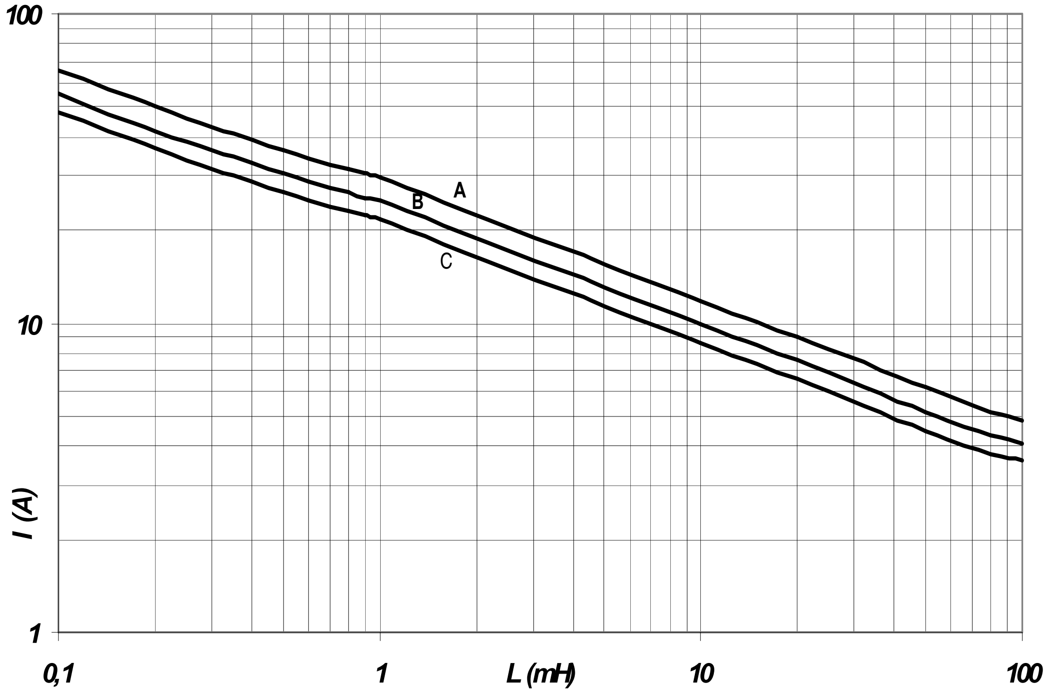
Equation 3

$$V_{OUT}\Big|_{Pull-up\_ON} = \frac{(R_{PD} \cdot V_{PU}) - (R_{PU} \cdot R_{PD} \cdot I_{L(off2)r})}{(R_{PU} + R_{PD})} > V_{OLmax} = 4\ V$$

For the values of V_{OLmin} ,V_{OLmax}, $I_{L(off2)r}$ and $I_{L(off2)f}$ (see *Table 10: Open-load detection (8 V < VCC < 18 V)*).

3.4 Maximum demagnetization energy (V_{CC} = 13.5 V)

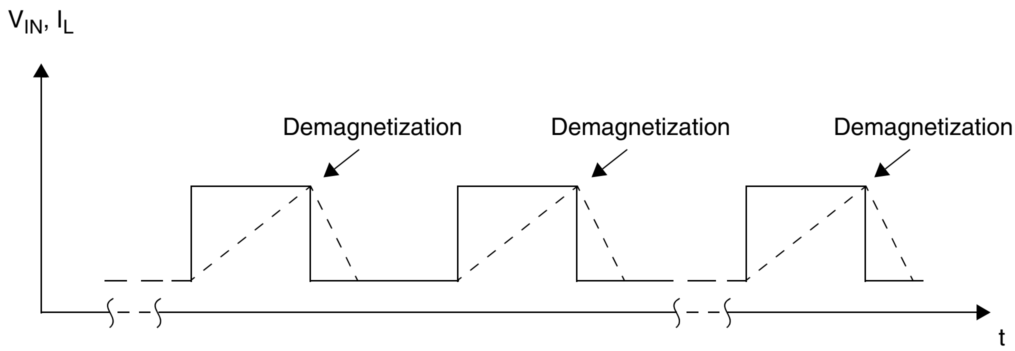
Figure 34. Maximum turn-off current versus inductance( )



A: T_{jstart} = 150 °C (single pulse)

B: T_{jstart} = 100 °C (repetitive pulse)

C: T_{jstart} = 125 °C (repetitive pulse)

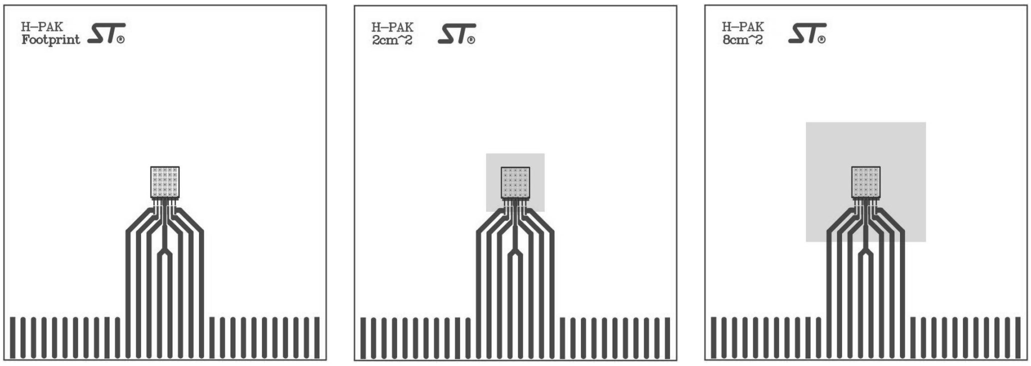


Note:
Values are generated with R_L = 0 Ω.
In case of repetitive pulses, T_{jstart} (at beginning of each demagnetization) of every pulse must not exceed the temperature specified above for curves A and B.

4 Package and PC board thermal data

4.1 HPAK thermal data

Figure 35. PC board



Note:
Layout condition of Rth and Zth measurements (PCB FR4 area = 58 mm x 58 mm, PCB thickness =1.8 mm, Cu thickness = 70 µm, Copper areas: from minimum pad lay-out to 8 cm^2).

Figure 36. $R_{thj-amb}$ vs. PCB copper area in open box free air condition

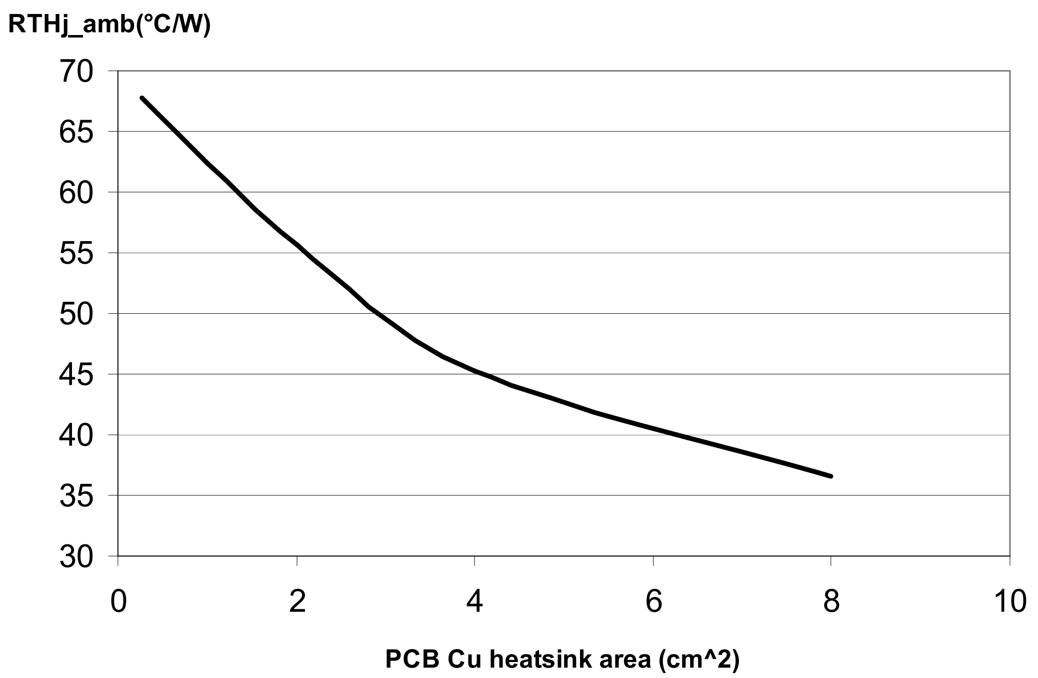


Figure 37. HPAK thermal impedance junction ambient single pulse

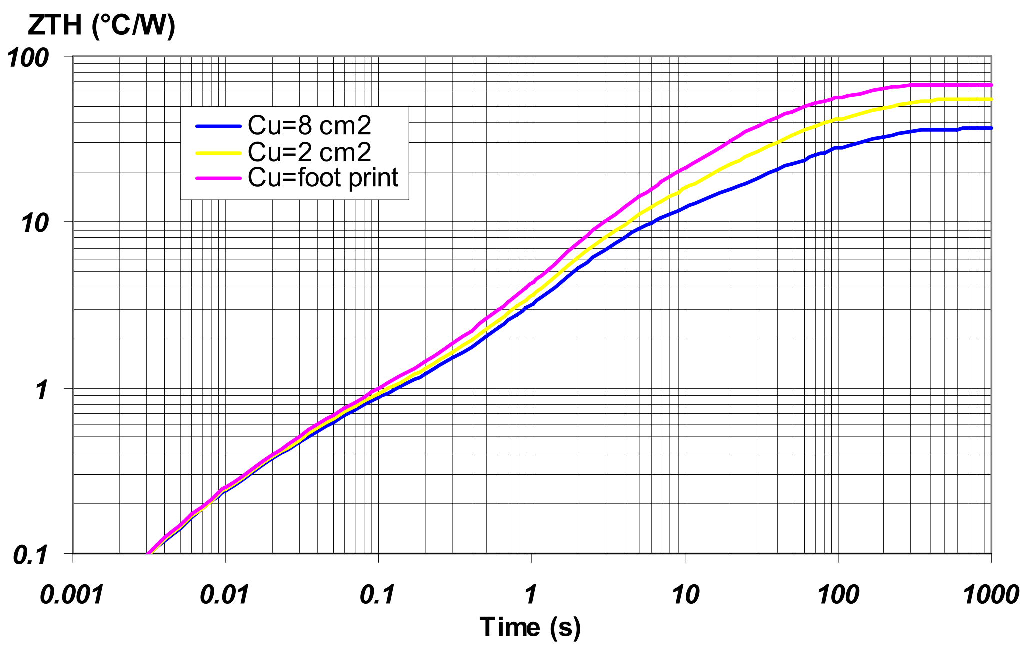
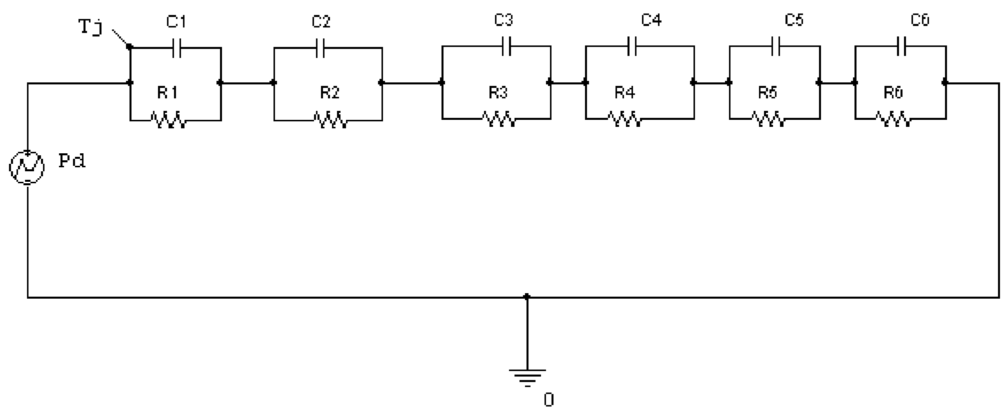


Figure 38. Thermal fitting model of a single-channel HSD in HPAK



Note:
The fitting model is a simplified thermal tool and is valid for transient evolutions where the embedded protections (power limitation or thermal cycling during thermal shutdown) are not triggered.

Equation 4: pulse calculation formula

$$Z_{TH\delta} = R_{TH} \cdot \delta + Z_{THtp}(1 - \delta)$$

where $\delta = t_P/T$

Table 15. Thermal parameter

Area/island (cm^2)	Footprint	4	8
R1 (°C/W)	0.01		
R2 (°C/W)	0.15		
R3 (°C/W)	0.5		
R4 (°C/W)	8		
R5 (°C/W)	28	22	12
R6 (°C/W)	31	25	16
C1 (W.s/°C)	0.005		
C2 (W.s/°C)	0.05		
C3 (W.s/°C)	0.1		
C4 (W.s/°C)	0.4		
C5 (W.s/°C)	0.8	1.4	3
C6 (W.s/°C)	3	6	9

5 Package and packing information

5.1 ECOPACK®

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: www.st.com. ECOPACK® is an ST trademark.

5.2 HPAK mechanical data

Figure 39. HPAK package dimension

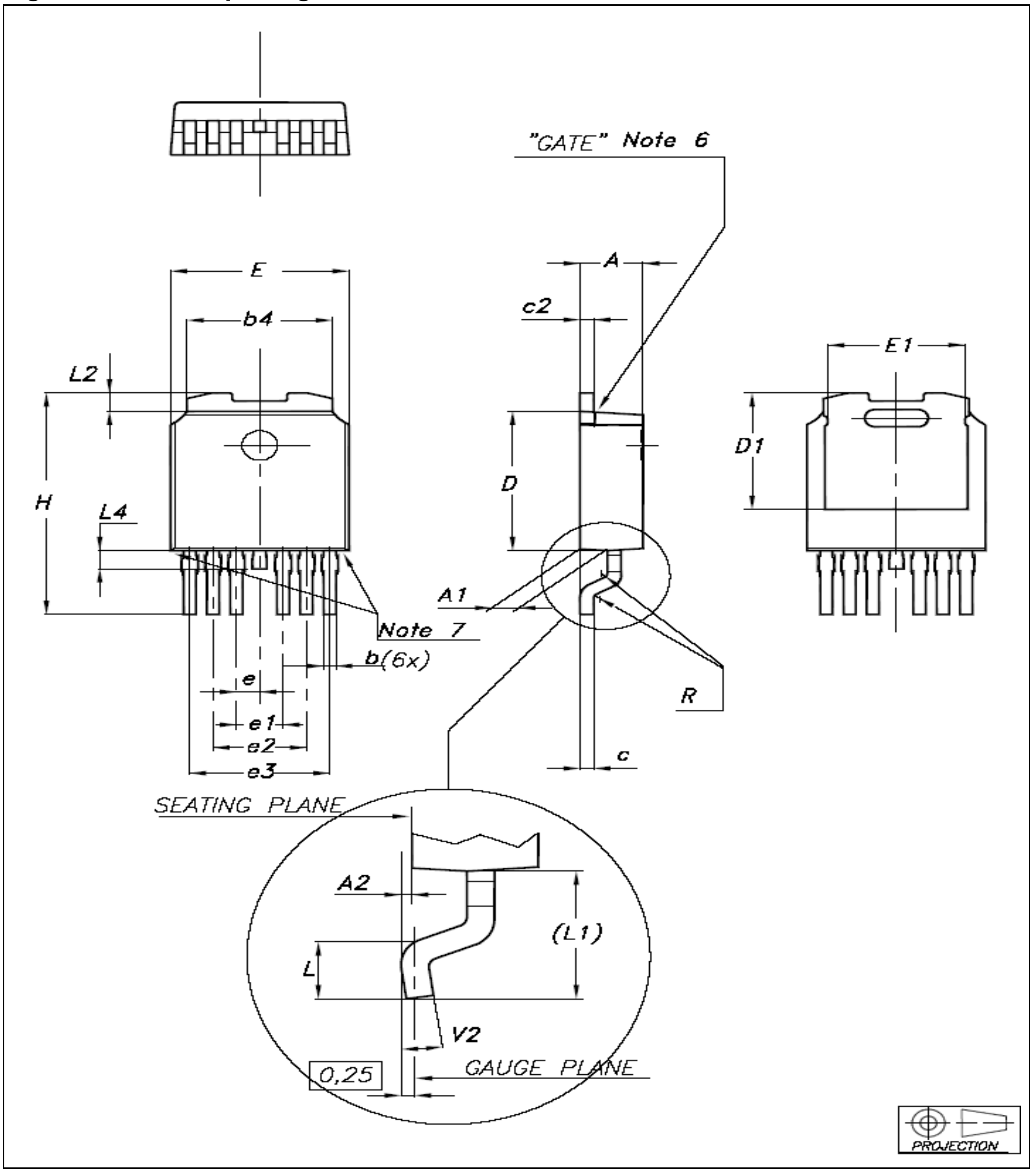
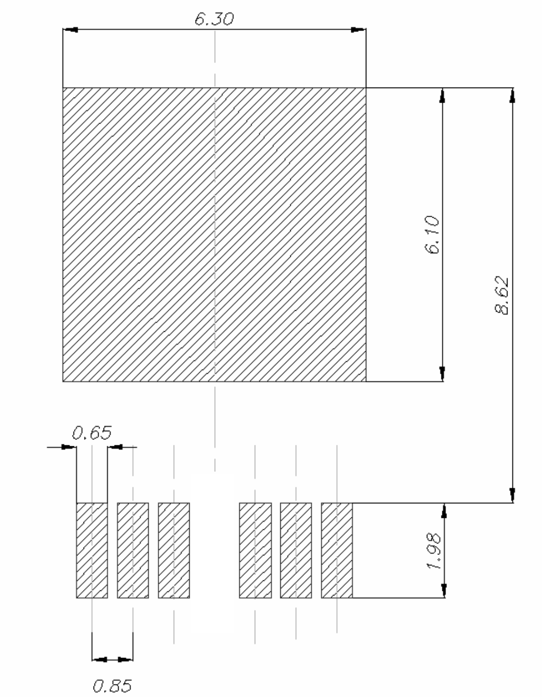


Table 16. HPAK mechanical data

Ref. dim	Data book mm		
	Nom.	Min.	Max.
A		2.20	2.40
A1		0.90	1.10
A2		0.03	0.23
b		0.40	0.55
b4		5.20	5.40
c		0.45	0.60
c2		0.48	0.60
D		6.00	6.20
D1	5.10		
E		6.40	6.60
E1	5.20		
e	0.85		
e1		1.60	1.80
e2		3.30	3.50
e3		5.00	5.20
H		9.35	10.10
L		1	
(L1)	2.80		
L2	0.80		
L4		0.60	1.00
R	0.20		
V2		0°	8°

5.3 HPAK suggested land pattern

Figure 40. HPAK suggested pad layout



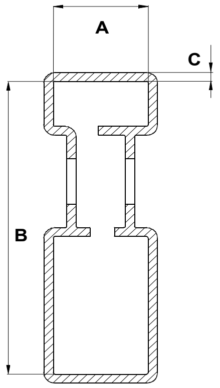
All dimensions are in mm.

Note:
The land pattern proposed is not intended to overrule User's PCB design, manufacturing and soldering process rules

5.4 Packing information

The devices can be packed in tube or tape and reel shipments (see *Table 17: Device summary*).

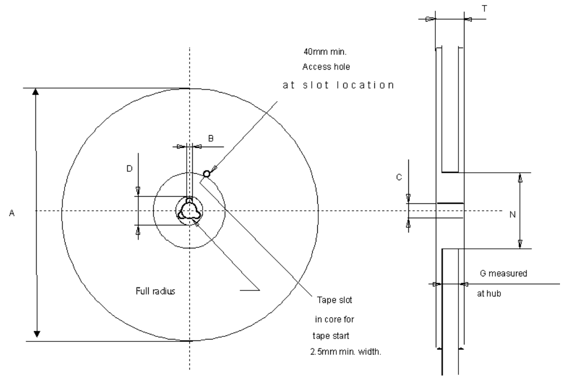
Figure 41. HPAK tube shipment (no suffix)



Base q.ty	75
Bulk q.ty	3000
Tube length (± 0.5)	532
A	6
B	21.3
C (± 0.1)	0.6

All dimensions are in mm.

Figure 42. HPAK tape and reel (suffix “TR”)



REEL DIMENSIONS

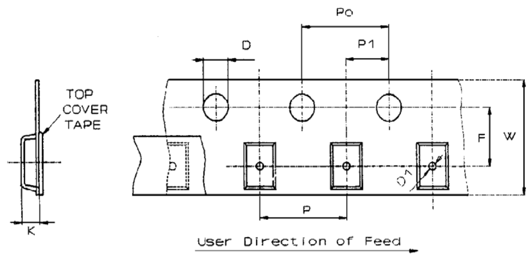
All dimensions are in mm.

Base q.ty	2500
Bulk q.ty	2500
A (max)	330
B (min)	1.5
C (± 0.2)	13
F	20.2
G (+ 2 / -0)	16.4
N (min)	60
T (max)	22.4

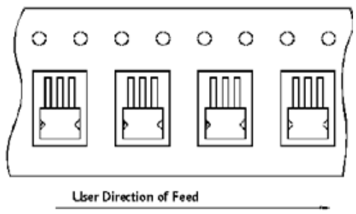
TAPE DIMENSIONS

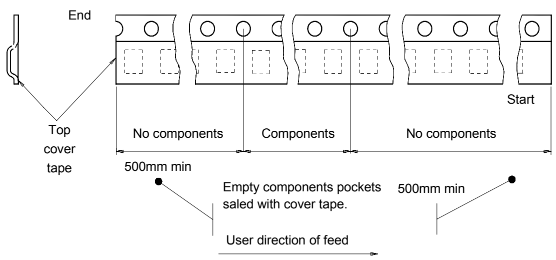
According to Electronic Industries Association (EIA) Standard 481 rev. A, Feb 1986

Tape width	W	16
Tape hole spacing	P0 (± 0.1)	4
Component spacing	P	8
Hole diameter	D (± 0.1/-0)	1.5
Hole diameter	D1 (min)	1.5
Hole position	F (± 0.05)	7.5
Compartment depth	K (max)	2.75
Hole spacing	P1 (± 0.1)	2



All dimensions are in mm.





6 Order codes

Table 17. Device summary

Package	Order codes	
	Tube	Tape and reel
6 pins HPAK	VN5E010AFH-E	VN5E010AFHTR-E

7 Revision history

Table 18. Document revision history

Date	Revision	Changes
02-Nov-2010	1	Initial release.
15-Dec-2010	2	Changed document state from preliminary data to datasheet.