

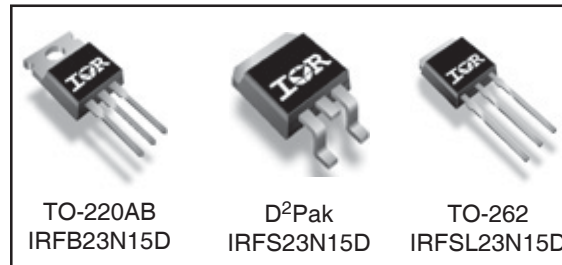
**Applications**

- High frequency DC-DC converters
- Lead-Free

<b>V<sub>DSS</sub></b>	<b>R<sub>DS(on) max</sub></b>	<b>I<sub>D</sub></b>
<b>150V</b>	<b>0.090Ω</b>	<b>23A</b>

**Benefits**

- Low Gate-to-Drain Charge to Reduce Switching Losses
- Fully Characterized Capacitance Including Effective C<sub>OSS</sub> to Simplify Design, (See App. Note AN1001)
- Fully Characterized Avalanche Voltage and Current



**Absolute Maximum Ratings**

	<b>Parameter</b>	<b>Max.</b>	<b>Units</b>
I <sub>D</sub> @ T <sub>C</sub> = 25°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	23	A
I <sub>D</sub> @ T <sub>C</sub> = 100°C	Continuous Drain Current, V <sub>GS</sub> @ 10V	17	
I <sub>DM</sub>	Pulsed Drain Current ①	92	
P <sub>D</sub> @ T <sub>A</sub> = 25°C	Power Dissipation ②	3.8	W
P <sub>D</sub> @ T <sub>C</sub> = 25°C	Power Dissipation	136	
	Linear Derating Factor	0.9	W/°C
V <sub>GS</sub>	Gate-to-Source Voltage	± 30	V
dv/dt	Peak Diode Recovery dv/dt ③	4.1	V/ns
T <sub>J</sub>	Operating Junction and	-55 to + 175	°C
T <sub>STG</sub>	Storage Temperature Range		
	Soldering Temperature, for 10 seconds		
	Mounting torque, 6-32 or M3 screw④	10 lbf•in (1.1N•m)	

**Typical SMPS Topologies**

- Telecom 48V input DC-DC Active Clamp Reset Forward Converter

# IRFB/IRFS/IRFSL23N15DPbF

Static @ T<sub>J</sub> = 25°C (unless otherwise specified)

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	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	150	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS</sub> /ΔT <sub>J</sub>	Breakdown Voltage Temp. Coefficient	—	0.18	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resistance	—	—	0.090	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 14A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	3.0	—	5.5	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 150V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 120V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 30V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -30V

## Dynamic @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
g <sub>fs</sub>	Forward Transconductance	11	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 14A
Q <sub>g</sub>	Total Gate Charge	—	37	56	nC	I <sub>D</sub> = 14A V <sub>DS</sub> = 120V V <sub>GS</sub> = 10V, ④
Q <sub>gs</sub>	Gate-to-Source Charge	—	9.6	14		
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	19	29		
t <sub>d(on)</sub>	Turn-On Delay Time	—	10	—	ns	V <sub>DD</sub> = 75V I <sub>D</sub> = 14A R <sub>G</sub> = 5.1Ω V <sub>GS</sub> = 10V ④
t <sub>r</sub>	Rise Time	—	32	—		
t <sub>d(off)</sub>	Turn-Off Delay Time	—	18	—		
t <sub>f</sub>	Fall Time	—	8.4	—		
C <sub>iss</sub>	Input Capacitance	—	1200	—	pF	V <sub>GS</sub> = 0V V <sub>DS</sub> = 25V f = 1.0MHz⑥
C <sub>oss</sub>	Output Capacitance	—	260	—		
C <sub>rss</sub>	Reverse Transfer Capacitance	—	65	—		
C <sub>oss</sub>	Output Capacitance	—	1520	—		
C <sub>oss</sub>	Output Capacitance	—	120	—		
C <sub>oss eff.</sub>	Effective Output Capacitance	—	210	—		

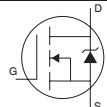
## Avalanche Characteristics

	Parameter	Typ.	Max.	Units
E <sub>AS</sub>	Single Pulse Avalanche Energy②	—	260	mJ
I <sub>AR</sub>	Avalanche Current①	—	14	A
E <sub>AR</sub>	Repetitive Avalanche Energy①	—	13.6	mJ

## Thermal Resistance

	Parameter	Typ.	Max.	Units
R <sub>θJC</sub>	Junction-to-Case	—	1.1	°C/W
R <sub>θCS</sub>	Case-to-Sink, Flat, Greased Surface ⑥	0.50	—	
R <sub>θJA</sub>	Junction-to-Ambient⑥	—	62	
R <sub>θJA</sub>	Junction-to-Ambient⑦	—	40	

## Diode Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	23	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	92		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 14A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	150	220	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 14A
Q <sub>rr</sub>	Reverse Recovery Charge	—	0.8	1.2	μC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

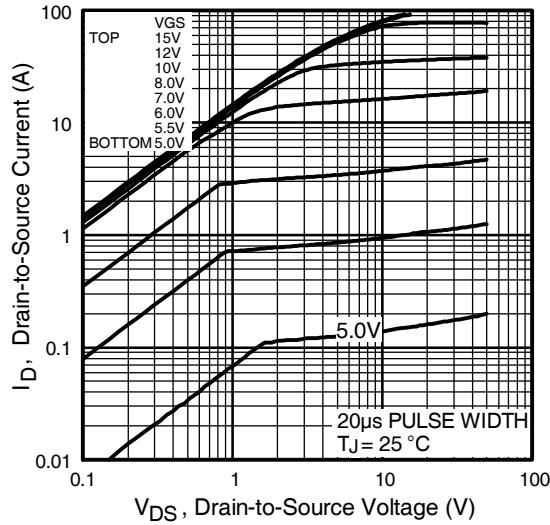


Fig 1. Typical Output Characteristics

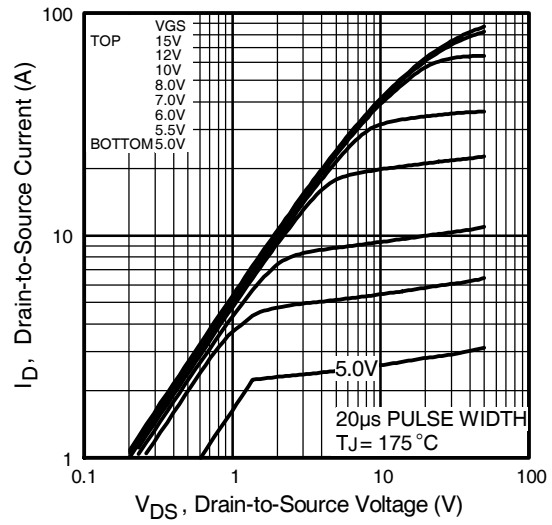


Fig 2. Typical Output Characteristics

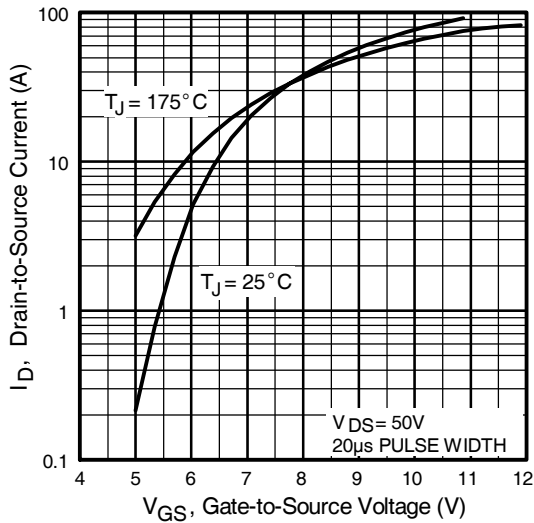


Fig 3. Typical Transfer Characteristics

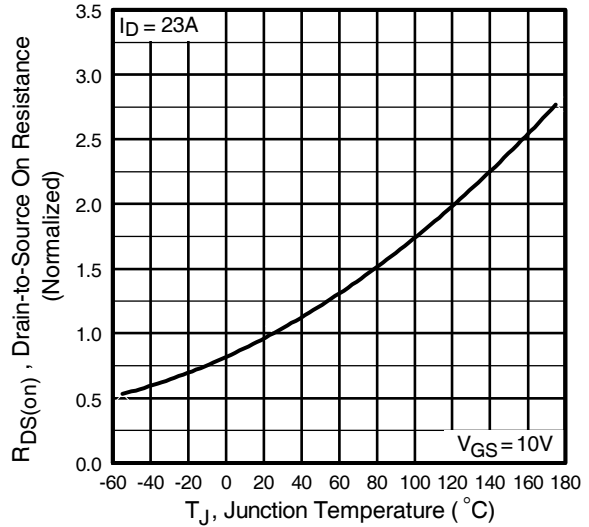
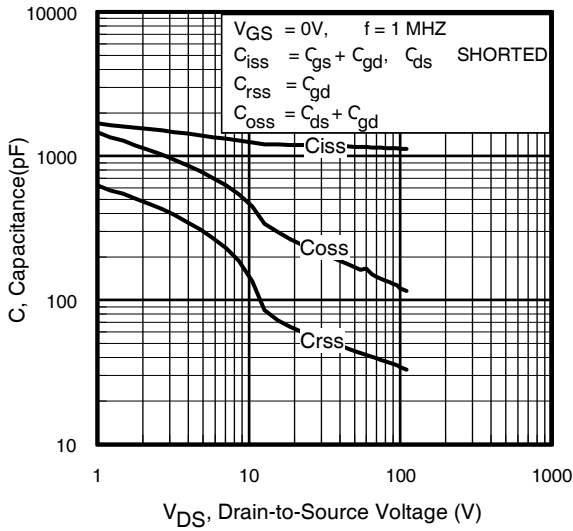
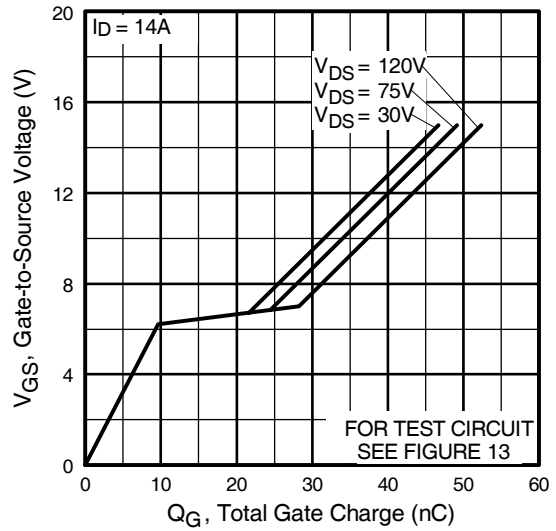


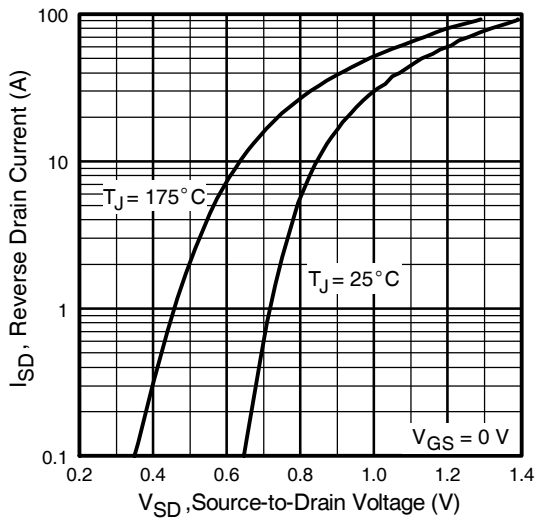
Fig 4. Normalized On-Resistance Vs. Temperature



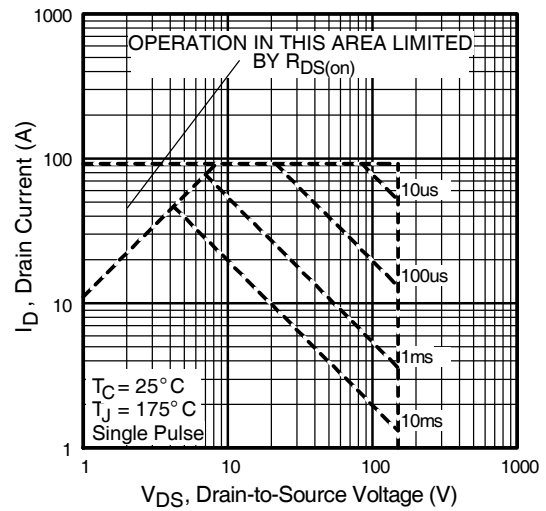
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



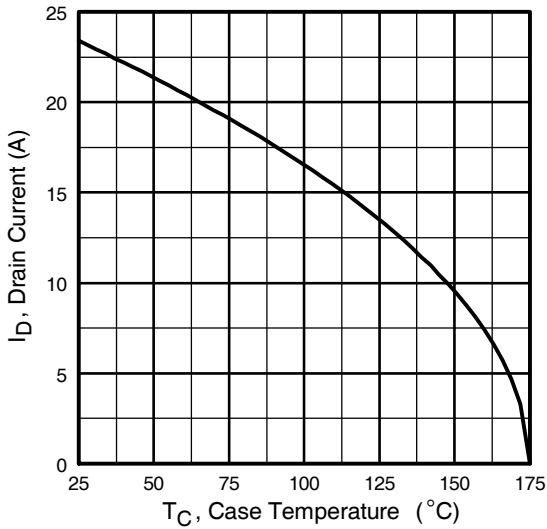
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



**Fig 7.** Typical Source-Drain Diode Forward Voltage



**Fig 8.** Maximum Safe Operating Area



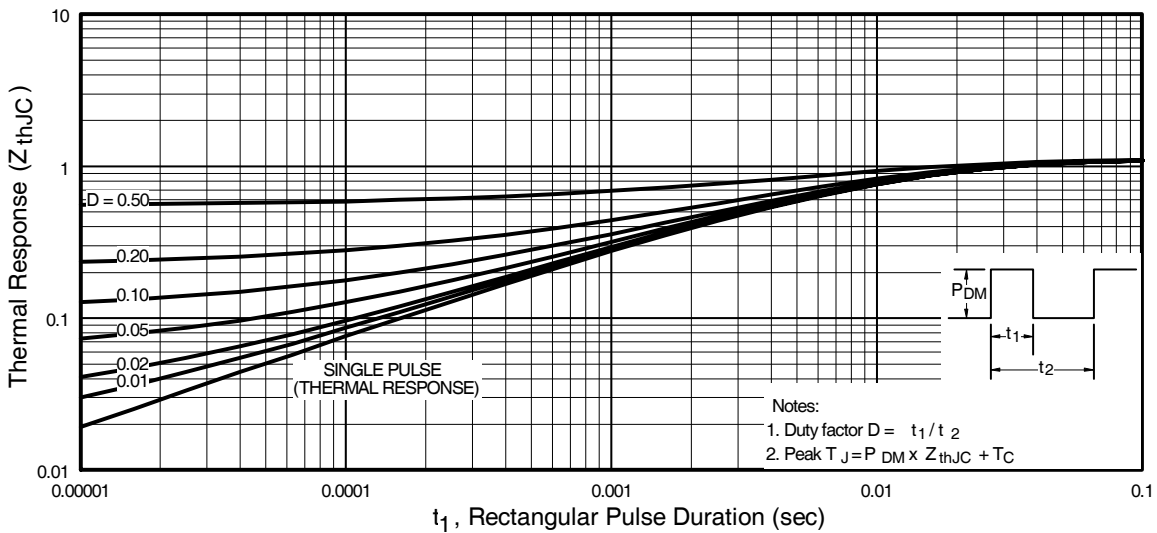
**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10a.** Switching Time Test Circuit



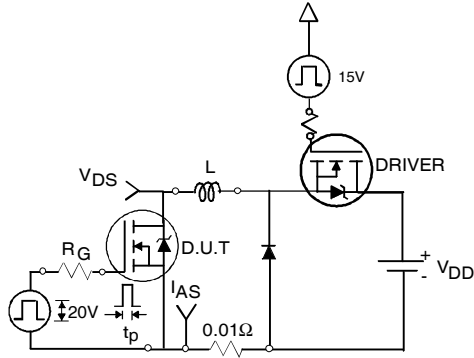
**Fig 10b.** Switching Time Waveforms



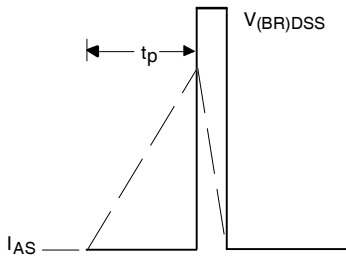
**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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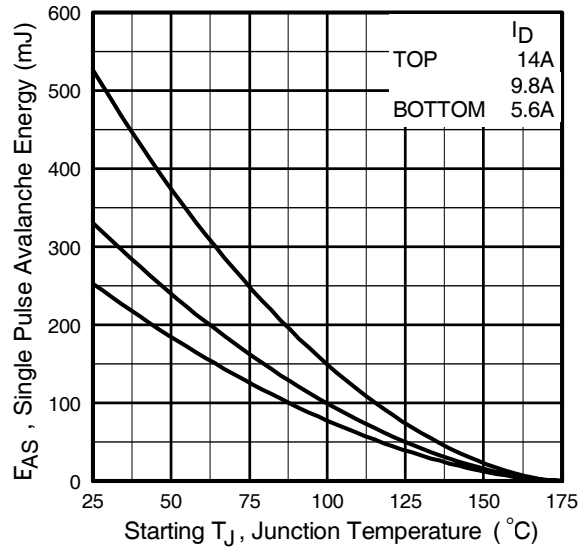
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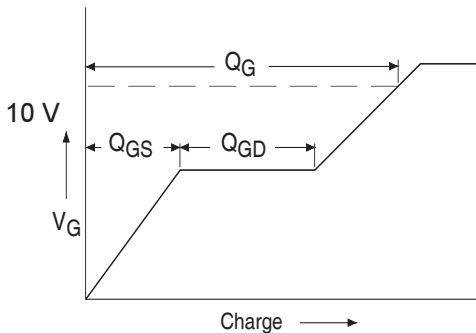
**Fig 12a.** Unclamped Inductive Test Circuit



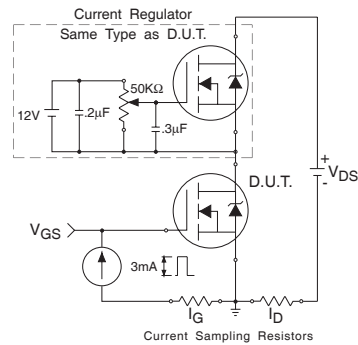
**Fig 12b.** Unclamped Inductive Waveforms



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current

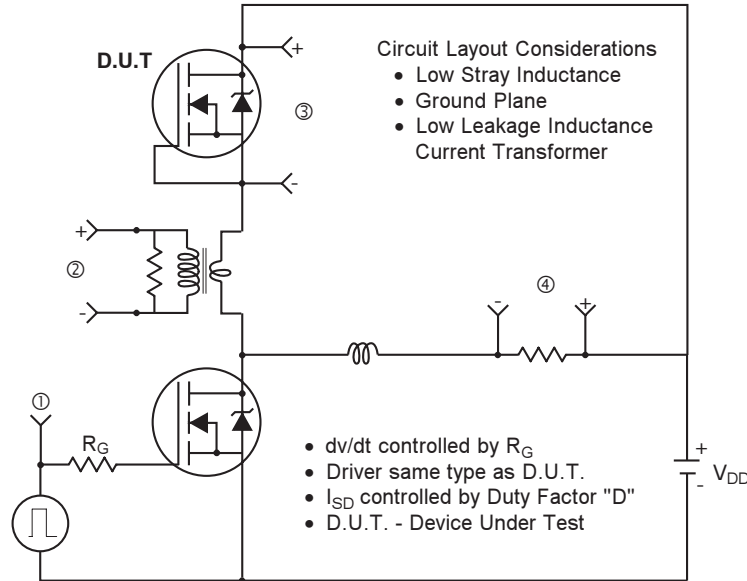


**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit

## Peak Diode Recovery dv/dt Test Circuit

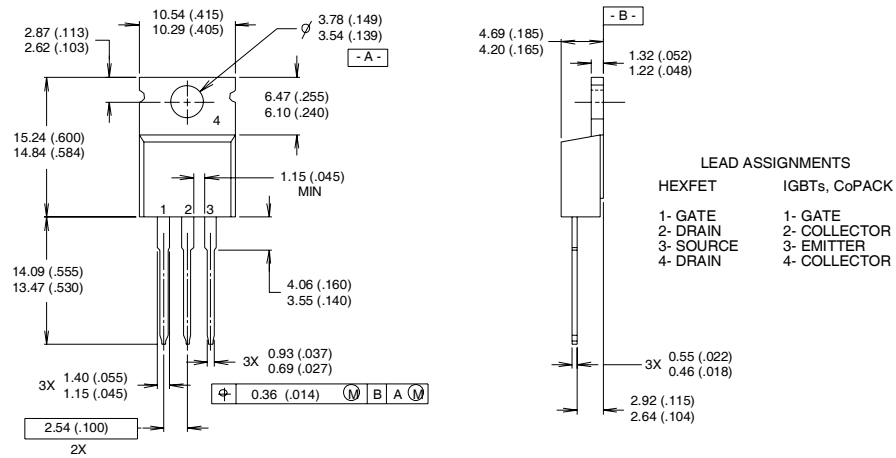


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® Power MOSFETs

## TO-220AB Package Outline

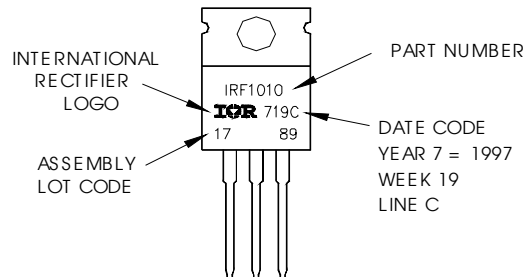
Dimensions are shown in millimeters (inches)



- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION : INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

## TO-220AB Part Marking Information

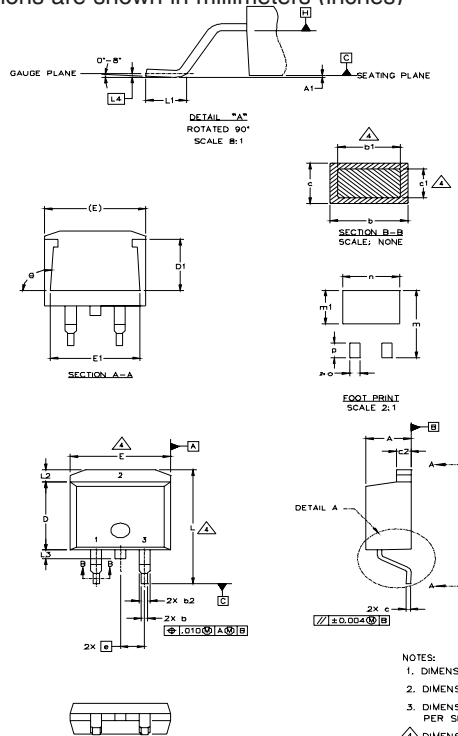
EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line  
 position indicates "Lead-Free"





## D<sup>2</sup>Pak Package Outline

Dimensions are shown in millimeters (inches)



SYMBOL	DIMENSIONS				UNIT
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	4.06	4.83	.160	.190	4
A1		0.127		.005	
b	0.51	0.99	.020	.039	
b1	0.51	0.89	.020	.035	
b2	1.14	1.40	.045	.055	4
c	0.43	0.63	.017	.025	
c1	0.38	0.74	.015	.029	
c2	1.14	1.40	.045	.055	
D	8.51	9.65	.335	.380	3
D1	5.33		.210		
E	9.65	10.67	.380	.420	3
E1	6.22		.245		
e	2.54 BSC		.100 BSC		
L	14.61	15.88	.575	.625	
L1	1.78	2.79	.070	.110	
L2		1.65		.065	
L3	1.27	1.78	.050	.070	
L4	0.25 BSC		.010 BSC		
m	17.78		.700		
m1	8.89		.350		
n	11.43		.450		
o	2.08		.082		
p	3.81		.150		
θ	90°	93°	90°	93°	

**LEAD ASSIGNMENTS**

<b>HEXFET</b>	<b>IGBTs_CoPACK</b>	<b>DIODES</b>
1.- GATE	1.- GATE	1.- ANODE *
2.- DRAIN	2.- COLLECTOR	2.- CATHODE
3.- SOURCE	3.- EMITTER	3.- ANODE

\* PART DEPENDENT.

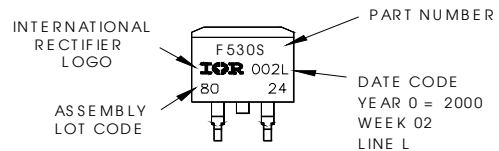
**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994
2. DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES]
3. DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.127 [005"] PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTMOST EXTREMES OF THE PLASTIC BODY.
4. DIMENSION b1 AND c1 APPLY TO BASE METAL ONLY.
5. CONTROLLING DIMENSION: INCH.

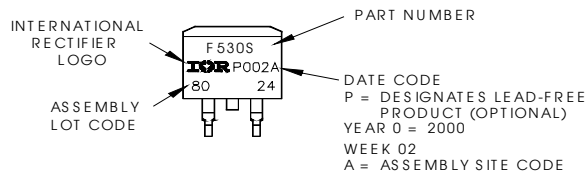
## D<sup>2</sup>Pak Part Marking Information (Lead-Free)

EXAMPLE: THIS IS AN IRF530S WITH  
LOT CODE 8024  
ASSEMBLED ON WW 02, 2000  
IN THE ASSEMBLY LINE "L"

Note: "P" in assembly line  
position indicates "Lead-Free"



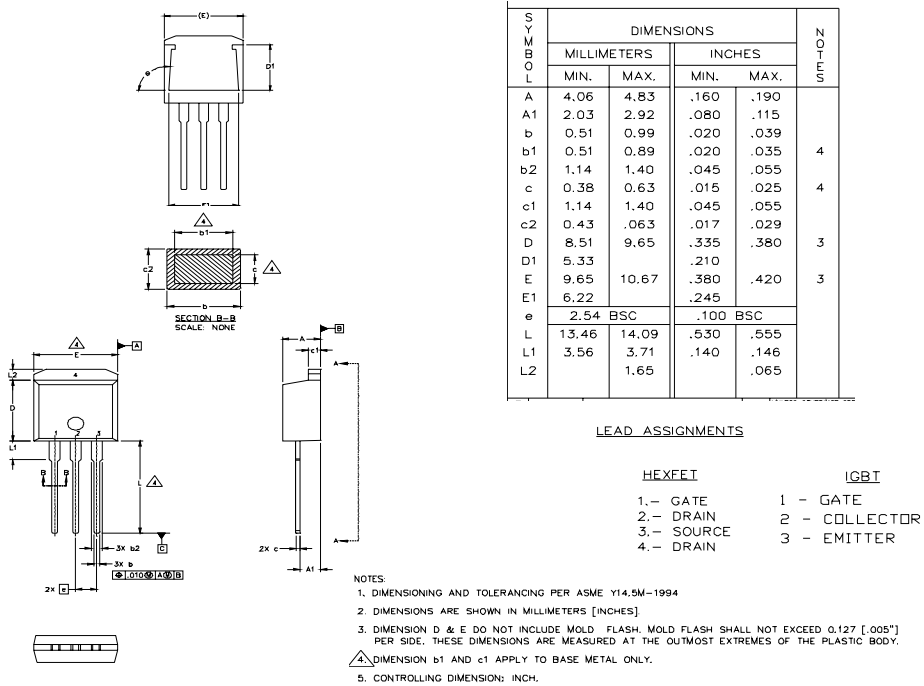
## OR



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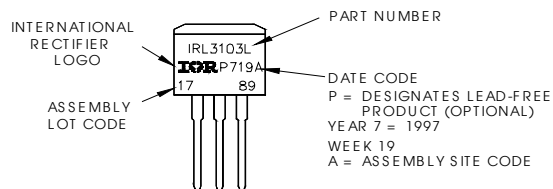
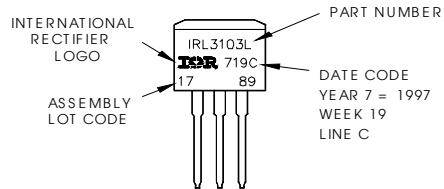
## TO-262 Package Outline



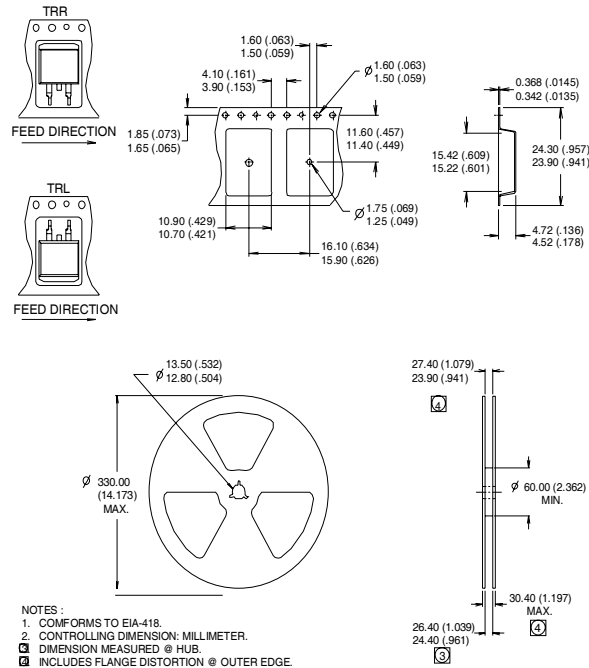
## TO-262 Part Marking Information

EXAMPLE: THIS IS AN IRL3103L  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
 Note: "P" in assembly line position indicates "Lead-Free"

**OR**



## D<sup>2</sup>Pak Tape & Reel Information



### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② Starting  $T_J = 25^\circ\text{C}$ ,  $L = 2.7\text{mH}$   
 $R_G = 25\Omega$ ,  $I_{AS} = 14\text{A}$ .
- ③  $I_{SD} \leq 14\text{A}$ ,  $di/dt \leq 240\text{A}/\mu\text{s}$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  
 $T_J \leq 175^\circ\text{C}$
- ④ Pulse width  $\leq 300\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- ⑤  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$
- ⑥ This is only applied to TO-220AB package
- ⑦ This is applied to D<sup>2</sup>Pak, when mounted on 1" square PCB ( FR-4 or G-10 Material ).  
 For recommended footprint and soldering techniques refer to application note #AN-994.

Data and specifications subject to change without notice.

International  
**IR** Rectifier

**IR WORLD HEADQUARTERS:** 233 Kansas St., El Segundo, California 90245, USA Tel: (310) 252-7105  
 TAC Fax: (310) 252-7903

Visit us at [www.irf.com](http://www.irf.com) for sales contact information.07/04

Note: For the most current drawings please refer to the IR website at:  
<http://www.irf.com/package/>

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