

General Description

The WSF3013B is the highest performance trench N-ch and P-ch MOSFETs with extreme high cell density, which provide excellent RDSON and gate charge for most of the synchronous buck converter applications.

The WSF3013B meet the RoHS and Green Product requirement 100% EAS guaranteed with full function reliability approved.

Features

- Advanced high cell density Trench technology
- Super Low Gate Charge
- Excellent CdV/dt effect decline
- 100% EAS Guaranteed
- Green Device Available

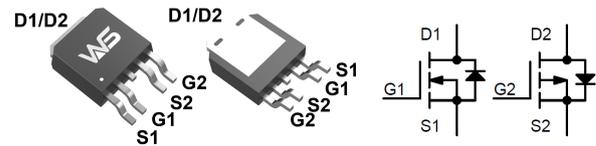
Product Summary

BVDSS	RDSON	ID
30V	15mΩ	22A
-30V	25mΩ	-19A

Applications

- High Frequency Point-of-Load Synchronous Buck Converter for MB/NB/UMPC/VGA
- Networking DC-DC Power System
- CCFL Back-light Inverter

TO-252-4L Pin Configuration



Absolute Maximum Ratings

Symbol	Parameter	Rating		Units
		N-Ch	P-Ch	
V_{DS}	Drain-Source Voltage	30	-30	V
V_{GS}	Gate-Source Voltage	± 20	± 20	V
I_D	Continuous Drain Current, $V_{GS(NP)}=10V, T_c=25^\circ C$	22	-19	A
	Continuous Drain Current, $V_{GS(NP)}=10V, T_c=100^\circ C$	10	-8	A
I_{DP}^a	Pulse Drain Current Tested, $V_{GS(NP)}=10V$	52	-45	A
E_{AS}^c	Avalanche Energy, Single pulse, L=0.5mH	22	45	mJ
I_{AS}^c	Avalanche Current, Single pulse, L=0.5mH	21	-30	A
P_D	Total Power Dissipation, $T_c=25^\circ C$	18	18	W
T_{STG}	Storage Temperature Range	-55 to 150	-55 to 150	$^\circ C$
T_J	Operating Junction Temperature Range	150	150	$^\circ C$
$R_{\theta JA}^b$	Thermal Resistance-Junction to Ambient, Steady State	62	62	$^\circ C/W$
$R_{\theta JC}$	Thermal Resistance-Junction to Case, Steady State	5.0	5.0	$^\circ C/W$

Note * : Max. current is limited by bonding wire.

Note a : Pulse width limited by max. junction temperature.

Note b : $R_{\theta JA}$ steady state $t=999s$. $R_{\theta JA}$ is measured with the device mounted on 1in², FR-4 board with 2oz. Copper.

Note c : UIS tested and pulse width limited by maximum junction temperature 150 $^\circ C$ (initial temperature $T_J=25^\circ C$).

N-Electrical Characteristics (T_J=25 °C, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV _{DSS}	Drain-Source Breakdown Voltage	V _{GS} =0V, I _D =250uA	30	---	---	V
R _{DS(ON)} ^d	Static Drain-Source On-Resistance	V _{GS} =10V, I _D =10A	---	15	22	mΩ
		V _{GS} =4.5V, I _D =5A	---	20	30	
V _{GS(th)}	Gate Threshold Voltage	V _{GS} =V _{DS} , I _D =250uA	1.0	1.6	2.5	V
I _{DSS}	Drain-Source Leakage Current	V _{DS} =20V, V _{GS} =0V, T _J =25°C	---	---	1	uA
		V _{DS} =20V, V _{GS} =0V, T _J =85°C	---	---	30	
I _{GSS}	Gate-Source Leakage Current	V _{GS} =±20V, V _{DS} =0V	---	---	±100	nA
R _g	Gate Resistance	V _{DS} =0V, V _{GS} =0V, f=1MHz	---	2.5	5.0	Ω
Q _g ^e	Total Gate Charge	V _{DS} =20V, V _{GS} =4.5V, I _{DS} =10A	---	7.2	---	nC
Q _{gs} ^e	Gate-Source Charge		---	1.4	---	
Q _{gd} ^e	Gate-Drain Charge		---	2.2	---	
T _{d(on)} ^e	Turn-On Delay Time	V _{DD} =15V, I _{DS} =5A, V _{GS} =10V, R _G =3.3R.	---	4.1	---	ns
T _r ^e	Rise Time		---	9.8	---	
T _{d(off)} ^e	Turn-Off Delay Time		---	15.5	---	
T _f ^e	Fall Time		---	6.0	---	
C _{iss} ^e	Input Capacitance	V _{DS} =15V, V _{GS} =0V, f=1MHz	---	572	---	pF
C _{oss} ^e	Output Capacitance		---	81	---	
C _{rss} ^e	Reverse Transfer Capacitance		---	65	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I _S	Continuous Source Current	V _G =V _D =0V, Force Current	---	---	10	A
V _{SD} ^d	Diode Forward Voltage	V _{GS} =0V, I _S =1A, T _J =25°C	---	---	1.2	V

Note d : Pulse test ; pulse width≤300μs, duty cycle≤2%.

Note e : Guaranteed by design, not subject to production testing.

P-Channel Electrical Characteristics ($T_J=25^\circ\text{C}$, unless otherwise noted)

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS}=0V, I_D=-250\mu A$	-30	---	---	V
$R_{DS(ON)}^d$	Static Drain-Source On-Resistance	$V_{GS}=-10V, I_D=-7A$	---	25	33	m Ω
		$V_{GS}=-4.5V, I_D=-5A$	---	37	54	
$V_{GS(th)}$	Gate Threshold Voltage	$V_{GS}=V_{DS}, I_D=-250\mu A$	-1.0	---	-2.8	V
I_{DSS}	Drain-Source Leakage Current	$V_{DS}=-20V, V_{GS}=0V, T_J=25^\circ\text{C}$	---	---	-1	μA
		$V_{DS}=-20V, V_{GS}=0V, T_J=85^\circ\text{C}$	---	---	-30	
I_{GSS}	Gate-Source Leakage Current	$V_{GS}=\pm 20V, V_{DS}=0V$	---	---	± 100	nA
Q_g^e	Total Gate Charge	$V_{DS}=-15V, V_{GS}=-4.5V, I_D=-12A$	---	9.8	---	nC
Q_{gs}^e	Gate-Source Charge		---	2.2	---	
Q_{gd}^e	Gate-Drain Charge		---	3.4	---	
$T_{d(on)}^e$	Turn-On Delay Time	$V_{DD}=-15V, V_{GS}=-10V, R_G=6\Omega, I_D=-1A, R_L=15\Omega,$	---	16.4	---	ns
T_r^e	Rise Time		---	20.2	---	
$T_{d(off)}^e$	Turn-Off Delay Time		---	55	---	
T_f^e	Fall Time		---	10	---	
C_{iss}^e	Input Capacitance	$V_{DS}=-15V, V_{GS}=0V, f=1\text{MHz}$	---	930	---	pF
C_{oss}^e	Output Capacitance		---	148	---	
C_{rss}^e	Reverse Transfer Capacitance		---	115	---	

Diode Characteristics

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
I_S	Continuous Source Current	$V_G=V_D=0V$, Force Current	---	---	-8	A
V_{SD}^e	Diode Forward Voltage	$V_{GS}=0V, I_S=-1A, T_J=25^\circ\text{C}$	---	---	-1.2	V

Note d : Pulse test; pulse width $\leq 300\mu s$, duty cycle $\leq 2\%$.

Note e : Guaranteed by design, not subject to production testing.

N-Channel Typical Characteristics

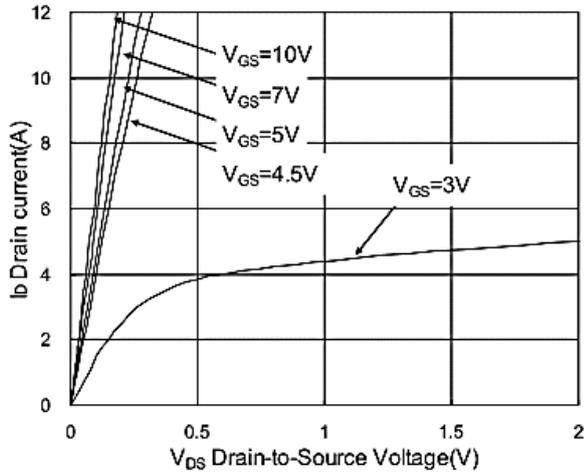


Fig.1 Typical Output Characteristics

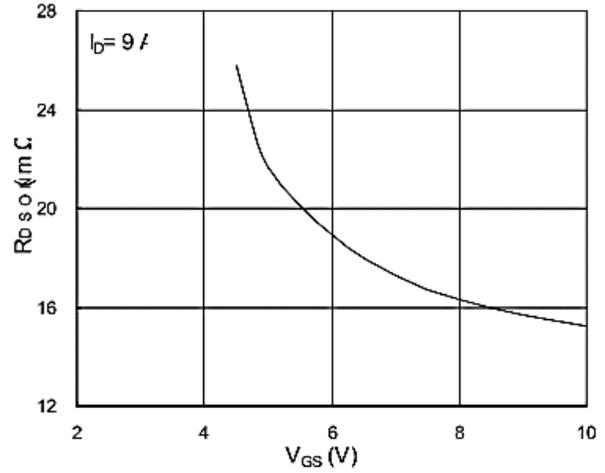


Fig.2 On-Resistance v.s Gate-Source

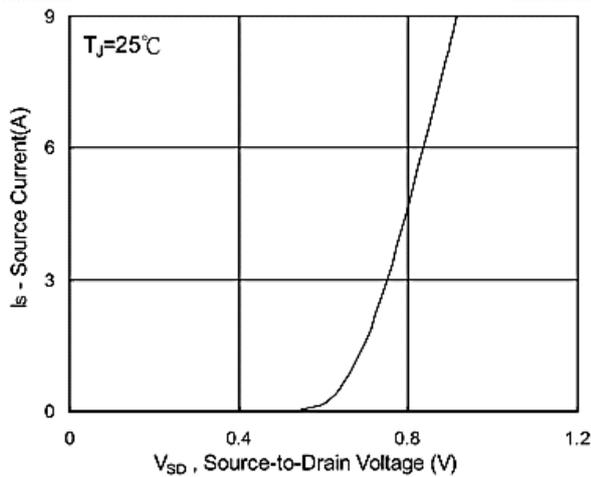


Fig.3 Forward Characteristics Of Reverse

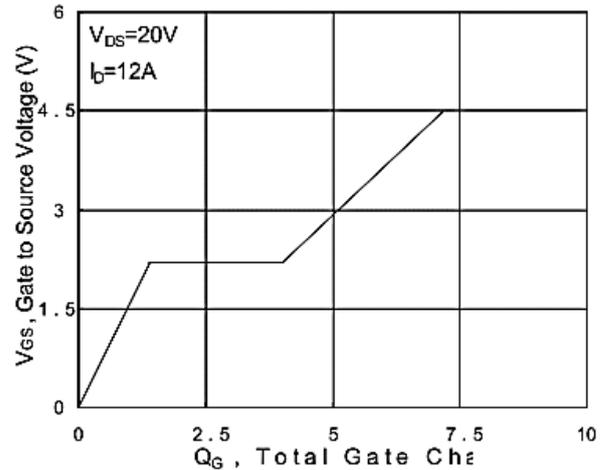


Fig.4 Gate-Charge characteristics

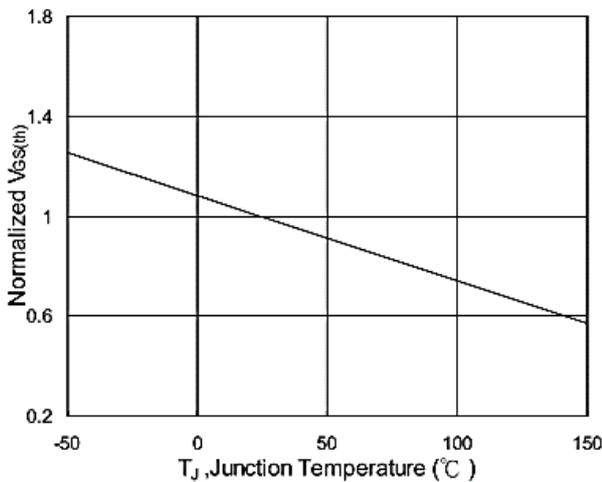


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

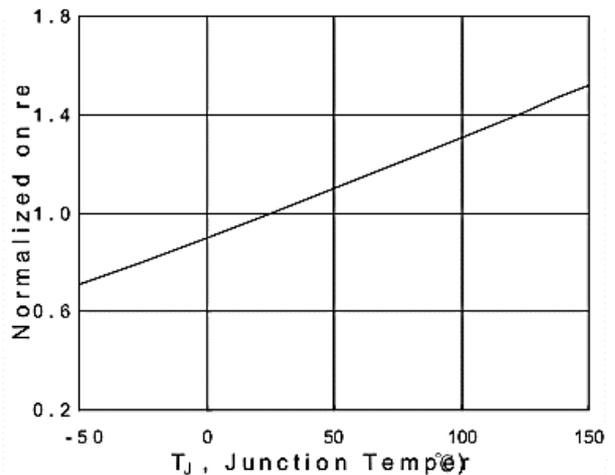


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

N-Channel Typical Characteristics

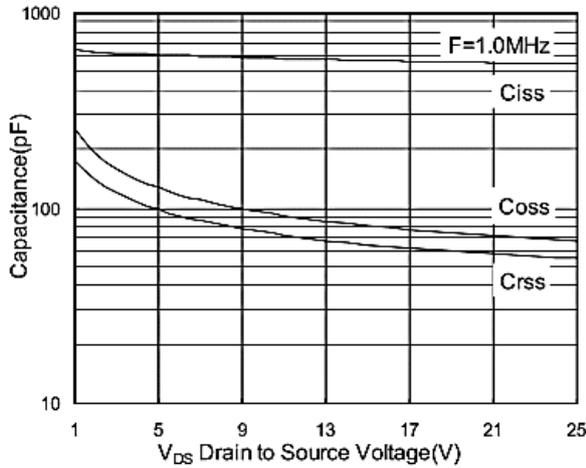


Fig.7 Capacitance

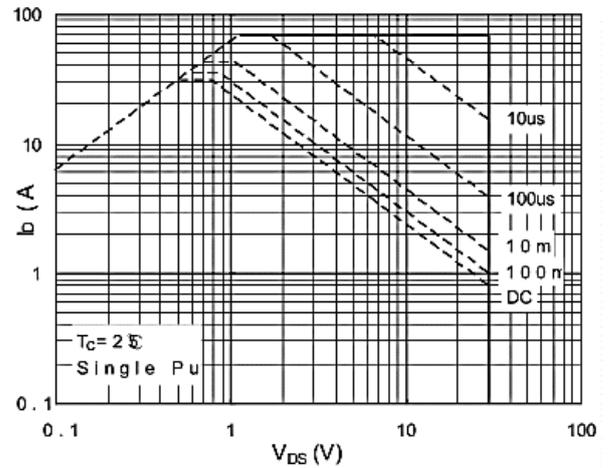


Fig.8 Safe Operating Area

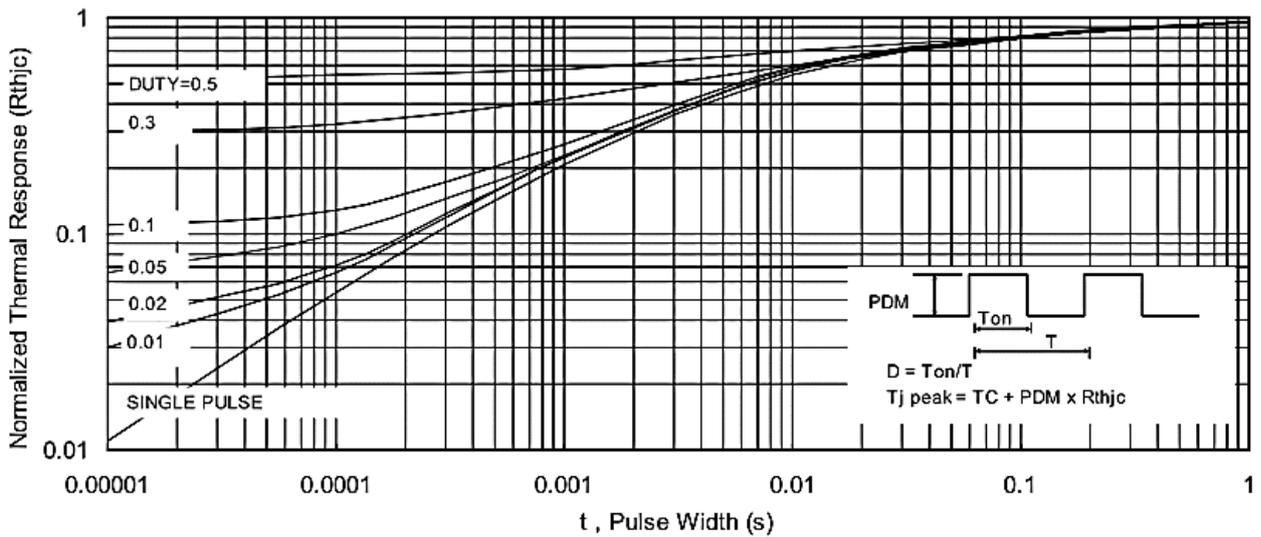


Fig.9 Normalized Maximum Transient Thermal Impedance

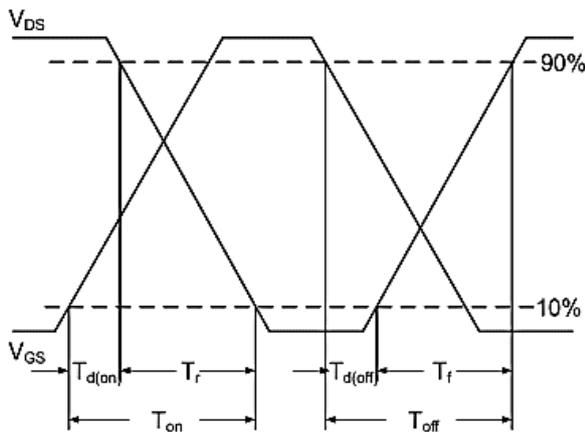


Fig.10 Switching Time Waveform

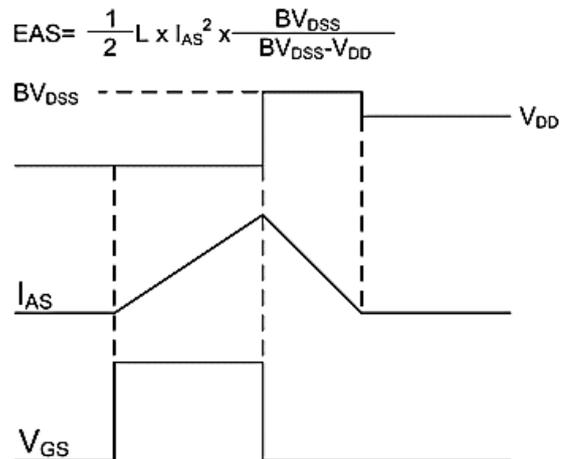


Fig.11 Unclamped Inductive Waveform

P-Channel Typical Characteristics

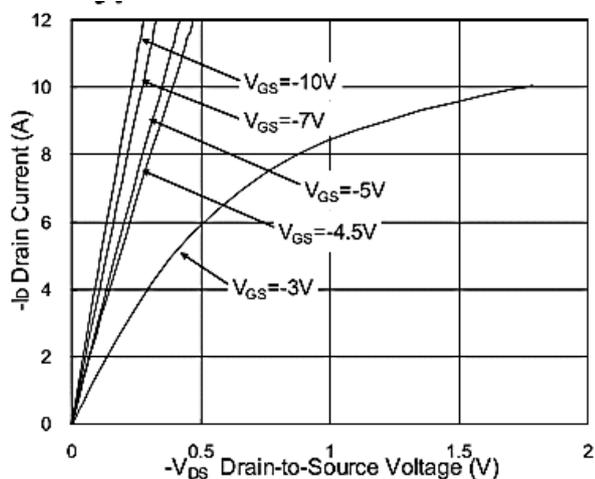


Fig.1 Typical Output Characteristics

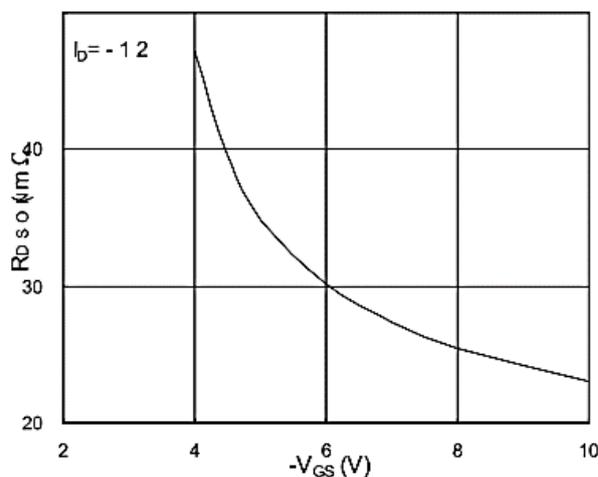


Fig.2 On-Resistance v.s Gate-Source

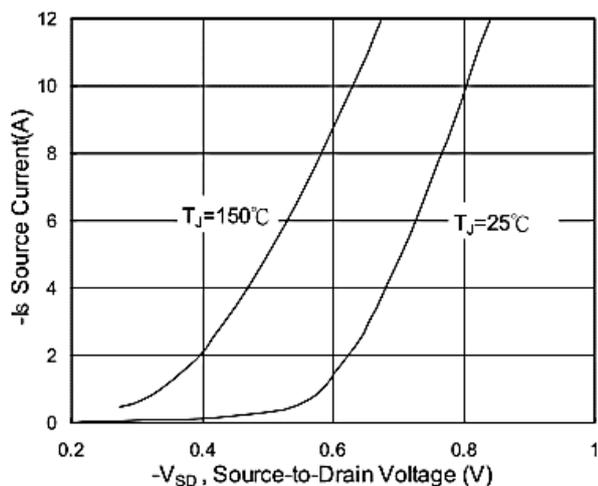


Fig.3 Forward Characteristics Of Reverse

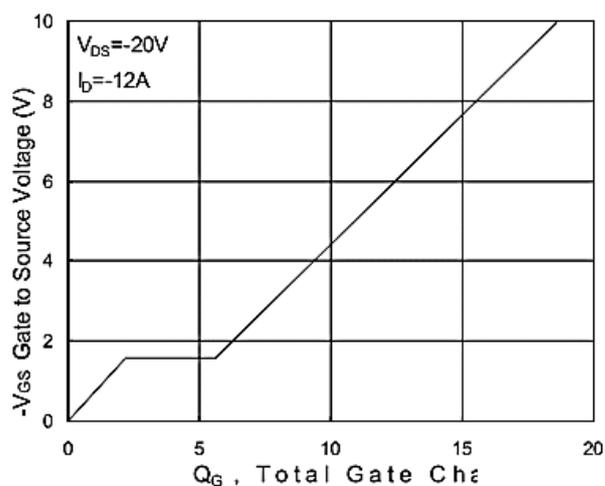


Fig.4 Gate-Charge Characteristics

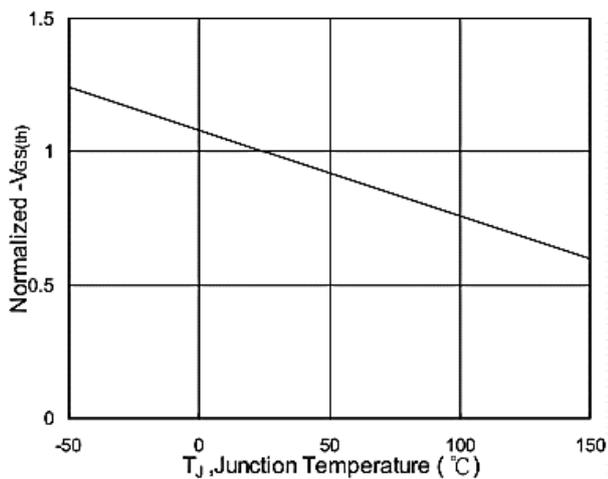


Fig.5 Normalized $V_{GS(th)}$ v.s T_J

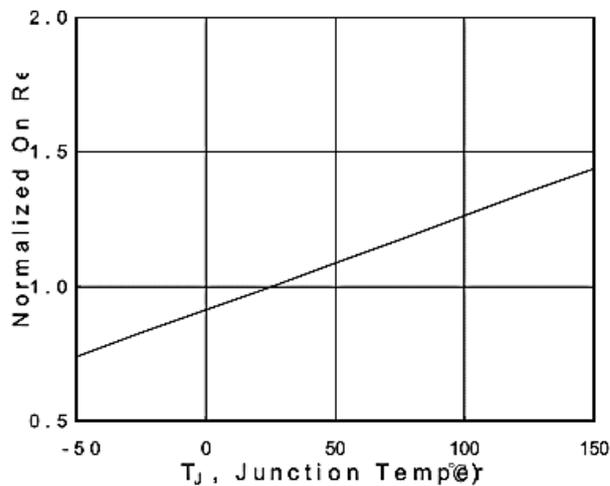


Fig.6 Normalized $R_{DS(on)}$ v.s T_J

P-Channel Typical Characteristics

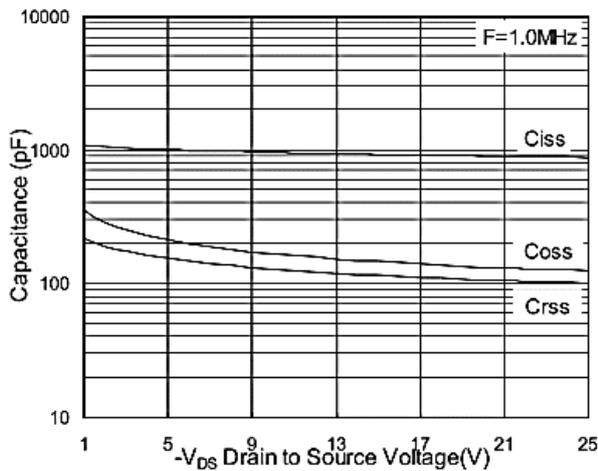


Fig.7 Capacitance

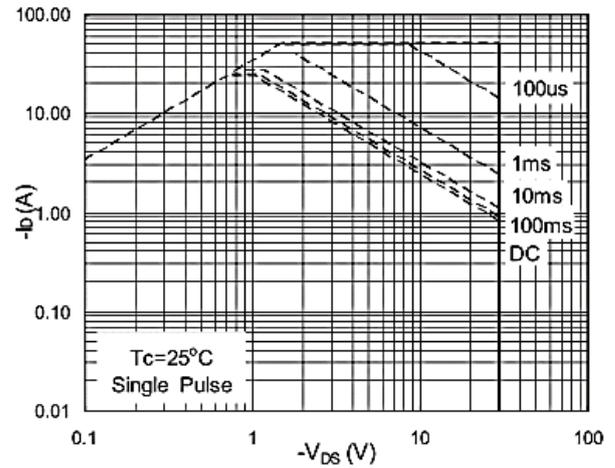


Fig.8 Safe Operating Area

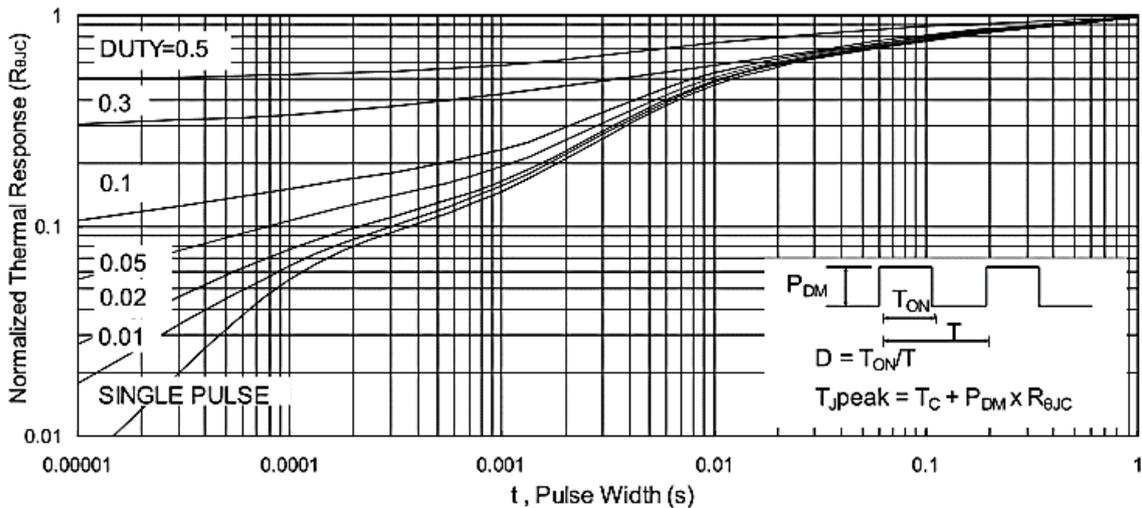


Fig.9 Normalized Maximum Transient Thermal Impedance

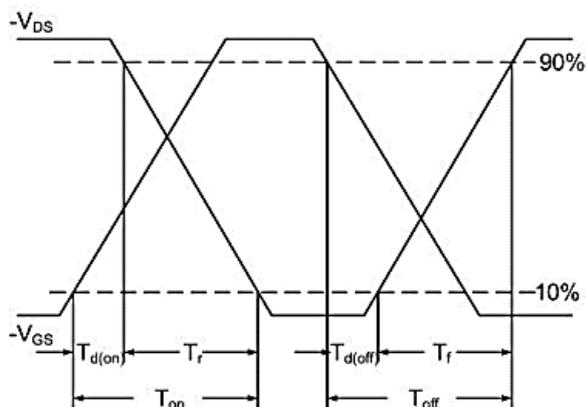


Fig.10 Switching Time Waveform

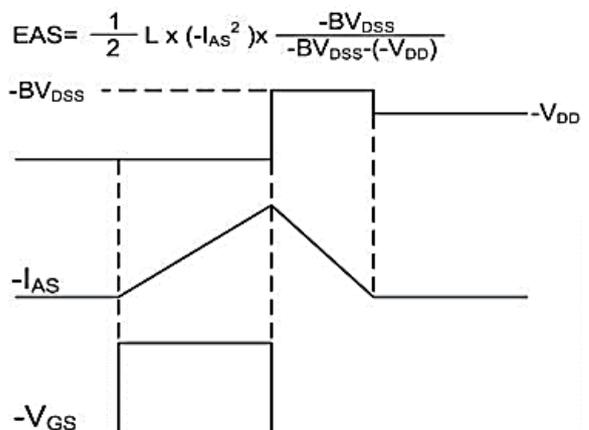


Fig.11 Unclamped Inductive Waveform

$$EAS = \frac{1}{2} L \times (-I_{AS}^2) \times \frac{-BV_{DSS}}{-BV_{DSS} - (-V_{DD})}$$



Attention

- 1, Any and all Winsok power products described or contained herein do not have specifications that can handle applications that require extremely high levels of reliability, such as life-support systems, aircraft's control systems, or other applications whose failure can be reasonably expected to result in serious physical and/or material damage. Consult with your Winsok power representative nearest you before using any Winsok power products described or contained herein in such applications.
- 2, Winsok power assumes no responsibility for equipment failures that result from using products at values that exceed, even momentarily, rated values (such as maximum ratings, operating condition ranges, or other parameters) listed in products specifications of any and all Winsok power products described or contained herein.
- 3, Specifications of any and all Winsok power products described or contained herein stipulate the performance, characteristics, and functions of the described products in the independent state, and are not guarantees of the performance, characteristics, and functions of the described products as mounted in the customer's products or equipment. To verify symptoms and states that cannot be evaluated in an independent device, the customer should always evaluate and test devices mounted in the customer's products or equipment.
- 4, Winsok power Semiconductor CO., LTD. strives to supply high-quality high-reliability products. However, any and all semiconductor products fail with some probability. It is possible that these probabilistic failures could give rise to accidents or events that could endanger human lives that could give rise to smoke or fire, or that could cause damage to other property. When designing equipment, adopt safety measures so that these kinds of accidents or events cannot occur. Such measures include but are not limited to protective circuits and error prevention circuits for safe design, redundant design, and structural design.
- 5, In the event that any or all Winsok power products (including technical data, services) described or contained herein are controlled under any of applicable local export control laws and regulations, such products must not be exported without obtaining the export license from the authorities concerned in accordance with the above law.
- 6, No part of this publication may be reproduced or transmitted in any form or by any means, electronic or mechanical, including photocopying and recording, or any information storage or retrieval system, or otherwise, without the prior written permission of Winsok power Semiconductor CO., LTD.
- 7, Information (including circuit diagrams and circuit parameters) herein is for example only; it is not guaranteed for volume production. Winsok power believes information herein is accurate and reliable, but no guarantees are made or implied regarding its use or any infringements of intellectual property rights or other rights of third parties.
- 8, Any and all information described or contained herein are subject to change without notice due to product/technology improvement, etc. When designing equipment, refer to the "Delivery Specification" for the Winsok power product that you intend to use.
- 9, this catalog provides information as of Sep. 2014. Specifications and information herein are subject to change without notice.