- **Integrated Asynchronous Communications Element Compatible With PCMCIA PC Card Standard Release 2.01**
- **Consists of a Single TL16C550 ACE Plus PCMCIA Interface Logic**
- **Provides Common I Bus/Z Bus Microcontroller Inputs for Most Intel™ and Zilog™ Subsystems**
- **Fully Programmable 256-Byte Card Information Structure and 8-Byte Card Configuration Register**
- **Adds or Deletes Standard Asynchronous Communication Bits (Start, Stop and Parity) to or From Serial Data Stream**
- **Transmit, Receive, Line Status, and Data Set Interrupts Independently Controlled**
- **Selectable Serial Bypass Mode Provides Subsystem With Direct Parallel Access to the FIFOs**
- **Fully Programmable Serial Interface Characteristics:**
  - **5-, 6-, 7-, or 8-Bit Characters**
  - **Even-, Odd-, or No-Parity Bit Generation and Detection**
  - **1-, 1 1/2-, or 2-Stop Bit Generation**
  - **Baud Rate Generation**
- **Fully Prioritized Interrupt System Controls**
- **Modem Control Functions**
- **Provides TL16C450 Mode at Reset Plus Selectable Normal TL16C550 Operation or Extended 64-Byte FIFO Mode**
- **Selectable Auto-$\overline{\text{RTS}}$ Mode Deactivates $\overline{\text{RTS}}$ at 14 Bytes in 550 Mode and at 56 Bytes in Extended 550 Mode**
- **Selectable Auto-$\overline{\text{CTS}}$ Mode Deactivates Serial Transfers When $\overline{\text{CTS}}$ is Inactive**

description

The TL16PC564A† is designed to provide all the functions necessary for a Personal Computer Memory Card International Association (PCMCIA) universal asynchronous receiver transmitter (UART) subsystem interface. This interface provides a serial-to-parallel conversion for data to and from a modem coder decoder/digital signal processor (CODEC/DSP) function to a PCMCIA parallel data port format. A computer central processing unit (CPU), through a PCMCIA host controller, can read the status of the asynchronous communications element (ACE) interface at any point in the operation. Reported status information includes the type of transfer operation in process, the status of the operation, and any error conditions encountered.

Attribute memory consists of a 256-byte card information structure (CIS) and eight 8-byte card configuration registers (CCR). The CIS, implemented with a dual port random access memory (DPRAM), is available to both the host CPU and subsystem (modem), as are the CCRs. This DPRAM is used in place of the electrically erasable programmable read-only memory (EEPROM) normally used for the CIS. At power up, attribute memory is initialized by the subsystem.

The TL16PC564A uses a TL16C550 ACE-type core with an expanded 64 × 11 receiver first-in-first-out (FIFO) memory and a 64 × 8 transmitter FIFO memory. The receiver trigger logic flags have been adjusted in order to take full advantage of the increased capacity when in the extended mode. In addition, eight of the UART registers have been mapped into the subsystem (modem) memory space as read-only registers. This allows the subsystem to read UART status information.

A subsystem selectable serial bypass mode has been implemented to allow the subsystem to bypass the serial portion of the UART and write directly to the receiver FIFO and read directly from the transmitter FIFO. The interrupt operation is not affected in this mode.

The TL16PC564A is packaged in a 100-pin thin quad flat package (PZ).

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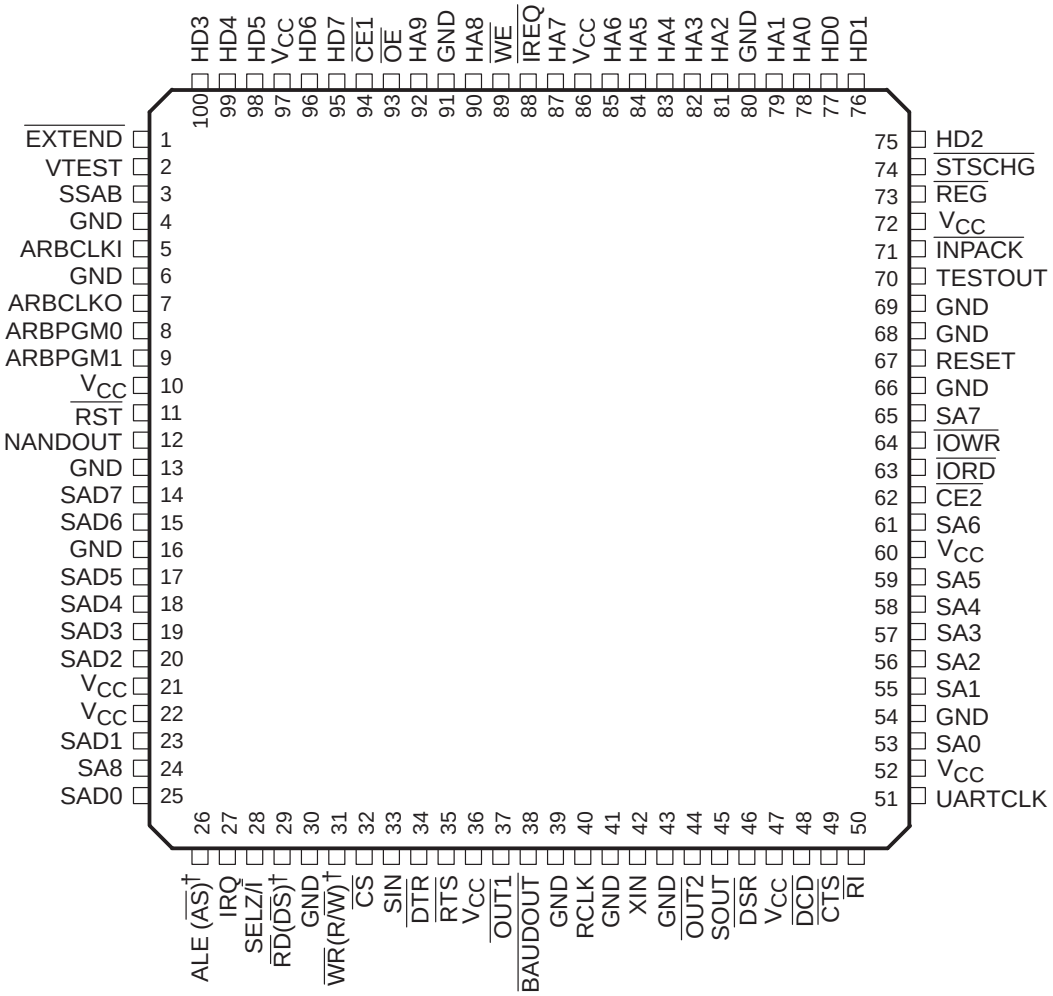
† Patent pending

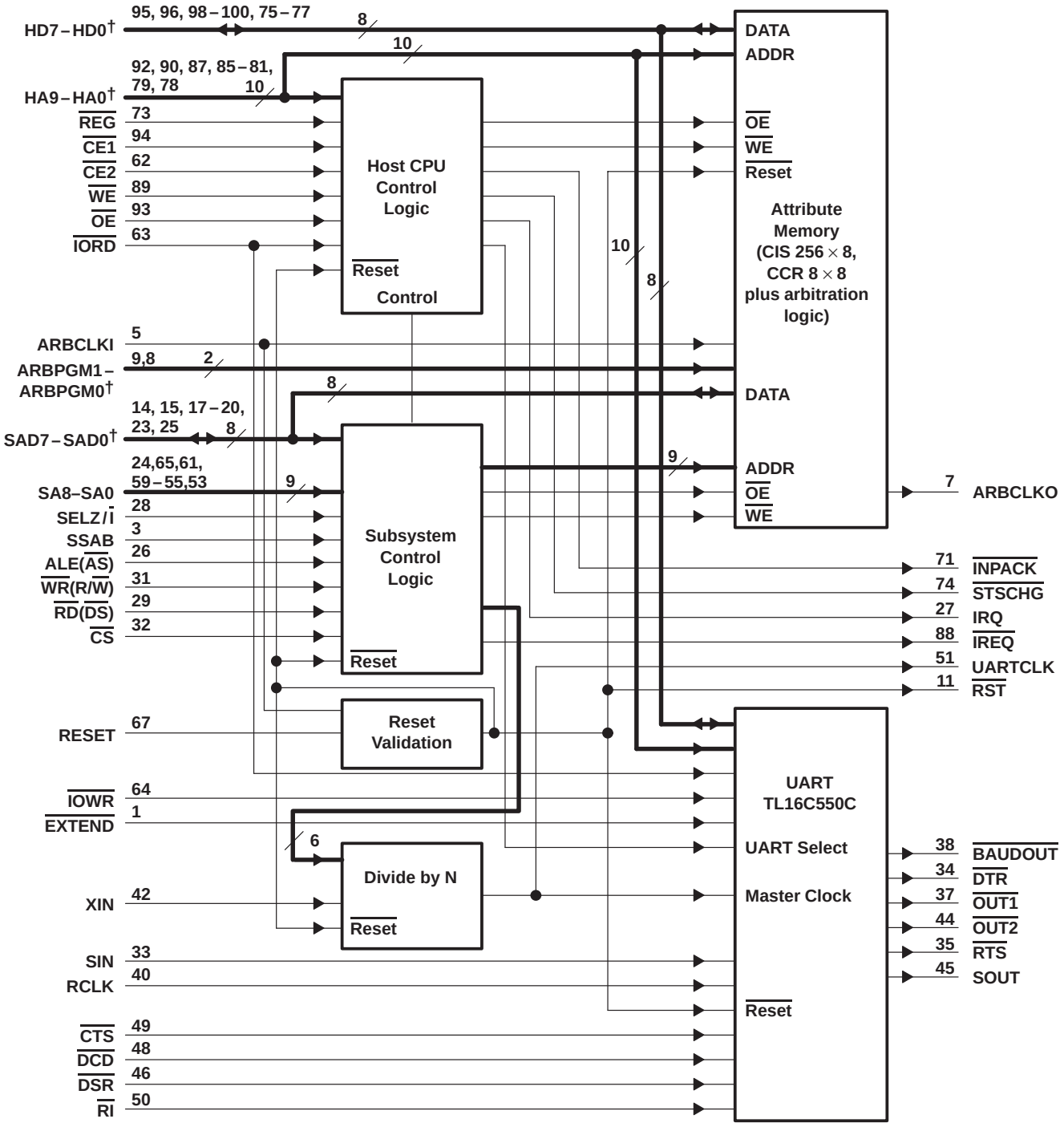
Intel is a trademark of Intel Corporation.
Zilog is a trademark of Zilog Corporation.

PZ PACKAGE
(TOP VIEW)



† The terminal names not enclosed in parentheses correspond to an Intel microcontroller signal, and the terminal names enclosed in parentheses correspond to a Zilog microcontroller signal.

block diagram



† Bit 0 is the least significant bit (LSB).

Terminal Functions

TERMINAL NAME	TERMINAL NO.	INTER-FACE†	I/O	DESCRIPTION
ALE ($\overline{AS}$)	26	S	I	Address latch enable/address strobe. ALE($\overline{AS}$) is an address latch enable in the Intel mode and an address strobe in the Zilog mode. ALE ($\overline{AS}$) is active high for an Intel subsystem and active low for a Zilog subsystem.
ARBCLKO	7	M	O	Arbitration clock output. ARBCLKO is equal to the input on ARBCLKI divided by the binary coded divisor input on ARBPGM (1–0).
ARBCLKI	5	M	I	Arbitration clock input. ARBCLKI is the base clock used in arbitration for the attribute memory DRAM and the reset validation circuitry.
ARBPGM0 ARBPGM1	8 9	M	I	Arbitration clock divisor program. These two bits set the divisor for ARBCLKI. Clock divisors 1, 2, 4, and 8 are available.
$\overline{BAUDOUT}$	38	U	O	Baud output. $\overline{BAUDOUT}$ is an active-low 16× signal for the transmitter section of the UART. The clock rate is established by the reference clock (UARTCLK) frequency divided by a divisor specified by the baud rate generator divisor latches. $\overline{BAUDOUT}$ may also be used for the receiver section by tying this output to the RCLK input.
$\overline{CE1}$ CE2	94 62	H	I	Card enable 1 and card enable 2 are active-low signals. $\overline{CE1}$ enables even numbered address bytes, and $\overline{CE2}$ enables odd numbered address bytes. A multiplexing scheme based on HA0, $\overline{CE1}$, and $\overline{CE2}$ allows an 8-bit host to access all data on HD0 through HD7 if desired. These signals have internal pullup resistors.
$\overline{CS}$	32	S	I	Chip select. $\overline{CS}$ is the active-low chip select from the Zilog or Intel microcontroller.
$\overline{CTS}$	49	U	I	Clear to send. $\overline{CTS}$ is an active-low modem status signal. Its condition can be checked by reading bit 4 (CTS) of the modem status register (MSR). Bit 0 (delta clear to send) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{CTS}$ changes states, an interrupt is generated.
DCD	48	U	I	Data carrier detect. $\overline{DCD}$ is an active-low modem status signal. Its condition can be checked by reading bit 7 (DCD) of the MSR. Bit 3 (delta data carrier detect) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DCD}$ changes states, an interrupt is generated.
$\overline{DSR}$	46	U	I	Data set ready. $\overline{DSR}$ is an active-low modem status signal. Its condition can be checked by reading bit 5 (DSR) of the MSR. Bit 1 (delta data set ready) of the MSR indicates that the signal has changed states since the last read from the MSR. If the modem status interrupt is enabled when $\overline{DSR}$ changes states, an interrupt is generated.
$\overline{DTR}$	34	U	O	Data terminal ready. $\overline{DSD}$ is an active-low signal. When active, $\overline{DTR}$ informs the modem or data set that the UART is ready to establish communication. $\overline{DTR}$ is placed in the active state by setting the DTR bit 0 of the modem control register (MCR) to a high level. $\overline{DTR}$ is placed in the inactive state either as a result of a reset, doing a loop mode operation, or clearing bit 0 (DTR) of the MCR.
$\overline{EXTEND}$	1	U	I	FIFO extend. When $\overline{EXTEND}$ is high, the UART is configured as a standard TL16C550 with 16-byte transmit and receive FIFOs. When $\overline{EXTEND}$ is low and FIFO control register (FCR) bit 5 is set, the FIFOs are extended to 64 bytes and the receiver interrupt trigger levels adjust accordingly. $\overline{EXTEND}$ low in conjunction with FCR bit 4 set high enables the auto-$\overline{RTS}$.
GND	4, 6, 13, 16, 30, 39, 41, 43, 54, 66, 68, 69, 80, 91	M		Common ground
HA0 HA1 HA2 HA3 HA4 HA5 HA6 HA7 HA8 HA9	78 79 81 82 83 84 85 87 90 92	H	I	H address bus. The 10-bit address bus addresses the attribute memory (bits 1–8) and addresses the internal UART as either PCMCIA I/O (bits 0–2) or as a standard COM port (bits 0–9).

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	INTER-FACE†	I/O	DESCRIPTION
HD0 HD1 HD2 HD3 HD4 HD5 HD6 HD7	77 76 75 100 99 98 96 95	H	I/O	H data bus. The 8-bit bidirectional data bus transfers data to and from the attribute memory and the internal UART.
$\overline{\text{INPACK}}$	71	H	O	Input port acknowledge. $\overline{\text{INPACK}}$ is an active-low output signal that is asserted when the card responds to an I/O read cycle at the address on the HA bus.
$\overline{\text{IORD}}$	63	H	I	I/O read strobe. $\overline{\text{IORD}}$ is an active-low input signal activated to read data from the card I/O space. The $\overline{\text{REG}}$ signal and at least one of the card enable inputs ($\overline{\text{CE1}}$, $\overline{\text{CE2}}$) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.
$\overline{\text{IOWR}}$	64	H	I	I/O write strobe. $\overline{\text{IORW}}$ is an active-low input signal activated to write data to the card I/O space. The $\overline{\text{REG}}$ signal and at least one of the card enable inputs ($\overline{\text{CE1}}$, $\overline{\text{CE2}}$) must also be active for the I/O transfer to take place. This signal has an internal pullup resistor.
$\overline{\text{IREQ}}$	88	H	O	Interrupt request. $\overline{\text{IREQ}}$ is an active-low output signal asserted by the card to indicate to the host CPU that a card device requires host software service. This signal doubles as the READY/BUSY signal during power-up initialization.
IRQ	27	S	O	Interrupt request. An active-high IRQ to the subsystem indicates a host CPU write to attribute memory has occurred.
NANDOUT	12	M	O	This is a production test output.
$\overline{\text{OE}}$	93	H	I	Output enable. $\overline{\text{OE}}$ is an active-low input signal that gates memory read data from the card. This signal has an internal pullup resistor.
$\overline{\text{OUT1}}$ $\overline{\text{OUT2}}$	37 44	U	O	Output 1 and output 2 are active-low signals. $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$ are user-defined output terminals that are set to their active state by setting the respective MCR bits (OUT1 and OUT2). $\overline{\text{OUT1}}$ and $\overline{\text{OUT2}}$ are set to their inactive (high) state as a result of a reset, by doing loop mode operation, or by clearing bit 2 (OUT1) or bit 3 (OUT2) of the MCR. These signals have open-drain outputs.
RCLK	40	U	I	Receiver clock. RCLK is the 16×-baud rate clock input for the receiver section of the UART.
$\overline{\text{RD}}$($\overline{\text{DS}}$)	29	S	I	Read enable or data strobe input. $\overline{\text{RD}}$($\overline{\text{DS}}$) is the active-low read enable in the Intel mode and the active-low data strobe in the Zilog mode.
$\overline{\text{REG}}$	73	H	I	Attribute memory select. This active-low input signal is generated by the host CPU and accesses attribute memory ($\overline{\text{OE}}$ and $\overline{\text{WE}}$ active) and I/O space ($\overline{\text{IORD}}$ or $\overline{\text{IOWR}}$ active). PCMCIA common memory access is excluded. This signal has an internal pullup resistor and hysteresis on the input buffer.
RESET	67	H	I	Reset. RESET is an active-high input that serves as the master reset for the device. RESET clears the UART, placing the card in an unconfigured state. This signal has an internal pullup resistor.
$\overline{\text{RI}}$	50	U	I	Ring indicator. $\overline{\text{RI}}$ is an active-low modem status signal. Its condition can be checked by reading bit 6 (RI) of the MSR. The trailing edge of ring indicator (TERI) bit 2 of the MSR indicates that $\overline{\text{RI}}$ has transitioned from a low to a high state since the last read from the MSR. If the modem status interrupt is enabled when this transition occurs, an interrupt is generated.
$\overline{\text{RST}}$	11	M	O	This is the qualified active-low reset signal. $\overline{\text{RST}}$ has a fail safe open-drain output.
$\overline{\text{RTS}}$	35	U	O	Request to send. $\overline{\text{RTS}}$ is an active-low signal. When active, $\overline{\text{RTS}}$ informs the modem of the data set that the UART is ready to receive data. $\overline{\text{RTS}}$ is set to its active state by setting the RTS modem control register bit and is set to its inactive (high) state either as a result of a reset, by doing a loop mode operation, or by clearing bit 1 (RTS) of the MCR.

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

Terminal Functions (Continued)

TERMINAL NAME	TERMINAL NO.	INTER-FACE†	I/O	DESCRIPTION
SA0 SA1 SA2 SA3 SA4 SA5 SA6 SA7	53 55 56 57 58 59 61 65	S	I	Subsystem address bus. When SSAB is high, this is the subsystem address bus and SAD (7–0) is the subsystem data bus. When SSAB is low, this bus is not used and SAD(7–0) is the subsystem multiplexed address/data bus.
SA8	24	S	I	Address bit 8 is bit 8 of the subsystem address bus.
SAD0 SAD1 SAD2 SAD3 SAD4 SAD5 SAD6 SAD7	25 23 20 19 18 17 15 14	S	I/O	Subsystem address/data bus. This is a multiplexed bidirectional address/data bus to the attribute memory DPRAM and CCRs when SSAB is low. This becomes a bidirectional data bus when SSAB is high.
SELZ/$\overline{\text{I}}$	28	S	I	Select Zilog or Intel mode. SELZ/$\overline{\text{I}}$ selects between a Zilog-like or Intel-like microcontroller. SELZ/$\overline{\text{I}}$ is asserted high to select Zilog. SELZ/$\overline{\text{I}}$ is asserted low to select Intel.
SIN	33	U	I	Serial data input. SIN moves information from the communication line or modem to the TL16PC564A UART receiver circuits. Data on the serial bus is disabled when operating in the loop mode.
SOUT	45	U	O	Serial out. SOUT is the composite serial data output to a connected communication device. SOUT is set to the marking (high) state as a result of a reset.
SSAB	3	S	I	Separate subsystem address bus. SSAB selects between a multiplexed address/data bus subsystem interface (SSAB = 0) and a subsystem interface with separate address and data buses (SSAB = 1). This signal has an internal pulldown resistor.
$\overline{\text{STSCHG}}$	74	H	O	Status change. $\overline{\text{STSCHG}}$ is an optional active-low output signal that alerts the host that a subsystem write to attribute memory has occurred. This signal has an open-drain output.
TESTOUT	70	M	O	Test output. This is a production test output.
UARTCLK	51	M	O	UART clock. UARTCLK is a clock output. Its frequency is determined by the frequency on XIN and the divisor value on the programmable clock (PGMCLK) register.
V_{CC}	10,21,22,36, 47,52,60, 72,86,97	M		3.3-V or 5-V supply voltage
VTEST	2	M	I	Voltage test. VTEST is an active-high production test input with an internal pulldown resistor. It can be left open or tied to ground.
$\overline{\text{WE}}$	89	H	I	Write enable. $\overline{\text{WE}}$ is an active-low input signal used for strobing attribute memory write data into the card. This signal has an internal pullup resistor
$\overline{\text{WR}}$(R/$\overline{\text{W}}$)	31	S	I	Write or read/write enable. $\overline{\text{WR}}$(R/$\overline{\text{W}}$) is the active-low write enable in the Intel mode and read/write in the Zilog mode.
XIN	42	M	I	Crystal input. XIN is a clock input divided internally based on the PGMCLK register value, then used as the primary UART clock input.

† Host = H, Subsystem = S, UART = U, Miscellaneous = M

detailed description

reset validation circuit

A reset validation circuit has been implemented to qualify the active-high RESET input. At power up, the level on the $\overline{RST}$ output is unknown. Whenever RESET is stable for at least eight ARBCLKIs, $\overline{RST}$ reflects the inverted state of that stable value of RESET. Any changes on RESET must be valid for eight ARBCLKI clocks before the change is reflected on $\overline{RST}$. This 8-clock filter provides needed hysteresis on the master reset input. $\overline{RST}$ is driven by a low noise, open-drain, fail safe output buffer.

host CPU memory map

The host CPU attribute memory space is mapped as shown in Table 1.

Table 1. Host CPU Attribute Memory Space

Host CPU Address Bits 9–1 (HA0 = 0)	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The host CPU I/O space is mapped as shown in Table 2.

Table 2. Host CPU I/O Memory Space

Normal Mode	Address Mode (hex)				I/O Space
	COM1	COM2	COM3	COM4	
0 (DLAB = 0)†	3F8	2F8	3E8	2E8	UART receiver buffer register (RBR) – read only
0 (DLAB = 0)†	3F8	2F8	3E8	2E8	UART transmitter holding register (THR) – write only
0 (DLAB = 1)†	3F8	2F8	3E8	2E8	UART divisor latch LSB (DLL)
1 (DLAB = 0)†	3F9	2F9	3E9	2E9	UART interrupt enable register (IER)
1 (DLAB = 1)†	3F9	2F9	3E9	2E9	UART divisor latch MSB (DLM)
2	3FA	2FA	3EA	2EA	UART interrupt identification register (IIR) – read only
2	3FA	2FA	3EA	2EA	UART FIFO control register (FCR) – write only
3	3FB	2FB	3EB	2EB	UART line control register (LCR)
4	3FC	2FC	3EC	2EC	UART modem control register (MCR) – bit 5 read only
5	3FD	2FD	3ED	2ED	UART line status register (LSR)
6	3FE	2FE	3EE	2EE	UART modem status register (MSR)
7	3FF	2FF	3EF	2EF	UART scratch register (SCR)

† DLAB is bit 7 of the line control register (LCR).

subsystem memory map

The subsystem attribute memory space is mapped as shown in Table 3.

Table 3. Subsystem Attribute Memory Space

Subsystem Address Bits 8–0	Attribute Memory Space
0 – 255	CIS
256	CCR0
257	CCR1
258	CCR2
259	CCR3
260	CCR4
261	CCR5
262	CCR6
263	CCR7

The subsystem control space is mapped as shown in Table 4.

Table 4. Subsystem Control Memory Space

Subsystem Address Bits 8 – 0	Control Space
272	Control Register
288	PGMCLK Register (write only)

The subsystem UART space is mapped as shown in Table 5.

Table 5. Subsystem UART Memory Space

Subsystem Address Bits 8 – 0	UART Space
304	UART MCR bit 5 (write only)
304	UART DLL (read only)
305	UART IER (read only)
306	UART FCR (read only)
307	UART LCR (read only)
308	UART MCR (read only)
309	UART LSR (read only)
310	UART MSR (read only)
311	UART DLM (read only)
320	UART transmitter FIFO (read only)†
320	UART receiver FIFO (write only)†

† Only when serial bypass mode is enabled

host CPU/attribute memory interface

The host CPU/attribute memory interface is comprised of one port of the internal DPRAM, the eight CCRs, and necessary control circuitry. Signals HA0 and $\overline{CE1}$ are gated together internally so that the output of the gate is low when both signals have been asserted by the host CPU. This output is combined with $\overline{REG}$ and the decoded address, HA(9–1), to provide the chip enable for the DPRAM and CCRs. This composite chip enable in combination with $\overline{WE}$ or $\overline{OE}$ allows writes and reads to the DPRAM and CCRs.

subsystem/attribute memory interface

The subsystem/attribute memory interface is comprised of the second port of the internal DPRAM, the eight CCRs, and necessary control circuitry. When in multiplexed mode (SSAB = 0), the combination of signals SELZ/$\overline{I}$ and ALE($\overline{AS}$) allows either a positive pulse Intel or a negative pulse Zilog address latch enable strobe to latch the address on SA8 and SAD(7–0). When in the Zilog mode (SELZ/$\overline{I}$ high), the combination of read/write [$\overline{WR}$(R/$\overline{W}$)], data strobe [$\overline{RD}$($\overline{DS}$)], and decoded address allows ZBUS access. When in the Intel configuration (SELZ/$\overline{I}$ low), the combination of read [$\overline{RD}$($\overline{DS}$)], write [$\overline{WR}$(R/$\overline{W}$)], and decoded address allows IBUS access.

When in nonmultiplexed mode (SSAB = 1), SA(7–0) become the lower-order address bits, SAD(7–0) are strictly the bidirectional data bus, and ALE($\overline{AS}$) is nonfunctional. All other interface signals function the same.

Table 6. Subsystem/Attribute Memory Interface

SSAB	SELZ/$\overline{I}$	$\overline{RD}$($\overline{DS}$)	$\overline{WR}$(R/$\overline{W}$)	Address	Operation
0	0	0	1	SA8, SAD(7–0)	Intel read
0	0	1	0	SA8, SAD(7–0)	Intel write
0	1	0	1	SA8, SAD(7–0)	Zilog read
0	1	0	0	SA8, SAD(7–0)	Zilog write
1	0	0	1	SA(8–0)	Intel read
1	0	1	0	SA(8–0)	Intel write
1	1	0	1	SA(8–0)	Zilog read
1	1	0	0	SA(8–0)	Zilog write

attribute memory arbitration

Arbitration for the attribute memory is necessary whenever there is simultaneous access to the same DPRAM or CCR address for the conditions of:

- Host CPU read and subsystem write
- Host CPU write and subsystem read
- Host CPU write and subsystem write

If arbitration were not provided, attribute memory data would be corrupted and invalid data read due to uncontrolled access to the same DPRAM or CCR address.

The arbitration control circuitry synchronizes the asynchronous accesses of the host CPU and subsystem to the DPRAM and CCR and controls the access based on the pending host CPU and subsystem attribute memory operation. The synchronizing and control circuitry needs a clock called the arbitration clock. The external clock (ARBCLKI) goes through a programmable divider and can be divided by 1, 2, 4, or 8 to generate a clock frequency within an allowed range for the arbitration logic to work correctly. The output of this frequency divider is named ARBCLKO. The programmable divider bits are defined as shown in Table 7.

Table 7. Programmable Divider Bits

ARBPGM1	ARBPGM0	INTERNAL ARBITRATION CLOCK
L	L	ARBCLKI/1
L	H	ARBCLKI/2
H	L	ARBCLKI/4
H	H	ARBCLKI/8

attribute memory arbitration (continued)

The upper period limit of ARBCLKO is N/6, where N (ns) is the shortest of the two attribute memory accesses, to either the host CPU or the subsystem. The lower period limit of ARBCLKO is based on the DPRAM specifications at the supply voltage used:

5 V = 14-ns clock cycle (71 MHz)
3.3 V = 26-ns clock cycle (38.5 MHz)

For any arbitration condition, attribute memory access is controlled to ensure valid data is read for a port that is doing a read operation and valid data is written for a port that is doing a write operation. When both the host CPU and subsystem are performing simultaneous write operations to the same address, the host CPU is allowed to write and the subsystem write is ignored.

host CPU/subsystem handshake

Two signals are provided for handshaking between the host CPU and the subsystem. The active-high IRQ signifies to the subsystem that the host CPU has written data into attribute memory. The subsystem can clear IRQ by setting bit 6 of the subsystem control register. The active-low $\overline{\text{STSCHG}}$ signifies to the host CPU that the subsystem has written data to attribute memory provided bit 2 of the subsystem control register ($\overline{\text{STSCHG}}$ enable) is set. The host CPU clears $\overline{\text{STSCHG}}$ by reading any location in attribute memory. The control of these signals is synchronized to ARBCLKO to ensure there are no false assertions/deassertions.

There is additional arbitration performed for instances of simultaneous assertion/deasseration of IRQ or $\overline{\text{STSCHG}}$. When a subsystem write and host CPU read occur simultaneously, $\overline{\text{STSCHG}}$ may be briefly deasserted prior to being asserted, but the write ultimately wins arbitration. If the host CPU read occurs more than one-half an arbitration clock after the subsystem write, $\overline{\text{STSCHG}}$ is deasserted. IRQ is arbitrated in a similar fashion.

host CPU/UART interface

The UART select is derived from either host CPU address information or logic levels on $\overline{\text{CE1}}$, $\overline{\text{CE2}}$ and $\overline{\text{REG}}$. In the address mode, host CPU address bits HA9, HA7, HA6, HA5, and HA3 are combined with conditional derivatives of HA4 and HA8 to select the UART (HA4 and HA8 select COM ports 1–4 based on settings in the subsystem control register). $\overline{\text{CE1}}$ and $\overline{\text{CE2}}$ are combined such that either of these two signals in combination with $\overline{\text{REG}}$ enable the UART in the event that these signals are present. In the event that $\overline{\text{CE1}}$ or $\overline{\text{CE2}}$ are not present, the UART must be accessed in the address mode previously described. The UART select in conjunction with $\overline{\text{IORD}}$ and $\overline{\text{IOWR}}$ allows host CPU accesses to the UART. Host CPU address bits HA2–HA0 are decoded to select which UART register is to be accessed.

All UART registers remain intact with the exception of the FIFO control register (FCR) and the modem control register (MCR). The FCR (host CPU write-only address 2) bits 4 and 5 in conjunction with $\overline{\text{EXTEND}}$ control $\overline{\text{RTS}}$ operation and FIFO depth are shown in Table 8.

Table 8. FIFO Control Register and $\overline{\text{EXTEND}}$ Signal Control of FIFO Depth and $\overline{\text{RTS}}$ Operation

BIT 5	BIT 4	$\overline{\text{EXTEND}}$	RTS OPERATION	FIFO DEPTH
X	X	H	Normal	16 bytes
0	0	L	Normal	16 bytes
0	1	L	Auto	16 bytes
1	0	L	Normal	64 bytes
1	1	L	Auto	64 bytes

host CPU/UART interface (continued)

FCR bit 5 high and $\overline{\text{EXTEND}}$ low redefine the receiver FIFO trigger levels set by FCR bits 6 and 7 are shown in Table 9.

Table 9. Receiver FIFO Trigger Level

BIT 7	BIT 6	RECEIVER FIFO TRIGGER LEVEL
0	0	1
0	1	16
1	0	32
1	1	56

The MCR bit 5 (host CPU address 4) is read only. This bit is controlled by the subsystem to enable (high) the auto-$\overline{\text{CTS}}$ mode of operation

subsystem/UART interface

The UART provides a serial communications channel to the subsystem with enhanced $\overline{\text{RTS}}$ control (see auto-$\overline{\text{RTS}}$ description). This channel is capable of operating at 115 kbps and is the main communications channel to the subsystem (refer to the TL16C550 specification for the detailed description of the serial communications channel).

Many of the UART registers have been mapped into the subsystems memory space as read only. In addition, MCR bit 5 (subsystem address 130 hex) is controlled by the subsystem to enable (set) auto-$\overline{\text{CTS}}$. The subsystem can read the MCR at address 134 hex. When reading the FCR (subsystem address 132 hex), bits 1 and 2 are always set, and bits 4 and 5 are cleared only when $\overline{\text{EXTEND}}$ is low and the host CPU has set them (64-byte FIFOs and auto-$\overline{\text{RTS}}$ enabled) (refer to the subsystem memory map).

subsystem control register

The subsystem control register is an 8-bit register located at subsystem address 110 (hex). This register is programmed based on host CPU configuration information and has a default selection of COM2 after a valid reset. The bit definitions are as follows (0 = LSB):

- Bits 0 and 1: These bits define which host COM port the UART is connected to when the chip is in the address mode. COM2 is the default (power-up) condition. COM port selection is shown in Table 10.

Table 10. COM Port Selection

BIT 1	BIT 0	COM PORT
0	0	COM1
1	0	COM2
0	1	COM3
1	1	COM4

- Bit 2: This bit is a host CPU interrupt enable bit. When this bit is set, any subsystem attribute memory write cycle causes $\overline{\text{STSCHG}}$ to be asserted. This bit is cleared after a valid reset.
- Bit 3: This bit enables or disables address mode selection as described in the host CPU/UART interface description. This bit is cleared (disabling the address mode) after a valid reset.

subsystem control register (continued)

- Bits 4 and 5: These bits together ensure adherence to PCMCIA power-up requirements. At power up, the card must operate as a memory card and all host CPU I/O operations must be disabled. $\overline{\text{IREQ}}$, which doubles as the host CPU READY/$\overline{\text{BUSY}}$ line, powers up low indicating that the memory card is busy. Once the subsystem initializes attribute memory, the subsystem sets bit 4 to indicate that the memory card is ready. Then bit 5 is cleared, changing the configuration from a memory card to an I/O card, enabling host CPU UART accesses. $\overline{\text{IREQ}}$ now becomes the host CPU interrupt request line. Memory card, I/O, and $\overline{\text{IREQ}}$ selection is shown in Table 11.

Table 11. Memory Card, I/O, and $\overline{\text{IREQ}}$ Selection

BIT 5	BIT 4	CONFIGURATION
1	0	Memory card and I/O operation (UART) are disabled; $\overline{\text{IREQ}}$ is low indicating that the card is busy (power-up and reset condition).
1	1	Memory card and I/O operation (UART) are disabled; $\overline{\text{IREQ}}$ is high indicating that the card is ready.
0	X	I/O card and I/O operation (UART) are enabled; $\overline{\text{IREQ}}$ now functions as the host CPU interrupt request line.

- Bit 6 is a self clearing bit that resets the subsystem IRQ signal. Writing a 1 to this location clears the IRQ interrupt.
- Bit 7 enables or disables serial bypass mode as described in the subsystem serial bypass mode description. This bit is cleared (disabling serial bypass mode) after a valid reset.

subsystem PGMCLK register/divide-by-n circuit

The subsystem PGMCLK register is a 6-bit write-only register located at address 120 hex and selects the divisor of the divide-by-n-and-a-half circuitry. Any write to this register generates a reset to the UART and the divide-by-n circuitry.

The divide-by-n circuitry allows for a divisor from 0 to 31.5 in 0.5 increments (PGMCLK0 is the half bit). The divided clock output drives the UART clock input and can be seen on UARTCLK. The UART requires a clock with a minimum high pulse duration of 50 ns and a minimum low pulse duration of 50 ns (10-MHz maximum operating frequency). A programmed divisor between 2 and 7.5 drives the UART clock low for one XIN clock cycle for integer divisors and 1.5 XIN clock cycles for integer-plus-a-half divisors. A programmed divisor of eight or greater drives the UART clock low for four XIN clock cycles for integer divisors and 4.5 XIN clock cycles for integer-plus-a-half divisors. Based on the above parameters, the acceptable

XIN/divisor combinations can be derived using XIN input clock. The precision of the programmable clock generator for integer-plus-a-half divisors depends on the closeness to a 50% duty cycle for the XIN input clock (see Table 12).

Table 12. Programmable Clock Generator Precision Selection

PGMCLK(0 – 5) VALUE (HEX)	RESULT
0 (0)	No clock (driven high)
0.5 (1)	Divide-by-1
1 (2)	Divide-by-1
1.5 (3)	Divide-by-1
2 (4) to 31.5 (3F)	Divide-by-2 to divide-by-31.5

subsystem serial bypass mode

The optional serial bypass mode is implemented to allow a high throughput path to/from the host CPU. When this mode is enabled and subsystem control register bit 7 is high, the serial portion of the UART is bypassed and the subsystem has direct parallel access to the receiver FIFO (write address 140 hex) and the transmitter FIFO (read address 140 hex). All host CPU interrupts operate normally except for receiver parity, framing, and breaking interrupts.

auto-$\overline{\text{CTS}}$ operation

The optional auto-$\overline{\text{CTS}}$ operation is implemented so that the host CPU cannot overflow the modem receive buffer. Auto-$\overline{\text{CTS}}$ operation is enabled when the subsystem sets MCR bit 5 (subsystem address 130 hex). When auto-$\overline{\text{CTS}}$ enabled, deactivating $\overline{\text{CTS}}$ (high) halts the transmitter section of the UART after it completes the current transfer. Once $\overline{\text{CTS}}$ is reactivated (low) by the modem, transfers resume. Interrupt operation is not affected by enabling auto-$\overline{\text{CTS}}$.

auto-$\overline{\text{RTS}}$ operation

The optional auto-$\overline{\text{RTS}}$ operation is implemented so that the subsystem cannot overflow the receiver FIFO. Auto-$\overline{\text{RTS}}$ operation is enabled when FCR bit 4 is high and $\overline{\text{EXTEND}}$ is low and operates independently from the trigger level circuitry. In the 16-byte FIFO mode, the RTS bit in the modem control register (bit 1) clears when 14 characters are in the receive FIFO. This action causes $\overline{\text{RTS}}$ to go high (inactive). In the 64-byte FIFO mode, the MCR RTS bit clears when 56 characters are in the receiver FIFO. Interrupt operation is not affected and operates the same way in either auto-$\overline{\text{RTS}}$ or nonauto-$\overline{\text{RTS}}$ mode. When enabled, a receive data available interrupt occurs after the trigger level is reached. The MCR RTS bit must then be set by the host CPU after the receiver FIFO has been read.

power consumption

The TL16PC564A has low power consumption under the following conditions:

- 32-MHz signal on XIN
- Divide-by-n is set to give a 1.8432-MHz UARTCLK signal
- Nominal data
- V_{CC} = 5 V

The current (I_{CC}) and power consumption are 18 mA (typical) and 90 mW (typical), respectively. These current and power figures fluctuate with changes in the above conditions.

absolute maximum ratings over operating free-air temperature range†

Supply voltage range, V_{CC}	–0.5 V to 6 V
Input voltage range, V_I (standard)	–0.5 V to V_{CC} + 0.5 V
Input voltage range, V_I (fail safe)	–0.5 V to 6.5 V
Output voltage range, V_O (standard)	–0.5 V to V_{CC} + 0.5 V
Output voltage range, V_O (fail safe)	–0.5 V to 6.5 V
Input clamp current, I_{IK} (V_I < 0 or V_I > V_{CC}) (see Note 1)	±20 mA
Output clamp current, I_{OK} (V_O < 0 or V_O > V_{CC}) (see Note 2)	±20 mA
Operating free-air operating temperature range, T_A	0°C to 70°C
Storage temperature range, T_{stg}	–65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. This applies for external input and bidirectional buffers. $V_I > V_{CC}$ does not apply to fail safe terminals.
2. This applies for external output and bidirectional buffers. $V_O > V_{CC}$ does not apply to fail safe terminals.

recommended operating conditions

low voltage (3.3 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		3	3.3	3.6	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage (CMOS), V_{IH} (see Note 3)		$0.7V_{CC}$			V
Low-level input voltage (CMOS), V_{IL} (see Note 3)				$0.3V_{CC}$	V
Output voltage, V_O (see Note 4)		0		V_{CC}	V
High-level output current, I_{OH}	All outputs except $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, $\overline{OUT2}$ (see Note 5)			1.8	mA
Low-level output current, I_{OL}	All outputs except $\overline{RST}$			3.2	mA
	$\overline{RST}$			6.4	
Input transition time, t_t		0		25	ns
Operating free-air temperature range, T_A		0	25	70	°C
Junction temperature range, T_J (see Note 6)		0	25	115	°C

NOTES: 3. Meets TTL levels, V_{IH}min = 2 V and V_{IL}max = 0.8 V on nonhysteresis inputs.
4. Applies for external output buffers.
5. $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, and $\overline{OUT2}$ are open-drain outputs, so I_{OH} does not apply.
6. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

standard voltage (5 V nominal)

		MIN	NOM	MAX	UNIT
Supply voltage, V_{CC}		4.75	5	5.25	V
Input voltage, V_I		0		V_{CC}	V
High-level input voltage (CMOS), V_{IH}		$0.7V_{CC}$			V
Low-level input voltage (CMOS), V_{IL}				$0.2V_{CC}$	V
Output voltage, V_O (see Note 4)		0		V_{CC}	V
High-level output current, I_{OH}	All outputs except $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, $\overline{OUT2}$ (see Note 5)			4	mA
Low-level output current, I_{OL}	All outputs except $\overline{RST}$			4	mA
	$\overline{RST}$			8	
Input transition time, t_t		0		25	ns
Operating free-air temperature range, T_A		0	25	70	°C
Junction temperature range, T_J (see Note 6)		0	25	115	°C

NOTES: 4. Applies for external output buffers.
5. $\overline{RST}$, $\overline{STSCHG}$, $\overline{OUT1}$, and $\overline{OUT2}$ are open-drain outputs, so I_{OH} does not apply.
6. These junction temperatures reflect simulation conditions. Absolute maximum junction temperature is 150°C. The customer is responsible for verifying junction temperature.

electrical characteristics over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted)

low voltage (3.3 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{CC}-0.55$		V
V_{OL}	Low-level output voltage	I_{OL} = rated		0.5	V
V_{IT+}	Positive-going input threshold voltage (see Note 7)			0.7 V_{CC}	V
V_{IT-}	Negative-going input threshold voltage (see Note 7)		0.3 V_{CC}		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$) (see Note 7)		0.1 V_{CC}	0.3 V_{CC}	V
I_{OZ}	3-state-output high-impedance current (see Note 8)	V_I = V_{CC} or GND		±10	µA
I_{IL}	Low-level input current (see Note 9)	V_I = GND		–1	µA
I_{IH}	High-level input current (see Note 10)	V_I = V_{CC}		1	µA

NOTES: 7. Applies for external input and bidirectional buffers with hysteresis.
8. The 3-state or open-drain output must be in the high-impedance state.
9. Specifications only apply with pullup terminator turned off.
10. Specifications only apply with pulldown terminator turned off.

standard voltage (5 V nominal)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
V_{OH}	High-level output voltage	I_{OH} = rated	$V_{CC}-0.8$		V
V_{OL}	Low-level output voltage	I_{OL} = rated		0.5	V
V_{IT+}	Positive-going input threshold voltage (see Note 7)			0.7 V_{CC}	V
V_{IT-}	Negative-going input threshold voltage (see Note 7)		0.2 V_{CC}		V
V_{hys}	Hysteresis ($V_{IT+} - V_{IT-}$) (see Note 7)		0.1 V_{CC}	0.3 V_{CC}	V
I_{OZ}	3-state-output high-impedance current (see Note 8)	V_I = V_{CC} or GND		±10	µA
I_{IL}	Low-level input current (see Note 9)	V_I = GND		–1	µA
I_{IH}	High-level input current (see Note 10)	V_I = V_{CC}		1	µA

NOTES: 7. Applies for external input and bidirectional buffers with hysteresis.
8. The 3-state or open-drain output must be in the high-impedance state.
9. Specifications only apply with pullup terminator turned off.
10. Specifications only apply with pulldown terminator turned off.

XIN timing requirements over recommended operating free-air temperature range (see Figure 1)

		TEST CONDITIONS	MIN	MAX	UNIT
	Input frequency	V_{CC} = 3.3 V		50	MHz
		V_{CC} = 5 V		60	
t_{c1}	Cycle time, XIN	V_{CC} = 3.3 V	20		ns
		V_{CC} = 5 V	16.7		
t_{w1}	Pulse duration, XIN clock high	V_{CC} = 3.3 V	10		ns
		V_{CC} = 5 V	8		
t_{w2}	Pulse duration, XIN clock low	V_{CC} = 3.3 V	10		ns
		V_{CC} = 5 V	8		

clock switching characteristics over recommended operating free-air temperature range (see Figure 1)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d1}	Delay time, XIN↑ to UARTCLK↑	V_{CC} = 3.3 V		14	ns
		V_{CC} = 5 V		8	
t_{d2}	Delay time, XIN↓ to UARTCLK↓	V_{CC} = 3.3 V		16	ns
		V_{CC} = 5 V		10	
t_{d3}	Delay time, XIN↑ to UARTCLK↓	V_{CC} = 3.3 V		19.8	ns
		V_{CC} = 5 V		13	
t_{d4}	Delay time, XIN↑ to UARTCLK↑	V_{CC} = 3.3 V		20.6	ns
		V_{CC} = 5 V		13.5	
t_{d5}	Delay time, XIN↓ to UARTCLK↑	V_{CC} = 3.3 V		21	ns
		V_{CC} = 5 V		13.8	

host CPU I/O read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 11)

		MIN	MAX	UNIT
t_{h1}	Hold time, HA(9–0) valid after $\overline{\text{IORD}}$↑	20		ns
t_{h2}	Hold time, $\overline{\text{REG}}$↑ valid after $\overline{\text{IORD}}$↑	0		ns
t_{w4}	Pulse duration, $\overline{\text{IORD}}$ low	165		ns
t_{su1}	Setup time, HA(9–0) valid before $\overline{\text{IORD}}$↓	70		ns
t_{su2}	Setup time, $\overline{\text{CE}}$x↓ before $\overline{\text{IORD}}$↓	5		ns
t_{h3}	Hold time, $\overline{\text{CE}}$x↑ after $\overline{\text{IORD}}$↑	20		ns
t_{h4}	Hold time, HD(7–0) valid after $\overline{\text{IORD}}$↑	0		ns
t_{su3}	Setup time, $\overline{\text{REG}}$↓ before $\overline{\text{IORD}}$↓	5		ns
t_{d6}	Delay time, HD(7–0) valid after $\overline{\text{IORD}}$↓		100	ns

NOTE 11. The maximum load on $\overline{\text{INPACK}}$ is one LSTTL with 50-pF total load. All timing is measured in nanoseconds.

host CPU I/O read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 2 and Note 11)

PARAMETER		MIN	MAX	UNIT
t_{d7}	Delay time, $\overline{\text{INPACK}}$↓ after $\overline{\text{IORD}}$↓		45	ns
t_{d8}	Delay time, $\overline{\text{INPACK}}$↑ after $\overline{\text{IORD}}$↑		45	ns

NOTE 11. The maximum load on $\overline{\text{INPACK}}$ is one LSTTL with 50-pF total load. All timing is measured in nanoseconds.

host CPU I/O write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 3)

		MIN	MAX	UNIT
t_{su4}	Setup time, HD(7–0) valid before $\overline{IOWR}\downarrow$	60		ns
t_{h5}	Hold time, HA(9–0) valid after $\overline{IOWR}\uparrow$	20		ns
t_{w6}	Pulse duration, $\overline{IOWR}$ low	165		ns
t_{su5}	Setup time, HA(9–0) valid before $\overline{IOWR}\downarrow$	70		ns
t_{h6}	Hold time, $\overline{REG}\uparrow$ after $\overline{IOWR}\uparrow$	0		ns
t_{su6}	Setup time, $\overline{CE}x\downarrow$ before $\overline{IOWR}\downarrow$	5		ns
t_{h7}	Hold time, $\overline{CE}x\uparrow$ after $\overline{IOWR}\uparrow$	20		ns
t_{su7}	Setup time, $\overline{REG}\downarrow$ before $\overline{IOWR}\downarrow$	5		ns
t_{h8}	Hold time, HD(7–0) valid after $\overline{IOWR}\uparrow$	30		ns

transmitter switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 4)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d9}	Delay time, $\overline{SOUT}\downarrow$ after $\overline{IOWR}\uparrow$		8	24	Baud cycles
t_{d10}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{SOUT}\downarrow$		8	8	Baud cycles
t_{d11}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{IOWR}\uparrow$		16	32	Baud cycles
t_{d12}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IOWR}\uparrow$	C_L = 100 pF		140	ns
t_{d13}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IORD}\uparrow$	C_L = 100 pF		140	ns

receiver switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 5)

PARAMETER		TEST CONDITIONS	MIN	MAX	UNIT
t_{d14}	Delay time, sample CLK$\uparrow$ after RCLK$\uparrow$			100	ns
t_{d15}	Delay time, $\overline{IREQ}\downarrow$ after SIN$\downarrow$			1	RCLK cycles
t_{d16}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IORD}\uparrow$	C_L = 100 pF		150	ns

modem control switching characteristics over recommended ranges of operating free-air temperature and supply voltage, C_L = 100 pF (see Figure 6)

PARAMETER		MIN	MAX	UNIT
t_{d17}	Delay time, $\overline{RTS}$, $\overline{DTR}$, $\overline{OUT1}$, $\overline{OUT2}$ $\downarrow$ or $\uparrow$ after $\overline{IOWR}\uparrow$		50	ns
t_{d18}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{CTS}$, $\overline{DSR}$, $\overline{DCD}\downarrow$		30	ns
t_{d19}	Delay time, $\overline{IREQ}\uparrow$ after $\overline{IORD}\uparrow$		35	ns
t_{d20}	Delay time, $\overline{IREQ}\downarrow$ after $\overline{RI}\uparrow$		30	ns

host CPU attribute memory write cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figures 7 and 8)

		MIN	MAX	UNIT
t_{c2}	Write cycle tIme, HA(9–0)	250		ns
t_{w8}	Pulse duration, $\overline{WE}$ low	150		ns
t_{su8}	Setup time, $\overline{CE}$x↓ before $\overline{WE}$↑	180		ns
t_{su9}	Setup time, HA(9–0) before $\overline{WE}$↑ (see Note 12)	180		ns
t_{su10}	Setup time, HA(9–0) before $\overline{WE}$↓ and $\overline{CE}$x↓(see Note 12)	30		ns
t_{su11}	Setup time, $\overline{OE}$↑ before $\overline{WE}$↓	10		ns
t_{h9}	Hold time, HD(7–0) IN after $\overline{WE}$↑	30		ns
t_{rec1}	Recovery time, HA(9–0) after $\overline{WE}$↑	30		ns
t_{su12}	Setup time, HD(7–0) IN before $\overline{WE}$↑	80		ns
t_{h10}	Hold time, $\overline{OE}$↓ after $\overline{WE}$↑	10		ns
t_{su13}	Setup time, $\overline{CE}$x↓ before $\overline{WE}$↓	0		ns
t_{h11}	Hold time, $\overline{CE}$x↑ after $\overline{WE}$↑	20		ns

NOTE 12. The $\overline{REG}$ signal timing is identical to address signal timing.

host CPU attribute memory write cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 7)

PARAMETER		MIN	MAX	UNIT
t_{dis1}	Disable time, HD(7–0) OUT after $\overline{WE}$↓		100	ns
t_{dis2}	Disable time, HD(7–0) OUT after $\overline{OE}$↑		100	ns
t_{en1}	Enable time, HD(7–0) OUT after $\overline{WE}$↑	5		ns
t_{en2}	Enable time, HD(7–0) OUT after $\overline{OE}$↓	5		ns

host CPU attribute memory read cycle timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

		MIN	MAX	UNIT
t_{c3}	Read cycle time	300		ns
t_{d22}	Delay time, HD(7–0) after HA(9–0)		300	ns
t_{d23}	Delay time, HD(7–0) after $\overline{CE}$x↓		300	ns
t_{d24}	Delay time, HD(7–0) after $\overline{OE}$↓		150	ns
t_{h12}	Hold time, HD(7–0) after HA(9–0)	0		ns
t_{su14}	Setup time, $\overline{CE}$x↓ before $\overline{OE}$↓	0		ns
t_{h13}	Hold time, HA(9–0) after $\overline{OE}$↑	20		ns
t_{su15}	Setup time, HA(9–0) before $\overline{OE}$↓	30		ns
t_{h14}	Hold time, $\overline{CE}$x↑ after $\overline{OE}$↑	20		ns

host CPU attribute memory read cycle switching characteristics over recommended ranges of operating free-air temperature and supply voltage (see Figure 9)

PARAMETER		MIN	MAX	UNIT
t_{dis3}	Disable time, HD(7–0) after $\overline{CE}$x↑		100	ns
t_{dis4}	Disable time, HD(7–0) after $\overline{OE}$↑		100	ns
t_{en3}	Enable time, HD(7–0) after $\overline{CE}$x↓	5		ns
t_{en4}	Enable time, HD(7–0) after $\overline{OE}$↓	5		ns

subsystem Intel mode timing requirements (32 MHz) (see Figure 10)

INTEL SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
t_{LHLL}	t_{w11}	Pulse duration, ALE high	48		ns
t_{AVLL}	t_{su16}	Setup time, SA8, SAD(7–0) valid to ALE low	21		ns
t_{PLLL}	t_{d25}	Delay time, $\overline{CS}$ low to ALE low	21		ns
t_{LLAX}	t_{h15}	Hold time, SA8, SAD(7–0) valid after ALE↓	21		ns
t_{LLWL}	t_{d26}	Delay time, ALE low to $\overline{WR}$ low	16		ns
t_{LLRL}	t_{d27}	Delay time, ALE low to $\overline{RD}$ low	16		ns
t_{WHLH}	t_{d28}	Delay time, $\overline{WR}$ high to ALE high	21		ns
t_{AFRL}	t_{d29}	Delay time, SA8, SAD(7–0) in high-impedance state to $\overline{RD}$ low	0		ns
t_{RLRH}	t_{w12}	Pulse duration, $\overline{RD}$ low	120		ns
t_{WLWH}	t_{w13}	Pulse duration, $\overline{WR}$ low	120		ns
t_{RHAX}	t_{d30}	Delay time, $\overline{RD}$ high to SA8, SAD(7–0) active	48		ns
t_{WHDX}	t_{h16}	Hold time, SA8, SAD(7–0) valid after $\overline{WR}$ high	48		ns
t_{WHPH}	t_{d31}	Delay time, $\overline{WR}$ high to $\overline{CS}$ high	21		ns
t_{RHPH}	t_{d32}	Delay time, $\overline{RD}$ high to $\overline{CS}$ high	21		ns
t_{PHPL}	t_{w14}	Pulse duration, $\overline{CS}$ high	21		ns

subsystem Zilog mode timing requirements (20 MHz) (see Figure 11)

ZILOG SYMBOL	JEDEC SYMBOL		MIN	MAX	UNIT
$t_{dA(AS)}$	t_{su17}	Setup time, SA8 and SAD(7–0) valid before $\overline{AS}$ high	20		ns
$t_{dAS(A)}$	t_{d33}	Delay time, $\overline{AS}$ high to SA8 and SAD(7–0) invalid	35		ns
$t_{dAS(DR)}$	t_{d34}	Delay time, $\overline{AS}$ high to data in on SAD(7–0)		150	ns
t_{wAS}	t_{w15}	Pulse duration, $\overline{AS}$ low	35		ns
$t_{dA(DS)}$	t_{d35}	Delay time, SA8 and SAD(7–0) invalid to $\overline{DS}$ low	0		ns
$t_{wDS(read)}$	t_{w16}	Pulse duration, $\overline{DS}$ low (read)	125		ns
$t_{wDS(write)}$	t_{w17}	Pulse duration, $\overline{DS}$ low (write)	65		ns
$t_{dDS(DR)}$	t_{d36}	Delay time, $\overline{DS}$ low to data in valid		80	ns
$t_{hDS(DR)}$	t_{h17}	Hold time, $\overline{DS}$ high to data in invalid	0		ns
$t_{dDS(A)}$	t_{h18}	Hold time, $\overline{DS}$ high to data out invalid	20		ns
$t_{dDS(AS)}$	t_{d37}	Delay time, $\overline{DS}$ high to $\overline{AS}$ low	30		ns
$t_{dDO(DS)}$	t_{d38}	Delay time, SAD(7–0) (write data from μP) valid to $\overline{DS}$ low	10		ns
$t_{dRW(AS)}$	t_{d39}	Delay time, R/$\overline{W}$ active to AS high	20		ns

subsystem Intel nonmultiplexed timing requirements (see Figure 12)

		MIN	MAX	UNIT
t_{su18}	Setup time, SA(8–0), $\overline{CS}$ valid to $\overline{RD}$, $\overline{WR}\downarrow$	30		ns
t_{w18}	Pulse duration, $\overline{RD}$ low	120		ns
t_{w19}	Pulse duration, $\overline{WR}$ low	120		ns
t_{su19}	Setup time, SAD(7–0) valid to $\overline{WR}\uparrow$	50		ns
t_{en4}	Enable time, $\overline{RD}\downarrow$ to SAD(7–0) driving	5		ns
t_{d40}	Delay time, $\overline{RD}\downarrow$ to SAD(7–0) valid		105	ns
t_{h19}	Hold time, SA(8–0), $\overline{CS}$ valid after $\overline{RD}$, $\overline{WR}\uparrow$	30		ns
t_{h20}	Hold time, SAD(7–0) valid after $\overline{WR}\uparrow$	30		ns
t_{dis3}	Disable time, $\overline{RD}\uparrow$ to SAD(7–0) high impedance	5	15	ns

subsystem Zilog nonmultiplexed timing requirements (see Figure 13)

		MIN	MAX	UNIT
t_{su20}	Setup time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid to $\overline{DS}\downarrow$ (write)	90		ns
t_{su21}	Setup time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid to $\overline{DS}\downarrow$ (read)	30		ns
t_{w20}	Pulse duration, $\overline{DS}$ low (write)	65		ns
t_{w21}	Pulse duration, $\overline{DS}$ low (read)	125		ns
t_{su22}	Setup time, SAD(7–0) valid to $\overline{DS}\uparrow$	50		ns
t_{en5}	Enable time, $\overline{DS}\downarrow$ to SAD(7–0) driving	5		ns
t_{d41}	Delay time, $\overline{DS}\downarrow$ to SAD(7–0) valid		105	ns
t_{h21}	Hold time, SA(8–0), $\overline{CS}$, R/$\overline{W}$ valid after $\overline{DS}\uparrow$	30		ns
t_{h22}	Hold time, SAD(7–0), $\overline{CS}$, R/$\overline{W}$ valid after $\overline{DS}\uparrow$	30		ns
t_{dis4}	Hold time, $\overline{DS}\uparrow$ to SAD(7–0) high impedance	5	15	ns

ARBCLK switching characteristics over recommended operating free-air temperature range (see Figure 14)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{c4}	Cycle time, internal arbitration clock (ARBCLKI ÷ ARBPGM)	V_{CC} = 3.3 V	26	Note 13	ns
		V_{CC} = 5 V	14	Note 13	
t_{c5}	Cycle time, arbitration clock	V_{CC} = 3.3 V	26		ns
		V_{CC} = 5 V	14		
t_{d42}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷1)	V_{CC} = 3.3 V		13	ns
		V_{CC} = 5 V		7.3	
t_{d43}	Delay time, ARBCLKI↓ to ARBCLK0↓ (÷1)	V_{CC} = 3.3 V		15.5	ns
		V_{CC} = 5 V		10	
t_{d44}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷2)	V_{CC} = 3.3 V		15.3	ns
		V_{CC} = 5 V		8.8	
t_{d45}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷2)	V_{CC} = 3.3 V		17.5	ns
		V_{CC} = 5 V		11	
t_{d46}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷4)	V_{CC} = 3.3 V		19.5	ns
		V_{CC} = 5 V		11.5	
t_{d47}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷4)	V_{CC} = 3.3 V		21.5	ns
		V_{CC} = 5 V		13.5	
t_{d48}	Delay time, ARBCLKI↑ to ARBCLK0↑ (÷8)	V_{CC} = 3.3 V		22.7	ns
		V_{CC} = 5 V		13.5	
t_{d49}	Delay time, ARBCLKI↑ to ARBCLK0↓ (÷8)	V_{CC} = 3.3 V		25	ns
		V_{CC} = 5 V		15.7	

NOTE 13. t_{c4} max = N/6, where N = shortest (in ns) of the two attribute memory accesses, host CPU or subsystem.

reset timing requirements over recommended ranges of operating free-air temperature and supply voltage (unless otherwise noted) (see Figure 15)

		TEST CONDITIONS	MIN	MAX	UNIT
t_{w22}	Pulse duration, RESET active		$8 \cdot t_{c5}$		ns
t_{w23}	Pulse duration, RESET inactive		$8 \cdot t_{c5}$		ns
t_{d50}	Delay time, ARBCLKI↑ to $\overline{RST}$ low	V_{CC} = 3.3 V		10.4	ns
		V_{CC} = 5 V		7.5	
t_{d51}	Delay time, ARBCLKI↑ to RST high impedance	V_{CC} = 3.3 V		13.9	ns
		V_{CC} = 5 V		9.7	

subsystem interrupt request timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 16)

		MIN	MAX	UNIT
t_{d52}	Delay time, $\overline{WE}$↑ to IRQ↑ (see Note 14)	$2t_{c5}$	$3t_{c5}$	ARBCLKI cycles
t_{d53}	Delay time, SCR bit 6↑ to IRQ↓ (see Note 15)	t_{c5}	$2t_{c5}$	ARBCLKI cycles

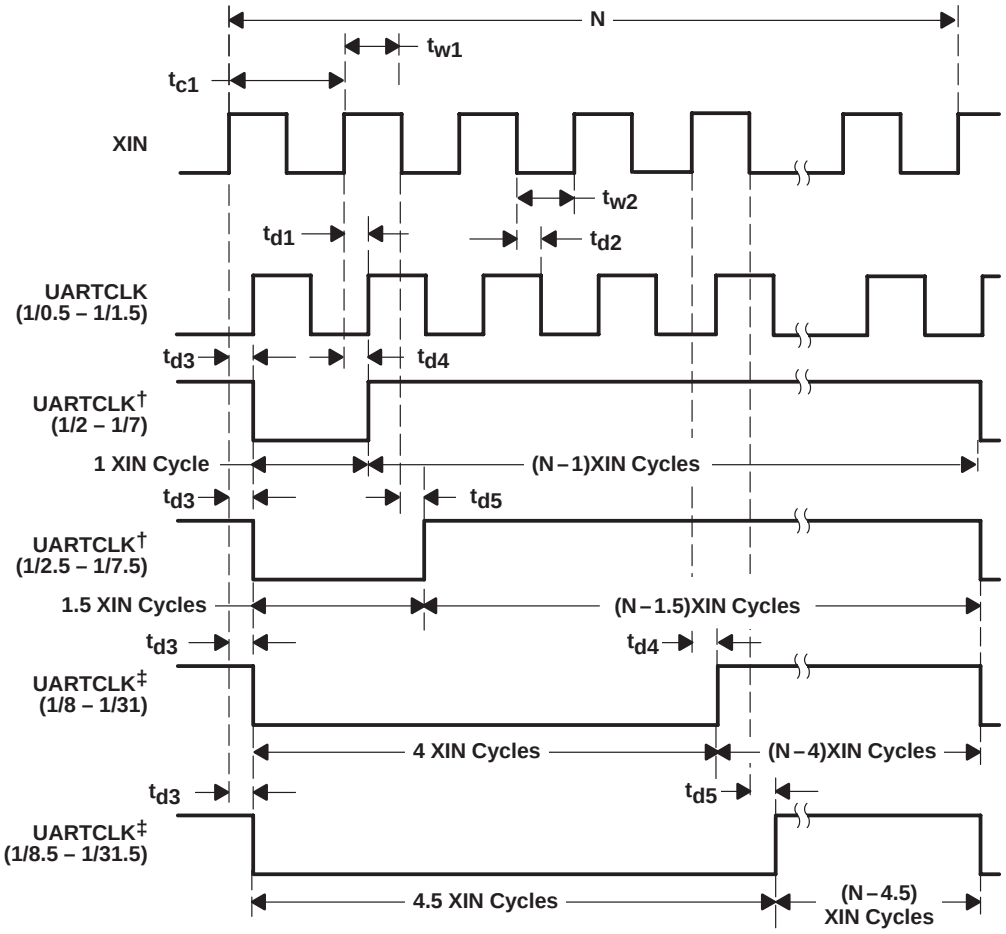
NOTES: 14. Synchronized to rising edge of ARBCLKI
15. Synchronized to falling edge of ARBCLKI

host CPU status change timing requirements over recommended ranges of operating free-air temperature and supply voltage (see Figure 17)

		MIN	MAX	UNIT
t_{d54}	Delay time, subsystem write↑ to $\overline{\text{STSCHG}}$↓ (see Note 14)	$2t_{c5}$	$3t_{c5}$	ARBCLKI cycles
t_{d55}	Delay time, $\overline{\text{OE}}$↓ to $\overline{\text{STSCHG}}$ high impedance (see Note 15)	t_{c5}	$2t_{c5}$	ARBCLKI cycles

NOTES: 14. Synchronized to rising edge of ARBCLKI
15. Synchronized to falling edge of ARBCLKI

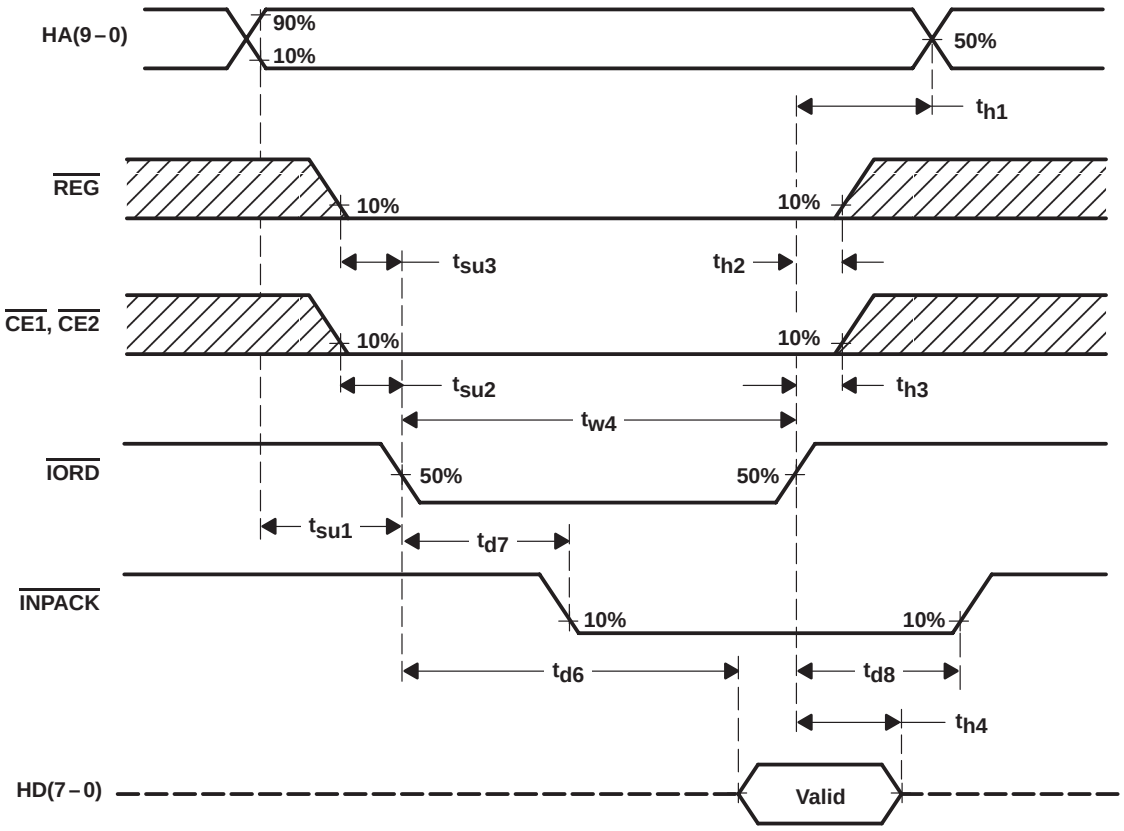
PARAMETER MEASUREMENT INFORMATION



† The low portion of the UARTCLK cycle = 1 XIN cycle for PGMCLK integer values of 2 to 7 and 1.5 XIN cycles for PGMCLK noninteger values 2.5 to 7.5.
‡ The low portion of the UARTCLK cycle = 4 XIN cycles for PGMCLK integer values of 8 to 31 and 4.5 XIN cycles for PGMCLK noninteger values 8.5 to 31.5.

Figure 1. XIN Clock Timing Waveforms

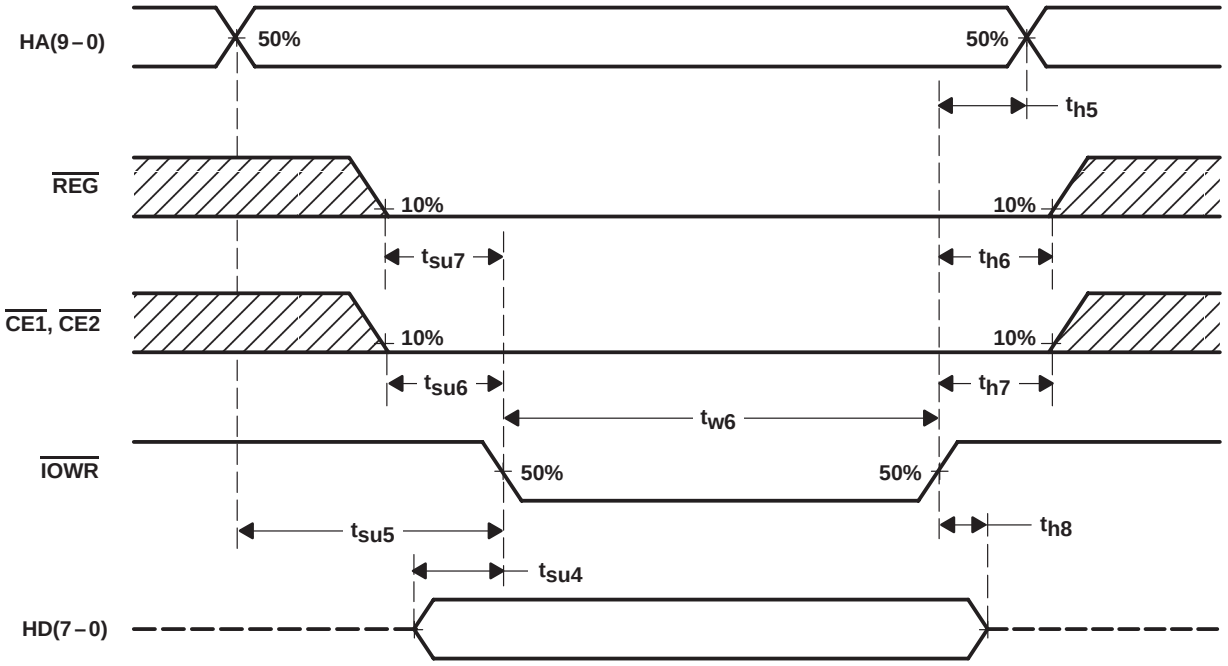
PARAMETER MEASUREMENT INFORMATION



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 2. Host CPU I/O Read Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: All timings are measured at the card. Skews and delays from the system driver/receiver to the card must be accounted for by the system design.

Figure 3. Host CPU I/O Write Timing Waveforms

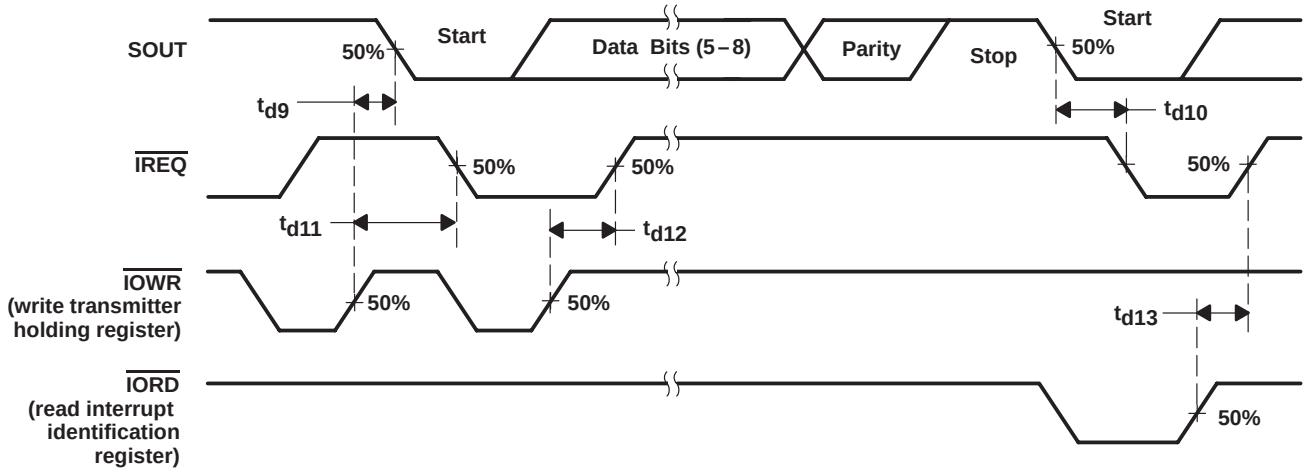


Figure 4. Transmitter Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

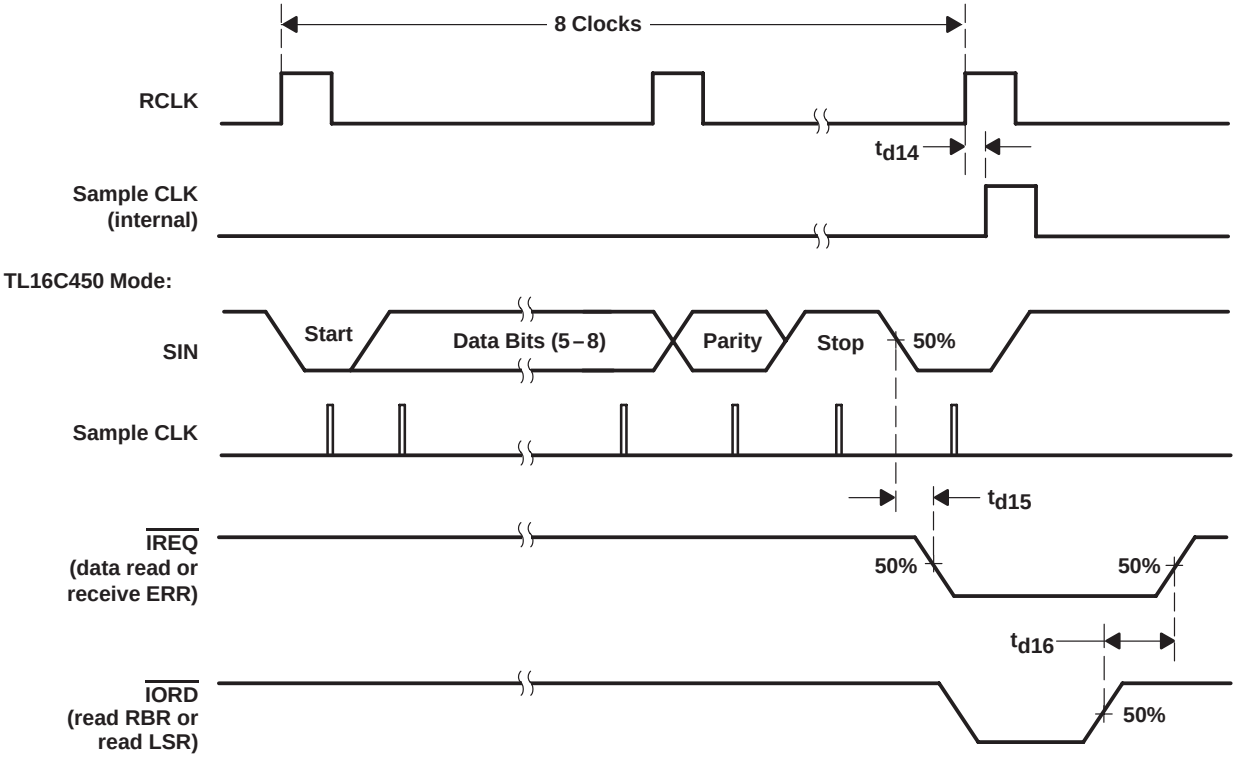


Figure 5. Receiver Timing Waveforms

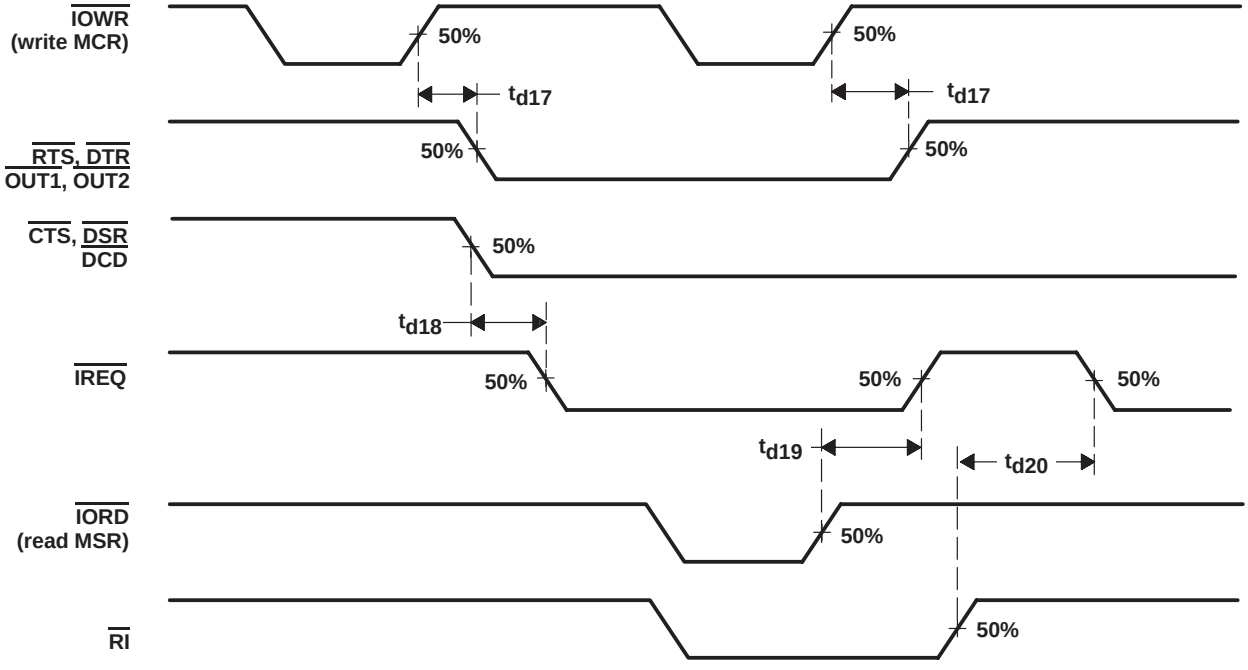
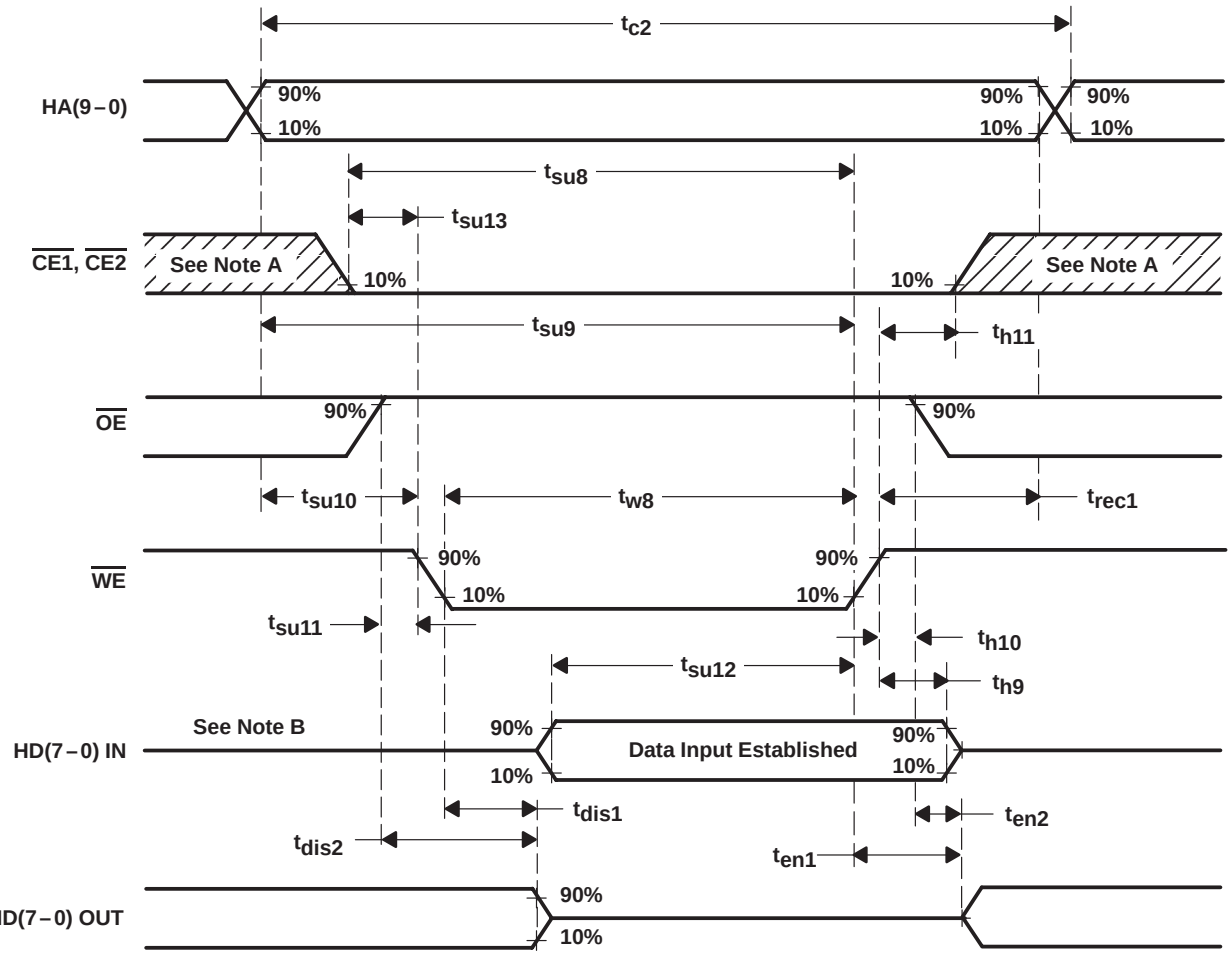


Figure 6. Modem Control Timing Waveforms

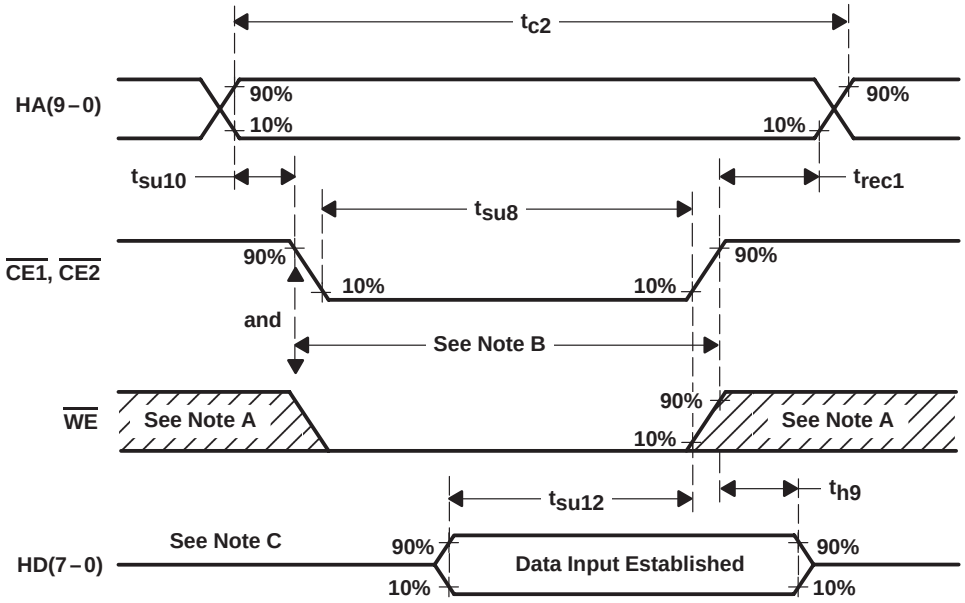
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The hatched portion may be either high or low.
B. When the data I/O terminal is in the output state, no signals shall be applied to HD(7 – 0) by the system.

Figure 7. Host CPU Attribute Memory Write Timing Waveforms ($\overline{WE}$ Control)

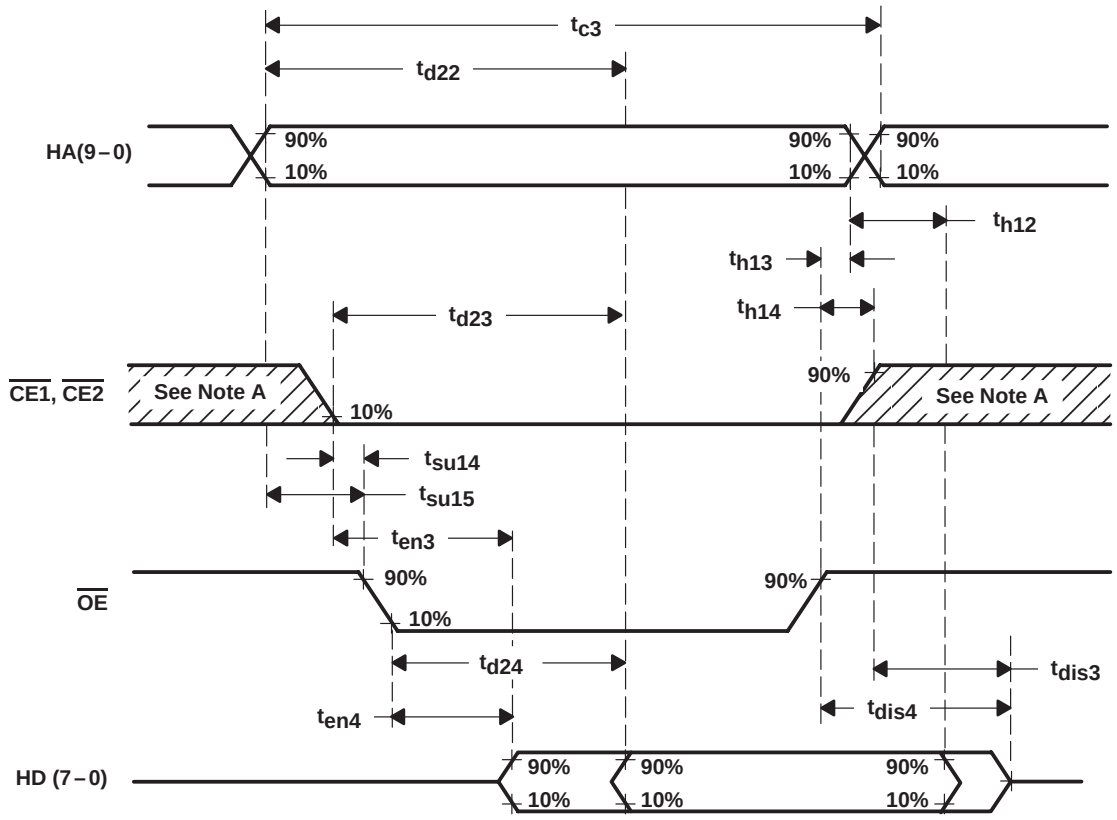
PARAMETER MEASUREMENT INFORMATION



NOTES: A. The hatched portion may be either high (H) or low (L).
B. $\overline{OE}$ must be high (H).
C. When the data I/O terminal is in the output state, no signals shall be applied to HD(7–0) by the system.

Figure 8. Host CPU Attribute Memory Write Timing Waveforms ($\overline{CE}$ Control)

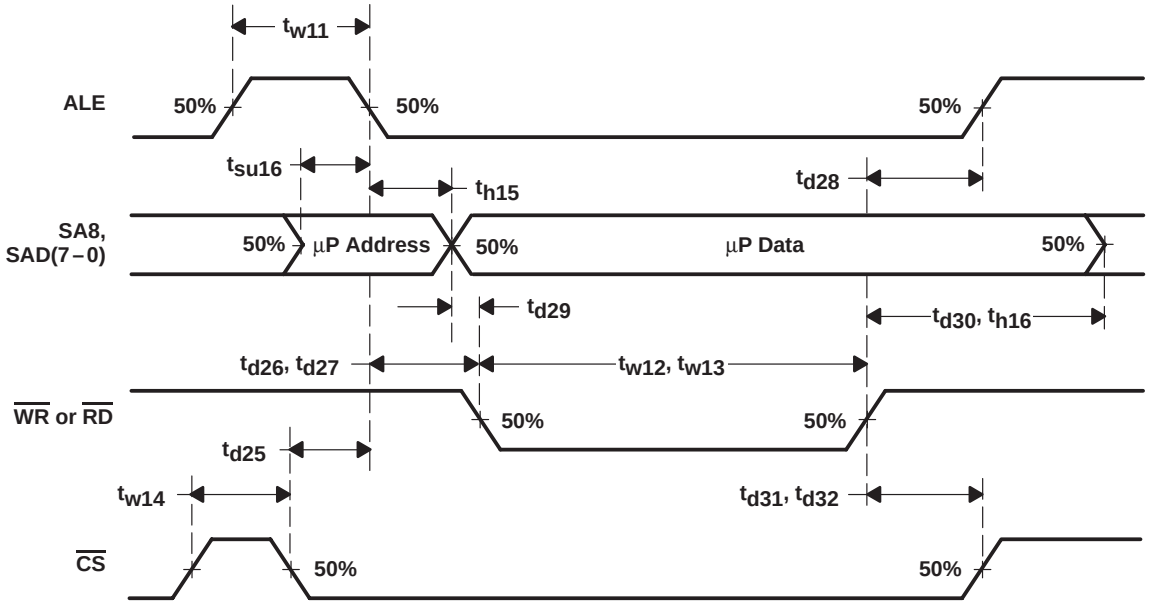
PARAMETER MEASUREMENT INFORMATION



NOTE A: The shaded portion may be either high or low.

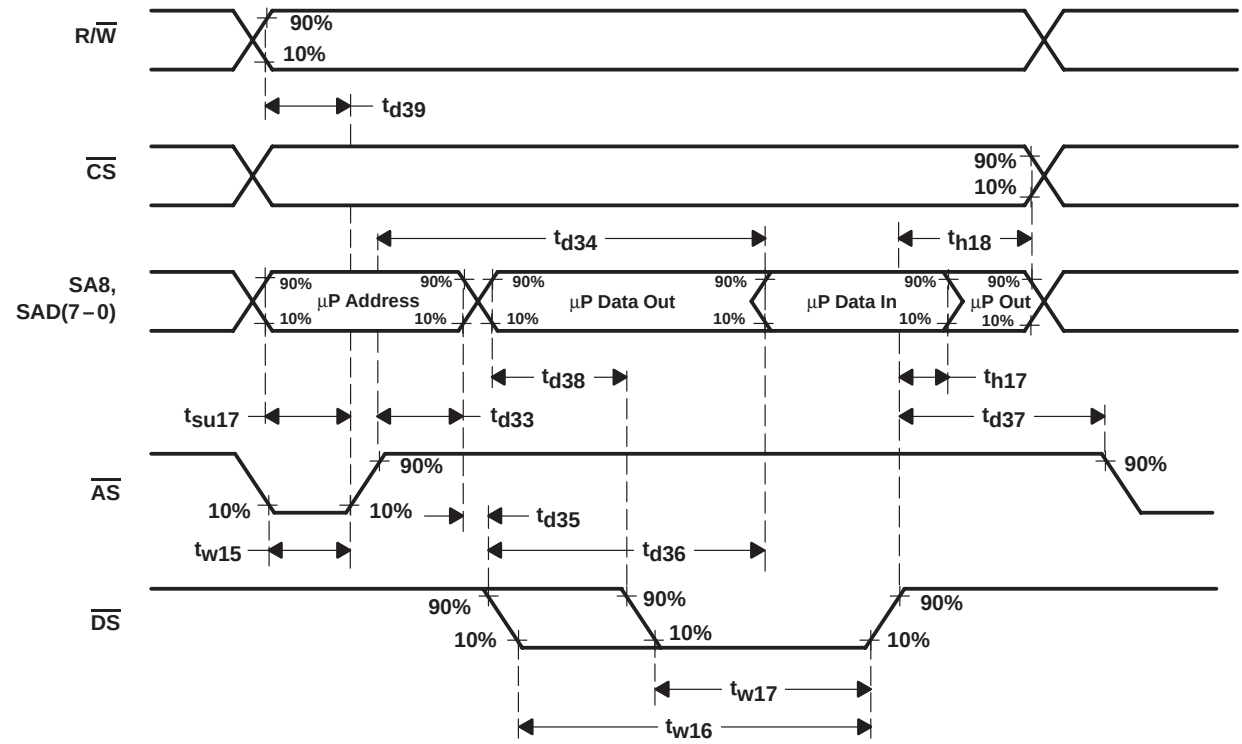
Figure 9. Host CPU Attribute Memory Read Timing Waveforms

PARAMETER MEASUREMENT INFORMATION



NOTE A: This figure is from the microprocessor perspective, not from the UART perspective.

Figure 10. Subsystem Intel Mode Timing Waveforms



NOTE A: This figure is from the microprocessor perspective, not from the UART perspective.

Figure 11. Subsystem Zilog Mode Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

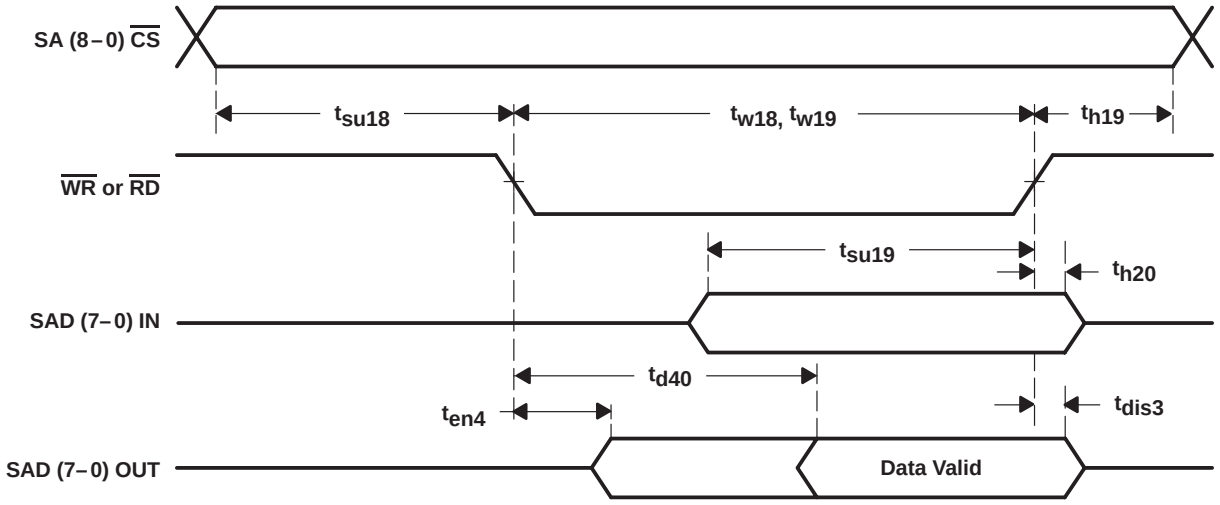


Figure 12. Subsystem Intel Nonmultiplexed Timing Waveforms

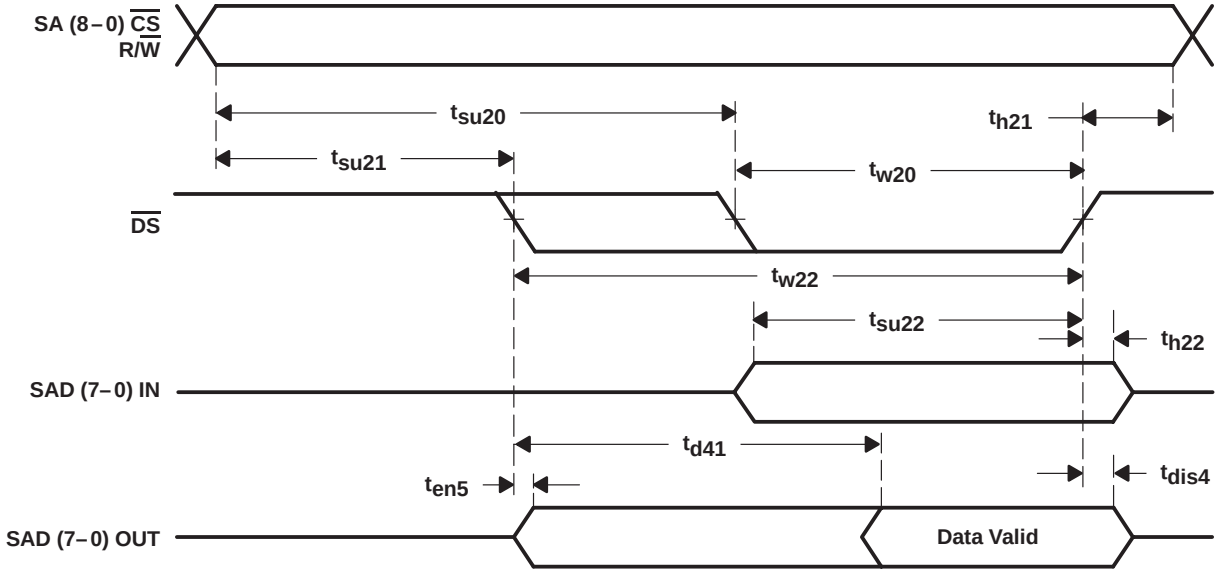


Figure 13. Subsystem Zilog Nonmultiplexed Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

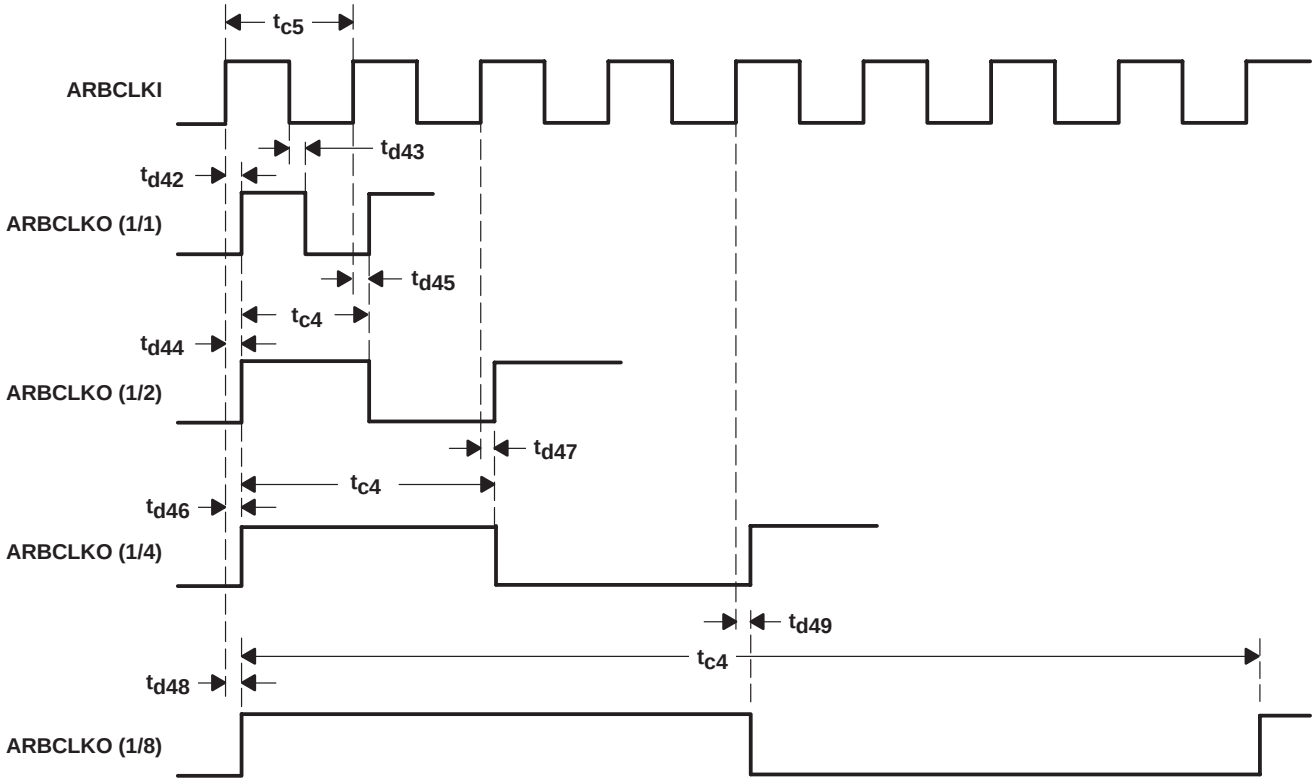


Figure 14. Arbitration Clock Timing Waveforms

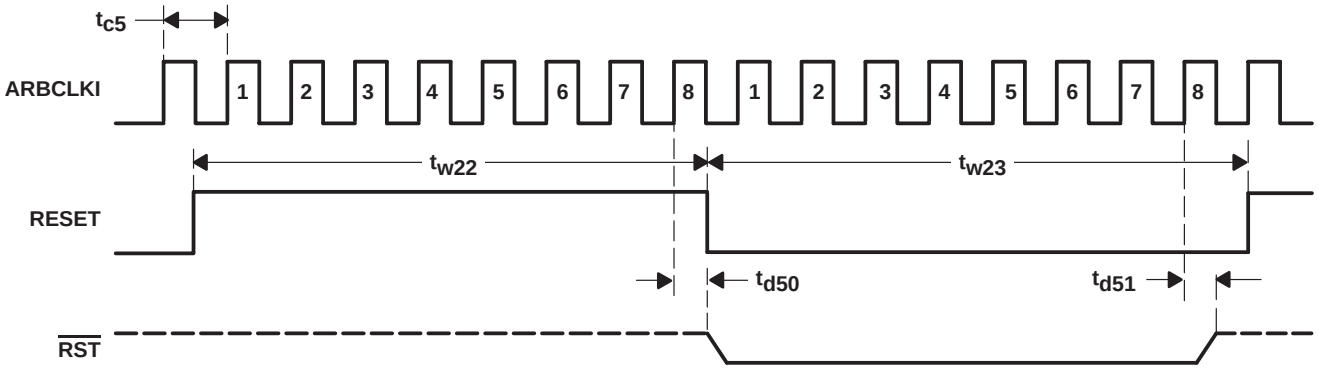


Figure 15. Reset Timing Waveforms

PARAMETER MEASUREMENT INFORMATION

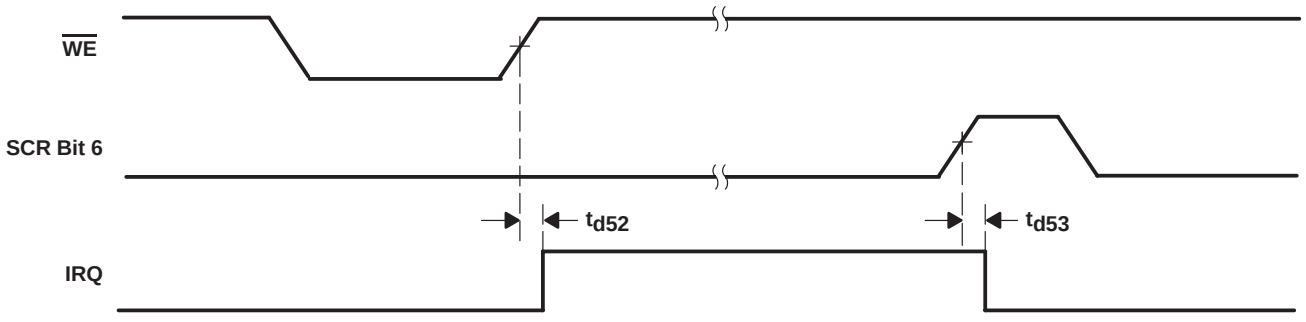


Figure 16. IRQ Timing Waveforms

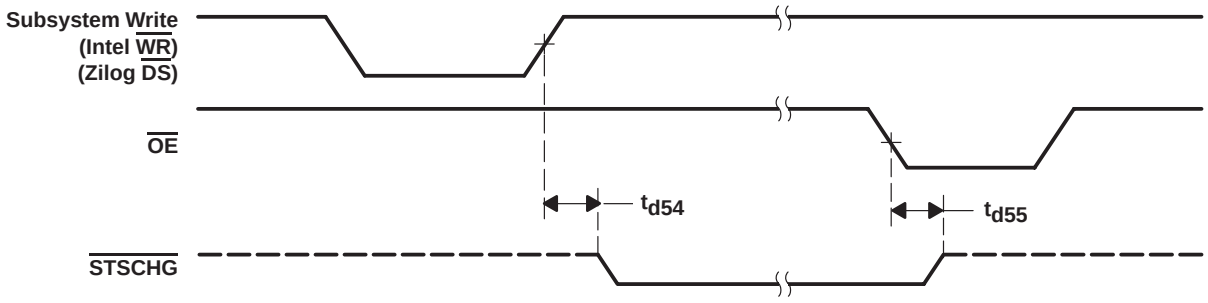


Figure 17. STSCHG Timing Waveforms

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