SGM58031
Ultra-Small, Low-Power, 16-Bit ADC with Internal Reference

GENERAL DESCRIPTION

The SGM58031 is a low-power, 16-bit, precision, delta-sigma (ΔΣ) analog-to-digital converter (ADC). It operates from a 3V to 5.5V supply.

The SGM58031 contains an on-chip reference and oscillator. It has an I^2C-compatible interface, and it can select four I^2C slave addresses. The date rate of the filter is up to 960SPS. The SGM58031 has an on-chip PGA, which can provide input ranges to as low as ±256mV from the power supply.

The input multiplexer supports 4 single-ended inputs or 2 differential inputs configuration.

The SGM58031 is available in Green MSOP-10 and TDFN-3×3-10L packages. It operates over an ambient temperature range of -40℃ to +125℃.

FEATURES

- **Single-Supply Voltage Range: 3V to 5.5V**
  - **I^2C Bus Voltage Range: 3V to 5.5V**
- **Low Quiescent Current:**
  - **Continuous Mode: 255μA (TYP)**
  - **Power-Down Mode: 0.8μA (TYP)**
- **Selectable Date Rates: 6.25SPS to 960SPS**
- **Input Multiplexer**
  - **4 Single-Ended Inputs or 2 Differential Inputs**
- **Internal Programmable Gain Amplifier (PGA)**
- **Internal Voltage Reference and Oscillator**
- **Selectable Digital Comparator**
- **I^2C-Compatible Serial Interface**
- **Available in Green MSOP-10 and TDFN-3×3-10L Packages**

APPLICATIONS

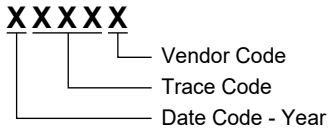
Portable Devices
Process Control
Battery Monitoring System
Temperature Measurement

PACKAGE/ORDERING INFORMATION

MODEL	PACKAGE DESCRIPTION	SPECIFIED TEMPERATURE RANGE	ORDERING NUMBER	PACKAGE MARKING	PACKING OPTION
SGM58031	MSOP-10	-40℃ to +125℃	SGM58031XMS10G/TR	SGM58031 XMS10 XXXXX	Tape and Reel, 4000
	TDFN-3×3-10L	-40℃ to +125℃	SGM58031XTD10G/TR	SGM 58031D XXXXX	Tape and Reel, 4000

MARKING INFORMATION

NOTE: XXXXX = Date Code, Trace Code and Vendor Code.



Green (RoHS & HSF): SG Micro Corp defines "Green" to mean Pb-Free (RoHS compatible) and free of halogen substances. If you have additional comments or questions, please contact your SGMICRO representative directly.

ABSOLUTE MAXIMUM RATINGS

Voltage Range (with Respect to GND)

V_{DD} ..... -0.3V to 5.5V

Analog Input Voltage..... -0.3V to 5.5V

SDA, SCL, ADDR, ALERT/RDY Voltage ..... -0.3V to 5.5V

Input Current (Momentary)..... 100mA

Input Current (Continuous) 10mA

Junction Temperature..... +150℃

Storage Temperature Range ..... -65℃ to +150℃

Lead Temperature (Soldering, 10s)..... +260℃

ESD Susceptibility

HBM..... 4000V

CDM 1000V

RECOMMENDED OPERATING CONDITIONS

Operating Temperature Range ..... -40℃ to +125℃

OVERSTRESS CAUTION

Stresses beyond those listed in Absolute Maximum Ratings may cause permanent damage to the device. Exposure to absolute maximum rating conditions for extended periods may affect reliability. Functional operation of the device at any conditions beyond those indicated in the Recommended Operating Conditions section is not implied.

ESD SENSITIVITY CAUTION

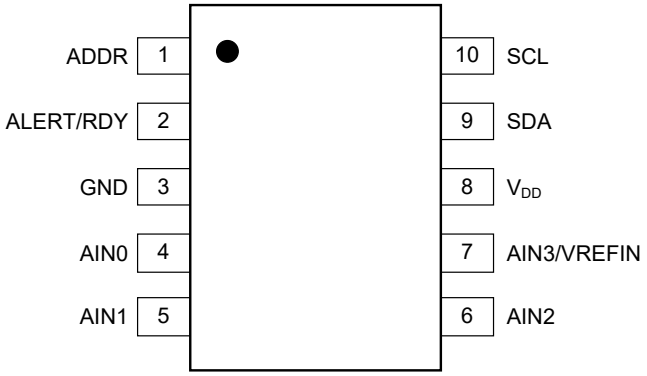
This integrated circuit can be damaged if ESD protections are not considered carefully. SGMICRO recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures can cause damage. ESD damage can range from subtle performance degradation to complete device failure. Precision integrated circuits may be more susceptible to damage because even small parametric changes could cause the device not to meet the published specifications.

DISCLAIMER

SG Micro Corp reserves the right to make any change in circuit design, or specifications without prior notice.

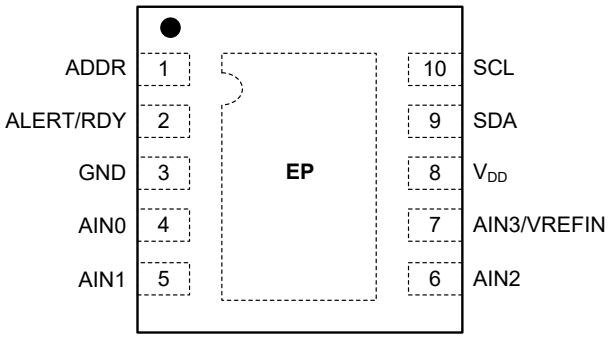
PIN CONFIGURATIONS

(TOP VIEW)



MSOP-10

(TOP VIEW)



TDFN-3×3-10L

PIN DESCRIPTION

PIN		NAME	TYPE (1)	FUNCTION
MSOP-10	TDFN-3×3-10L			
1	1	ADDR	DI	I^2C Address Selection Pin.
2	2	ALERT/RDY	DO	Digital Comparator Output/Conversion Ready Pin.
3	3	GND	G	Ground.
4	4	AIN0	AI	Positive Input of Differential Channel 1 or Input of Single-Ended Channel 1.
5	5	AIN1	AI	Negative Input of Differential Channel 1 or Input of Single-Ended Channel 2.
6	6	AIN2	AI	Positive Input of Differential Channel 2 or Input of Single-Ended Channel 3.
7	7	AIN3/VREFIN	AI	Negative Input of Differential Channel 2, or Input of Single-Ended Channel 4, or External Reference Input.
8	8	V_{DD}	P	Power Supply Pin. It can be operated from 3V to 5.5V
9	9	SDA	DIO	Serial Data Pin.
10	10	SCL	DI	Serial Clock Input Pin.
–	Exposed Pad	EP	–	Exposed pad should be soldered to PCB board and connected to GND.

NOTE:
1. AI = Analog Input, DI = Digital Input, DO = Digital Output, DIO = Digital Input and Output, P = Power, G = Ground.

ELECTRICAL CHARACTERISTICS

(V_{DD} = 3.3V, Full-Scale (FS) = ±2.048V, maximum and minimum specifications apply from T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Analog Input						
Full-Scale Input Voltage (1)		V_{IN} = (AIN_P) - (AIN_N)		±4.096/PGA		V
Analog Input Voltage		AIN_P or AIN_N to GND	GND		V_{DD}	V
Differential Input Impedance				See Table 1		
System Performance						
Resolution		No missing codes	16			Bits
Data Rate	DR			See Table 2		SPS
Data Rate Variation		All data rates	-6		6	%
Output Noise			See Table 3 and Table 4			
Integral Nonlinearity	INL	DR = 8SPS, FS = ±2.048V, best fit (99% of full-scale)		1	4	LSB
Offset Error		FS = ±2.048V, differential inputs		1	5	LSB
		FS = ±2.048V, single-ended inputs		2	8.5	
Offset Drift		FS = ±2.048V		0.005	0.06	LSB/℃
Offset Power-Supply Rejection		FS = ±2.048V		1.2		LSB/V
Gain Error (2)		FS = ±2.048V at +25℃		0.03	0.3	%
Gain Drift (3)		FS = ±0.256V		30		ppm/℃
		FS = ±2.048V		30	70	
		FS = ±6.144V (1)		30		
Gain Power-Supply Rejection				50	200	ppm/V
PGA Gain Match (2)		Match between any two PGA gains		0.1	0.28	%
Gain Match		Match between any two inputs		0.01	0.08	%
Offset Match		Match between any two gains		1	8.5	LSB
50/60Hz Rejection		FS = ±2.048V		95		dB
Channel-to-Channel Crosstalk		At DC and FS = ±2.048V, differential or single-ended inputs adjacent channels		90		dB
Common-Mode Rejection Ratio	CMRR	At DC and FS = ±0.256V		110		dB
		At DC and FS = ±2.048V		110		
		At DC and FS = ±6.144V (1)		110		
Internal Clock						
Frequency			386	410	434	kHz

NOTES:

1. The full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V be applied to this device.
2. It includes all errors from on-chip PGA and reference.
3. Gain temperature drift is defined as the maximum change of gain error measured over the specified temperature range. The gain error drift is calculated using the box method, as described by Equation: Gain Error Drift = (GE_{MAX} - GE_{MIN})/(T_{MAX} - T_{MIN}) where:

- GE_{MAX} and GE_{MIN} are the maximum and minimum gain errors, respectively.
- T_{MAX} and T_{MIN} are the maximum and minimum temperatures, respectively, over the temperature range -40℃ to +125℃.

ELECTRICAL CHARACTERISTICS (continued)

(V_{DD} = 3.3V, Full-Scale (FS) = ±2.048V, maximum and minimum specifications apply from T_A = -40℃ to +125℃, typical values are at T_A = +25℃, unless otherwise noted.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Reference							
Internal Reference					2.048		V
External Reference				0.5		2.5	V
External Reference Input Current		VREFIN = 2.5V, continuous mode			0.45		μA
Digital Input/Output							
High Input Voltage (4)	V_{IH}			0.7×V_{BUS}			V
Low Input Voltage (4)	V_{IL}					0.3×V_{BUS}	V
Low Output Voltage	V_{OL}	I_{OL} = 3mA			0.07	0.4	V
High Input Leakage Current (5)	I_{IH}	V_{IH} = 5.5V			0.1	1	μA
Low Input Leakage Current (5)	I_{IL}	V_{IL} = GND			0.1	1	μA
Power-Supply Requirements							
Power-Supply Voltage	V_{DD}			3		5.5	V
Supply Current	I_{DD}	V_{DD} = 5.5V	Power-down current at +25℃ (6)		0.8	1	μA
			Power-down current up to +125℃ (6)		1.8	3.8	
			Operating current at +25℃		255	320	
			Operating current up to +125℃		270	340	
Power Dissipation	P_D	V_{DD} = 5V			1.05		mW
		V_{DD} = 3.3V			0.6		

NOTES:

4. There are 2 scenarios: V_{DD} = 5V, V_{BUS} can be 3V to 5V; V_{DD} = 3.3V, V_{BUS} should be 3.3V. Note that V_{BUS} = 3V may cause leakage in some extreme conditions, and it's better to make it higher than 3.1V. For V_{BUS} = V_{DD}, V_{IL}/V_{IH} = 30%/70% of V_{BUS}. For V_{BUS} = 3.3V and V_{DD} = 5V, V_{IL}/V_{IH} = 20%/80% of V_{BUS}.

5. Meet the "loss of V_{DD}" requirement of I^2C fast mode. When V_{DD} is lost, the leakage drawn from the pin is controlled.

6. Power-down current increases to 2.3μA at +25℃ and 3.5μA at +125℃ when Config1 BUS_FLEX bit is set to '1'.

TIMING CHARACTERISTICS

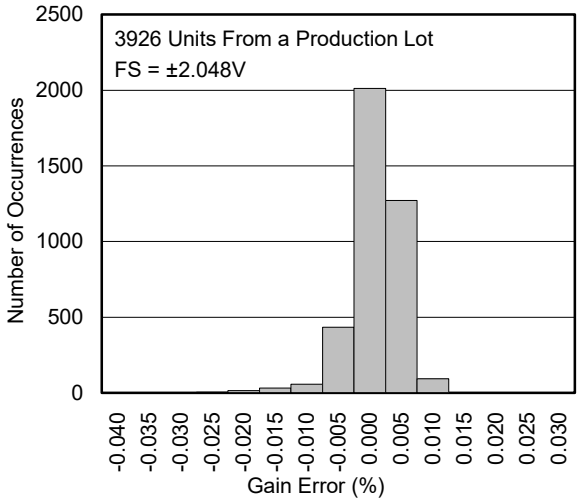
PARAMETER	SYMBOL	STANDARD MODE		FAST MODE		HIGH-SPEED MODE		UNITS
		MIN	MAX	MIN	MAX	MIN	MAX	
SCL Operating Frequency	f_{SCL}	0.01	0.1	0.01	0.4	0.01	3.4	MHz
Bus Free Time between START and STOP Condition	t_{BUF}	4700		600		160		ns
Hold Time after Repeated START Condition. After This Period, the First Clock is Generated.	t_{HDSTA}	4000		600		160		ns
Repeated START Condition Setup Time	t_{SUSTA}	4700		600		160		ns
Stop Condition Setup Time	t_{SUSTO}	4000		600		160		ns
Data Hold Time	t_{HDDAT}	0		0		0		ns
Data Setup Time	t_{SUDAT}	250		100		10		ns
SCL Clock Low Period	t_{LOW}	4700		1300		160		ns
SCL Clock High Period	t_{HIGH}	4000		600		60		ns
Clock/Data Fall Time (1)	t_F		300		300		160	ns
Clock/Data Rise Time	t_R		1000		300		160	ns

NOTE:
1. t_F (MIN) for SDA output is 20ns for normal/fast mode and 10ns for high-speed mode. Glitch filter capability is 50ns for normal/fast mode and 10ns for high-speed mode.

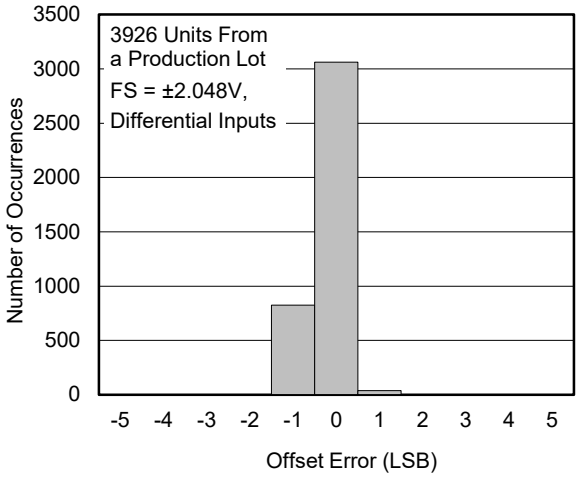
TYPICAL PERFORMANCE CHARACTERISTICS

T_A = +25℃, V_{DD} = 3.3V, Data Rate = 200SPS and Full-Scale (FS) = ±2.048V, unless otherwise noted.

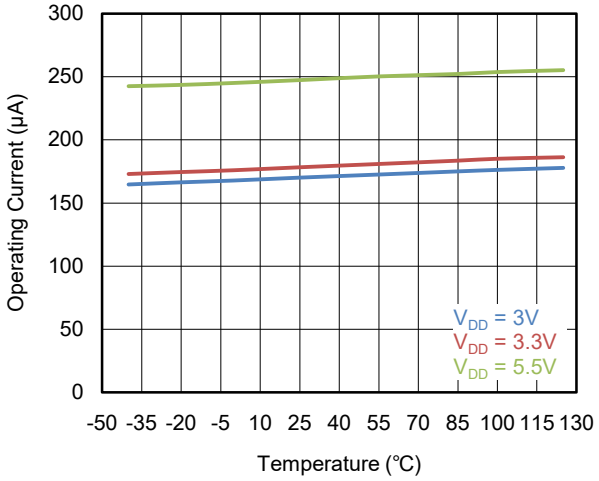
Gain Error Histogram



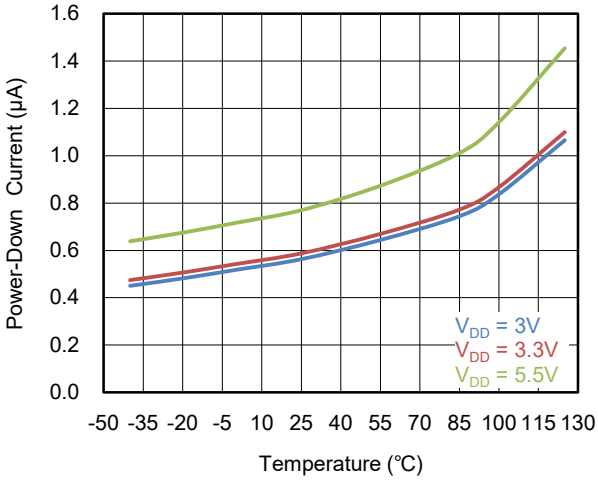
Offset Error Histogram



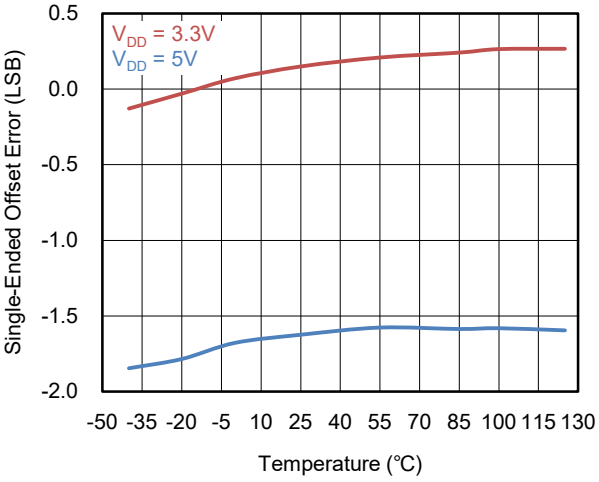
Operating Current vs. Temperature



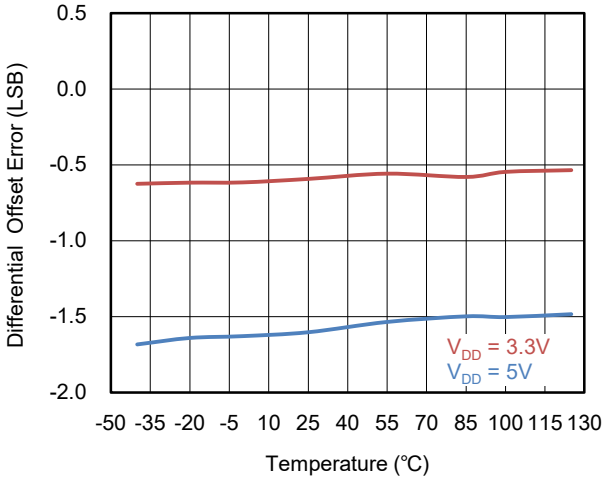
Power-Down Current vs. Temperature



Single-Ended Offset Error vs. Temperature



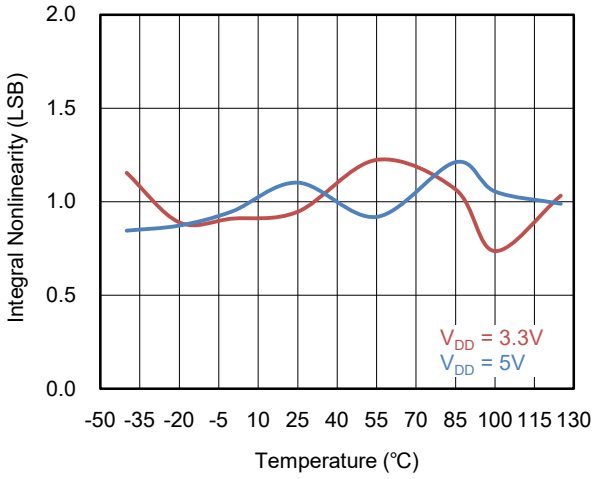
Differential Offset Error vs. Temperature



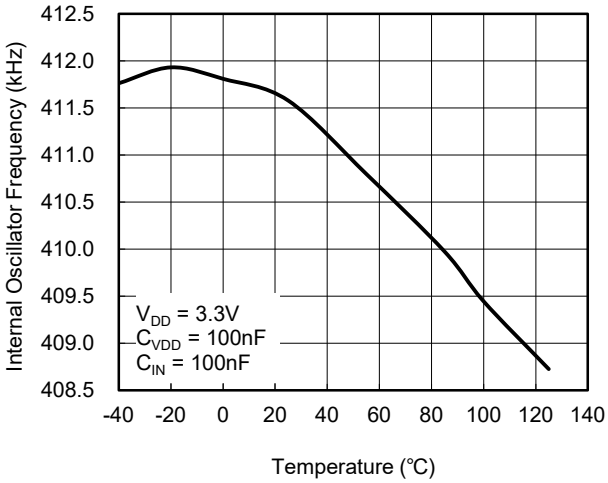
TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V, Data Rate = 200SPS and Full-Scale (FS) = ±2.048V, unless otherwise noted.

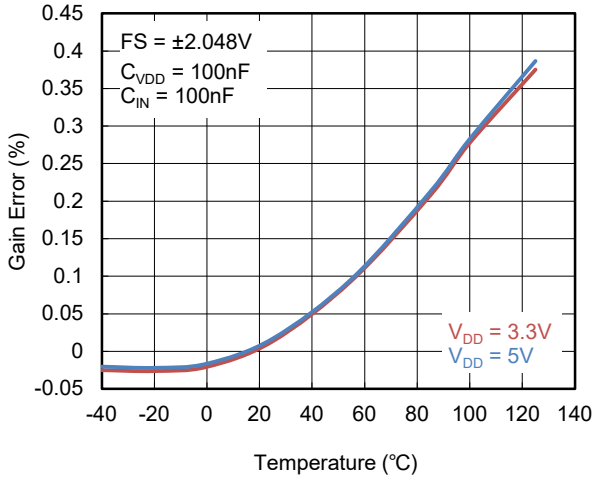
INL vs. Temperature



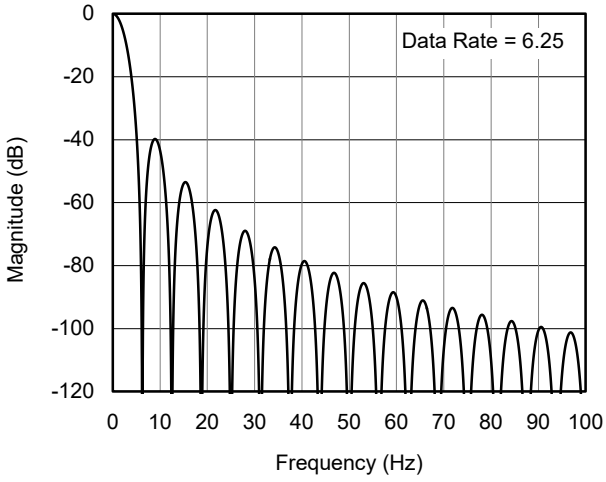
Internal Oscillator Frequency vs. Temperature



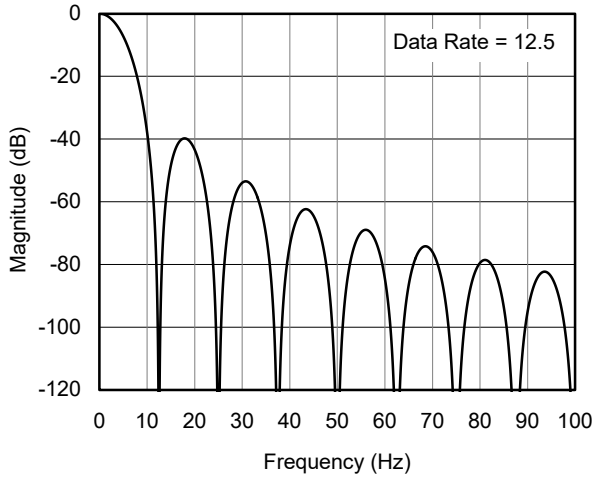
Gain Error vs. Temperature



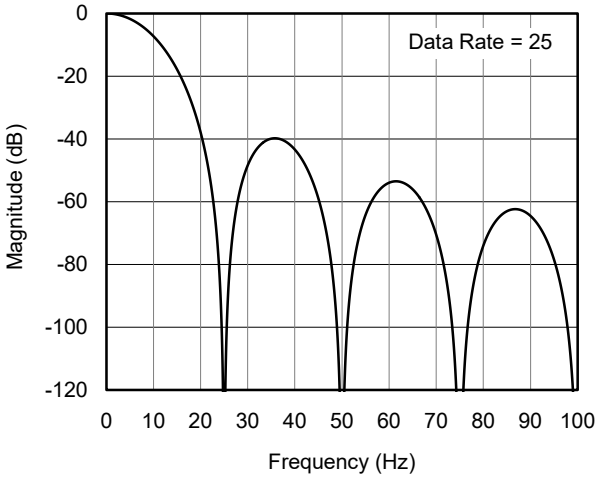
Filter Response



Filter Response

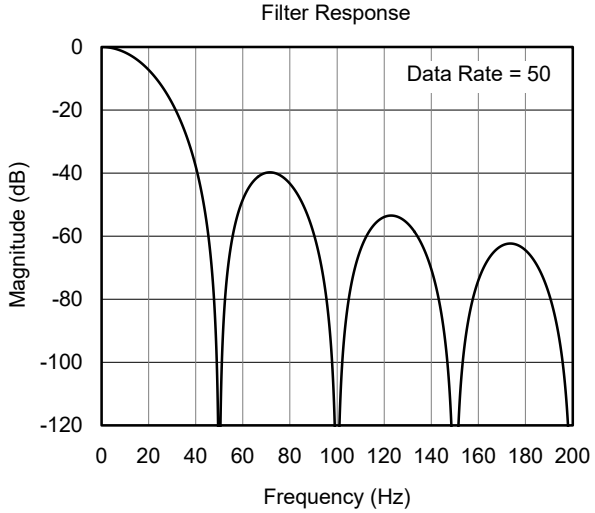


Filter Response



TYPICAL PERFORMANCE CHARACTERISTICS (continued)

T_A = +25℃, V_{DD} = 3.3V, Data Rate = 200SPS and Full-Scale (FS) = ±2.048V, unless otherwise noted.



DETAILED DESCRIPTION

Analog Inputs

Table 1. Differential Input Impedance

FS (V)	Differential Input Impedance
±6.144V (1)	37.5MΩ
±4.096V (1)	25MΩ
±2.048V	12.5MΩ
±1.024V	6.25MΩ
±0.512V	6.25MΩ
±0.256V	6.25MΩ

NOTE: 1. FS = Full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V be applied to this device.

Data Rate

Table 2. ADC Output Data Rate (SPS)

DR[2:0] Bits in Config Register	DR_SEL Bit in Config1 Register	
	DR_SEL = 0	DR_SEL = 1
000	6.25Hz	7.5Hz
001	12.5Hz	15Hz
010	25Hz	30Hz
011	50Hz	60Hz
100	100Hz	120Hz
101	200Hz	240Hz
110	400Hz	480Hz
111	800Hz	960HZ

ADC Noise

Table 3. ADC Noise with Internal Reference (RMS in μV)

DR / FS	800	400	200	100	50	25	12.5	6.25
6.144	187.5	187.5	187.5	187.5	187.5	187.5	187.5	187.5
4.096	125	125	125	125	125	125	125	125
2.048	62.5	62.5	62.5	62.5	62.5	62.5	62.5	62.5
1.024	31.25	31.25	31.25	31.25	31.25	31.25	31.25	31.25
0.512	15.62	15.62	15.62	15.62	15.62	15.62	15.62	15.62
0.256	7.81	7.81	7.81	7.81	7.81	7.81	7.81	7.81

Table 4. ADC ENOB (ENOB = (20log (FS/Noise_RMS) - 1.76)/6.02)

DR / FS	800	400	200	100	50	25	12.5	6.25
6.144	16	16	16	16	16	16	16	16
4.096	16	16	16	16	16	16	16	16
2.048	16	16	16	16	16	16	16	16
1.024	16	16	16	16	16	16	16	16
0.512	16	16	16	16	16	16	16	16
0.256	16	16	16	16	16	16	16	16

REGISTER MAPS

Register Address

Table 5. Register Address

Address	Register
0x0	Conversion Register
0x1	Config Register
0x2	Lo_Thresh Register
0x3	Hi_Thresh Register
0x4	Config1 Register
0x5	Chip_ID Register
0x6	GN_Trim1 for EXT_REF Register

Pointer Register

Table 6. Pointer Register Byte (Write-Only)

MSB							LSB
Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
0	0	0	0	0	Register Address		

Conversion Register

Table 7. 16-Bit Conversion Register (Read-Only)

MSB															LSB
Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
D15	D14	D13	D12	D11	D10	D9	D8	D7	D6	D5	D4	D3	D2	D1	D0

NOTE: Default Value = 0000h.

REGISTER MAPS (continued)

Config Register

Table 8. Config Register Details (Read/Write)

BITS	NAME	DESCRIPTION	COMMENT	DEFAULT VALUE
D[15]	OS	Operational Status (Single-Shot Conversion Start) A write status: 0 = No effect 1 = Start a single conversion in power-down mode A read status: 0 = A conversion is being performed currently 1 = A conversion is not being performed currently		
D[14:12]	MUX[2:0]	Input Multiplexer (MUX) Configuration 000 = AIN_P = AIN0 and AIN_N = AIN1 (default) 001 = AIN_P = AIN0 and AIN_N = AIN3 010 = AIN_P = AIN1 and AIN_N = AIN3 011 = AIN_P = AIN2 and AIN_N = AIN3 100 = AIN_P = AIN0 and AIN_N = GND 101 = AIN_P = AIN1 and AIN_N = GND 110 = AIN_P = AIN2 and AIN_N = GND 111 = AIN_P = AIN3 and AIN_N = GND		000
D[11:9]	PGA[2:0]	Programmable Gain Amplifier (PGA) Configuration 000 = FS = ±6.144V (1) 001 = FS = ±4.096V (1) 010 = FS = ±2.048V (default) 011 = FS = ±1.024V 100 = FS = ±0.512V 101 = FS = ±0.256V 110 = FS = ±0.256V 111 = FS = ±0.256V		010
D[8]	MODE	Operating Mode 0 = Continuous conversion mode 1 = Power-down single-shot mode (default)		1
D[7:5]	DR[2:0]	Data Rate	These bits control the data rate setting. See Table 2	100
D[4]	COMP_MODE	Comparator Mode 0 = A traditional comparator with hysteresis (default) 1 = A window comparator		0
D[3]	COMP_POL	Comparator Polarity (Control the Polarity of the ALERT/RDY Pin) 0 = Active low (default) 1 = Active high		0
D[2]	COMP_LAT	Latching Comparator 0 = Non-latching comparator (default) 1 = Latching comparator		0
D[1:0]	COMP_QUE[1:0]	Comparator Queue and Disable Function 00 = Assert after one conversion 01 = Assert after two conversions 10 = Assert after four conversions 11 = Disable comparator (default)		11

NOTES:

1. Default Value = 8583h.

2. FS = Full-scale range of the ADC scaling. In any event, it should not exceed V_{DD} + 0.3V be applied to this device.

DETAILED DESCRIPTION (continued)

Lo_Thresh and Hi_Thresh Registers

Table 9. Lo_Thresh and Hi_Thresh Registers (Read/Write)

Lo_Thresh Register							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Lo_Thresh15	Lo_Thresh14	Lo_Thresh13	Lo_Thresh12	Lo_Thresh11	Lo_Thresh10	Lo_Thresh9	Lo_Thresh8
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Lo_Thresh7	Lo_Thresh6	Lo_Thresh5	Lo_Thresh4	Lo_Thresh3	Lo_Thresh2	Lo_Thresh1	Lo_Thresh0
Hi_Thresh Register							
Bit 15	**Bit 14**	**Bit 13**	**Bit 12**	**Bit 11**	**Bit 10**	**Bit 9**	**Bit 8**
Hi_Thresh15	Hi_Thresh14	Hi_Thresh13	Hi_Thresh12	Hi_Thresh11	Hi_Thresh10	Hi_Thresh9	Hi_Thresh8
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
Hi_Thresh7	Hi_Thresh6	Hi_Thresh5	Hi_Thresh4	Hi_Thresh3	Hi_Thresh2	Hi_Thresh1	Hi_Thresh0

NOTE: Lo_Thresh Default Value = 8000h, Hi_Thresh Default Value = 7FFFh.

Config1 Register

Table 10. 16-Bit Config1 Register Details

BITS	NAME	DESCRIPTION	COMMENT	DEFAULT VALUE
D[15:9]	N/A			
D[8]	PD	Writing '1' to PD powers down this part, and this PD bit is automatically cleared internally. Another continuous/single conversion can be carried out again without the need to clear this bit.		0
D[7]	DR_SEL	0 = DR[2:0] = 000 ~ 111 for conversion rate of 6.25Hz, 12.5Hz, 25Hz, 50Hz, 100Hz, 200Hz, 400Hz and 800Hz (default) 1 = DR[2:0] = 000 ~ 111 for conversion rate of 7.5Hz, 15Hz, 30Hz, 60Hz, 120Hz, 240Hz, 480Hz and 960Hz		0
D[6]	BURNOUT	0 = No current sourced (default) 1 = Source a pair of 2μA current to selected pair of AINs		0
D[5]	INT_DIO	0 = None (default) 1 = Select internal diode as ADC input		0
D[4]	BUS_FLEX	0 = Disable leakage blocking circuit for the scenario that I^2C bus voltage is lower than V_{DD} of the part. The I^2C interface is still functional but V_{DD} sees leakage when $V_{BUS} < V_{DD}$ - 0.3V (default) 1 = Bus voltage can be lower than V_{DD} without causing leakage. The V_{DD} range is 3V to 5.5V and the I^2C bus voltage should be limited to 3V to 5.5V		0
D[3]	EXT_REF	0 = None (default) 1 = Use AIN3 as external reference for ADC		0
D[2:0]	N/A			

DETAILED DESCRIPTION (continued)

Chip_ID Register

Table 11. 16-Bit Chip_ID Register for Identifying Chip ID and Its Subversions (Read-Only)

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
N/A	N/A	N/A	ID[4:0]				
0	0	0	0	0	0	0	0
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
VER[2:0]			N/A	N/A	N/A	N/A	N/A
1	0	0	0	0	0	0	0

GN_Trim1 Register (When Using EXT_REF)

ADC gain coefficient for user selecting Config1 register EXT_REF bit as reference. We provide a default value and user is responsible for writing proper value to the register if they want to compensate external reference error. This register does not take effect when EXT_REF = 0 and internal reference is selected.

Table 12. GN_Trim1 Register

Bit 15	Bit 14	Bit 13	Bit 12	Bit 11	Bit 10	Bit 9	Bit 8
N/A	N/A	N/A	N/A	N/A	GN10	GN9	GN8
0	0	0	0	0	0	1	1
Bit 7	**Bit 6**	**Bit 5**	**Bit 4**	**Bit 3**	**Bit 2**	**Bit 1**	**Bit 0**
GN7	GN6	GN5	GN4	GN3	GN2	GN1	GN0
1	1	1	1	1	0	1	0

ADC GN_Trim1 register is an unsigned value. Default value used for final trimming is 1.3333 to compensate default ADC gain of 3/4. The value of GN[10:0] adds a constant to get the final gain trimming value.

GN_Trim1 + CONST = GN_Trim. The binary value of CONST is 1010011010110000, corresponding to a gain factor of 1.30225. After adding the default value of GN_Trim1 register (01111111010), the final default gain trimming value is 1.3333. The MAX final gain trimming value is 1.3547 when trimming register is all '1'; MIN value is 1.30225 when register is all '0'. This gives GN trimming a ±3% range and 32ppmFS step.

REVISION HISTORY

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

MARCH 2020 – REV.A to REV.A.1 **Page**

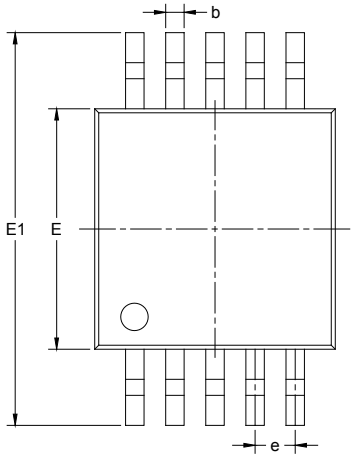
Update Figure 4 and Figure 5 12

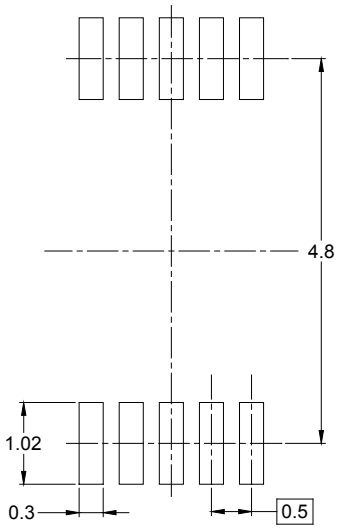
Changes from Original (DECEMBER 2019) to REV.A **Page**

Changed from product preview to production data ..... All

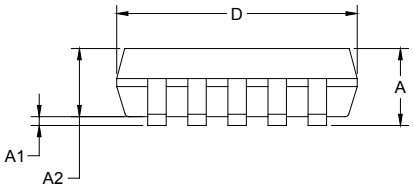
PACKAGE OUTLINE DIMENSIONS

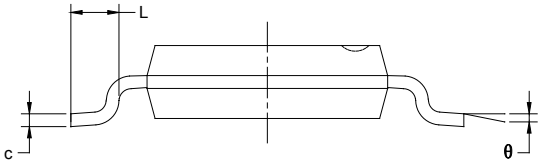
MSOP-10





RECOMMENDED LAND PATTERN (Unit: mm)

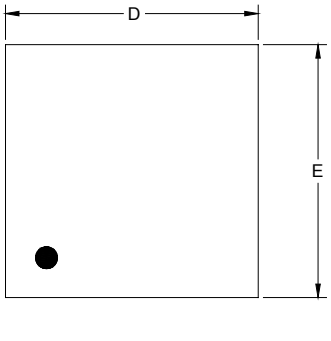




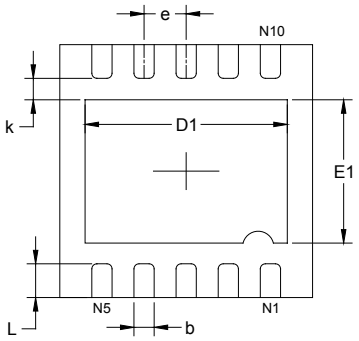
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.820	1.100	0.032	0.043
A1	0.020	0.150	0.001	0.006
A2	0.750	0.950	0.030	0.037
b	0.180	0.280	0.007	0.011
c	0.090	0.230	0.004	0.009
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
E1	4.750	5.050	0.187	0.199
e	0.500 BSC		0.020 BSC	
L	0.400	0.800	0.016	0.031
θ	0°	6°	0°	6°

PACKAGE OUTLINE DIMENSIONS

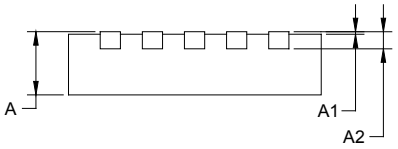
TDFN-3×3-10L



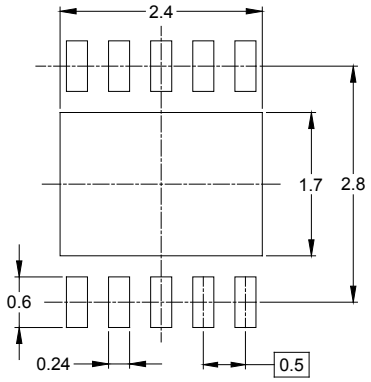
TOP VIEW



BOTTOM VIEW



SIDE VIEW

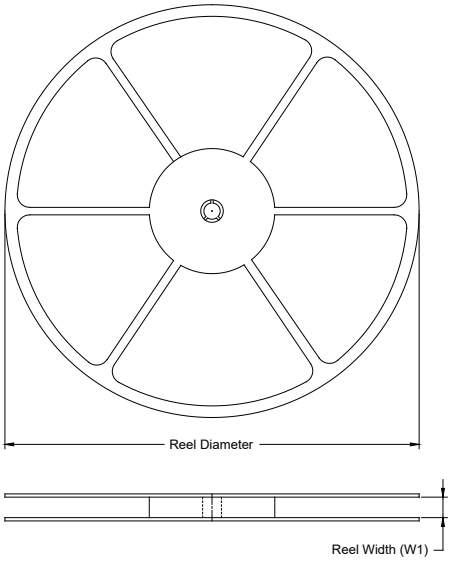


RECOMMENDED LAND PATTERN (Unit: mm)

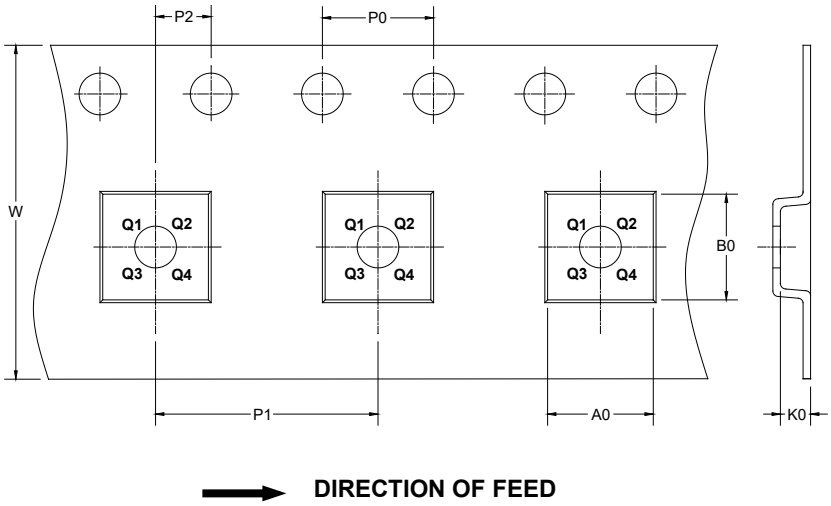
Symbol	Dimensions In Millimeters		Dimensions In Inches	
	MIN	MAX	MIN	MAX
A	0.700	0.800	0.028	0.031
A1	0.000	0.050	0.000	0.002
A2	0.203 REF		0.008 REF	
D	2.900	3.100	0.114	0.122
D1	2.300	2.600	0.091	0.103
E	2.900	3.100	0.114	0.122
E1	1.500	1.800	0.059	0.071
k	0.200 MIN		0.008 MIN	
b	0.180	0.300	0.007	0.012
e	0.500 TYP		0.020 TYP	
L	0.300	0.500	0.012	0.020

TAPE AND REEL INFORMATION

REEL DIMENSIONS



TAPE DIMENSIONS



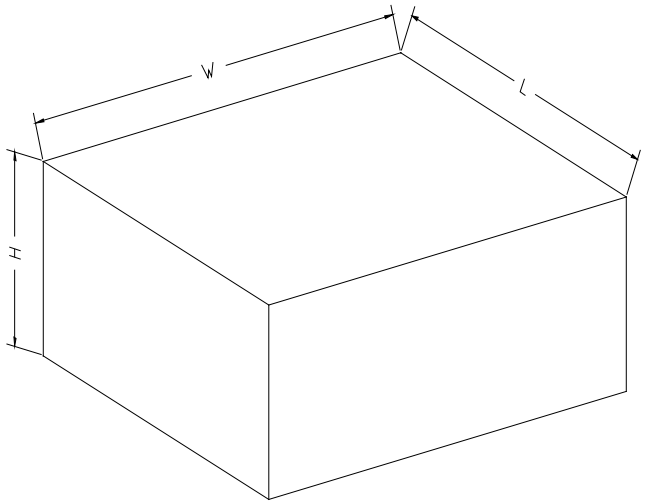
NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF TAPE AND REEL

Package Type	Reel Diameter	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P0 (mm)	P1 (mm)	P2 (mm)	W (mm)	Pin1 Quadrant
MSOP-10	13″	12.4	5.20	3.30	1.20	4.0	8.0	2.0	12.0	Q1
TDFN-3×3-10L	13″	12.4	3.35	3.35	1.13	4.0	8.0	2.0	12.0	Q1

DD0001

CARTON BOX DIMENSIONS



NOTE: The picture is only for reference. Please make the object as the standard.

KEY PARAMETER LIST OF CARTON BOX

Reel Type	Length (mm)	Width (mm)	Height (mm)	Pizza/Carton
13″	386	280	370	5

DD0002