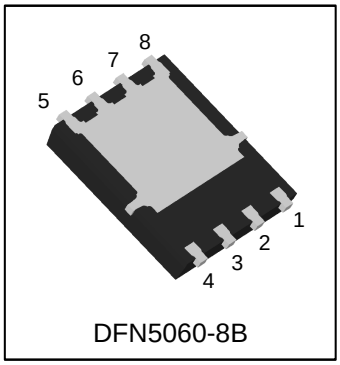
# LN73023DT1WG

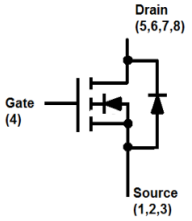
N-Channel Logic Level Enhancement Mode MOSFET



DFN5060-8B

## 1. FEATURES

- Low RDS(on) trench technology.
- Low thermal impedance.
- Fast switching speed.
- We declare that the material of product are Halogen Free and compliance with RoHS requirements.




## 2. APPLICATION

- Power Routing
- DC/DC Conversion
- Motor Drives

## 3. ORDERING INFORMATION

| Device | Marking | Shipping |
|---|---|---|
| LN73023DT1WG | LN73023 | 3000/Tape&Reel |

## 4. MAXIMUM RATINGS(Ta = 25ºC)

| Parameter | | Symbol | Limits | Unit |
|---|---|---|---|---|
| Drain−to−Source Voltage | | VDSS | 30 | V |
| Gate−to−Source Voltage | | VGS | ±20 | V |
| Continuous Drain Current(Note 1) | TC =25° C | ID | 100 | A |
| | TC =100° C | | 70 | |
| Pulsed Drain Current (Note 2) | | IDM | 400 | |
| Avalanche Current | | IAS | 44 | A |
| Avalanche Energy L=0.1mH | | EAS | 96.8 | mJ |
| Power Dissipation | TC =25° C | PD | 50 | W |
| | TC =100° C | | 20 | |
| Operating Junction Temperature | | TJ | −55 ~+150 | ℃ |
| Storage Temperature Range | | Tstg | −55 ~+150 | |

1.Package Limited.

2.Pulse width limited by maximum junction temperature.

3.50° C/W when mounted on a 1 $in^2$ pad of 2 oz copper.

## 5. THERMAL CHARACTERISTICS

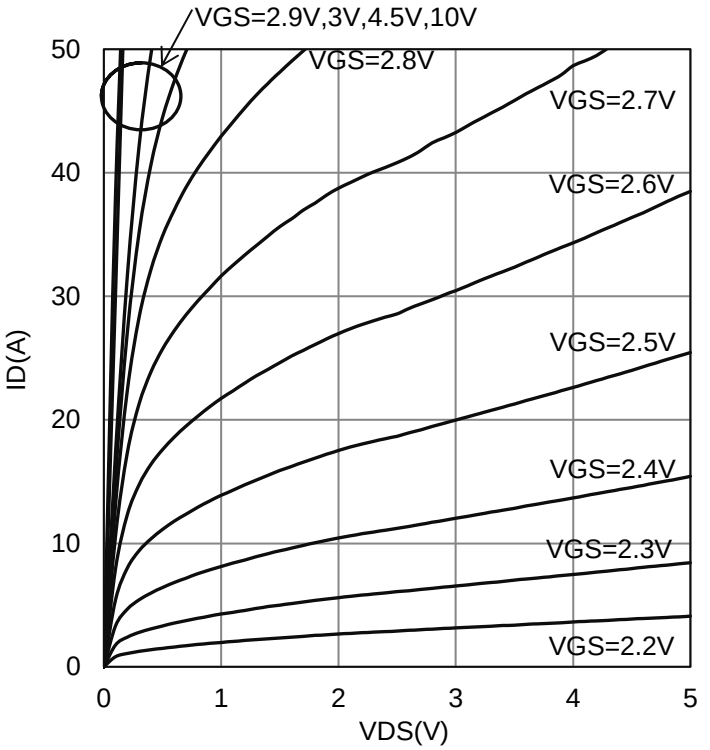
| Parameter | | Symbol | Limits | Unit |
|---|---|---|---|---|
| Maximum Junction-to-Ambient(Note 3) | t≤10s | RθJA | 25 | ℃/W |
| | Steady State | | 65 | |
| Maximum Junction-to-Case | | RθJC | 2.5 | ℃/W |

## 6. ELECTRICAL CHARACTERISTICS(Ta = 25ºC)

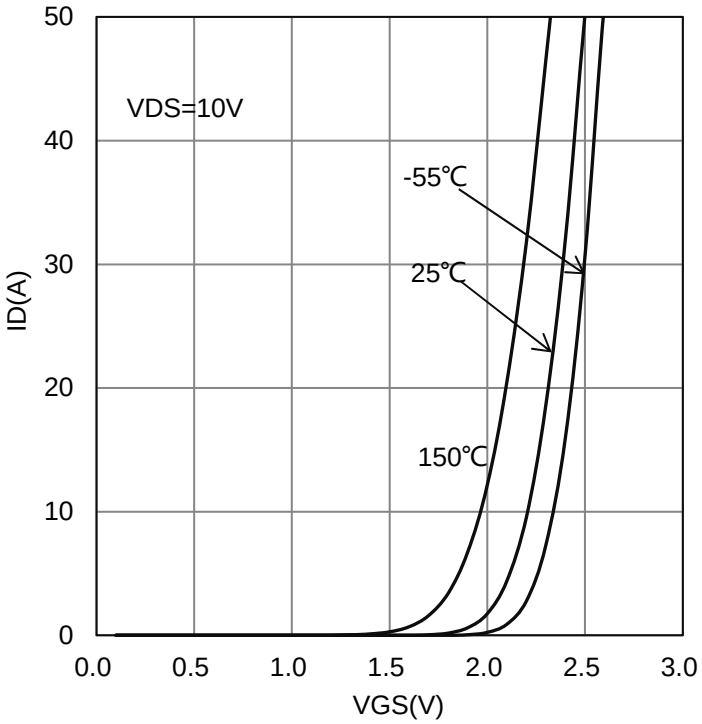
| Characteristic | | Symbol | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| Static | | | | | | |
| Drain-Source Breakdown Voltage<br>(VGS = 0V, ID = 250 uA) | | V(BR)DSS | 30 | - | - | V |
| Gate-Source Threshold Voltage<br>(VDS = VGS , ID = 250 uA) | | VGS(th) | 1 | 1.5 | 2.5 | V |
| Gate-Body Leakage<br>(VDS = 0 V, VGS = ±20 V) | | IGSS | - | - | ± 100 | nA |
| Zero Gate Voltage Drain Current<br>(VDS = 24 V, VGS = 0 V)<br>(VDS = 20 V, VGS = 0 V, TJ = 125°C) | | IDSS | -<br>- | -<br>- | 1<br>25 | μA |
| Drain-Source On-Resistance(Note 4)<br>(VGS = 10 V, ID = 25 A)<br>(VGS = 4.5 V, ID = 15 A) | | RDS(on) | -<br>- | 2<br>2.9 | 2.3<br>3.7 | mΩ |
| Dynamic | | | | | | |
| Total Gate Charge(VGS=10V) | (VDS = 15 V, VGS = 10 V,ID = 25 A) | Qg | - | 78 | - | nC |
| Total Gate Charge(VGS=4.5V) | | Qg | - | 40 | - | |
| Gate-Source Charge | | Qgs | - | 13 | - | |
| Gate-Drain Charge | | Qgd | - | 14 | - | |
| Input Capacitance | (VDS = 15 V, VGS = 0 V, f = 1 MHz) | Ciss | - | 4034 | - | pF |
| Output Capacitance | | Coss | - | 552 | - | |
| Reverse Transfer Capacitance | | Crss | - | 433 | - | |
| Turn-On Delay Time | (VDS = 15 V,ID = 1 A,VGS= 10 V,RGS =2.7Ω) | td(on) | - | 25 | - | ns |
| Rise Time | | tr | - | 16 | - | |
| Turn-Off Delay Time | | td(off) | - | 60 | - | |
| Fall Time | | tf | - | 25 | - | |
| Continuous Current | | IS | - | - | 100 | A |
| Pulsed Current | | ISM | - | - | 400 | A |
| Diode Forward Voltage<br>(IF =2.3A,VGS = 0V) | | VSD | - | - | 1.2 | V |
| Reverse Recovery Time | (IF = IS , dIF/dt = 100A /us) | trr | - | 35 | - | ns |
| Peak Reverse Recovery Current | | IRM(REC) | - | 200 | - | A |
| Reverse Recovery Charge | | Qrr | - | 25 | - | nC |

4.Pulse test: PW≤ 300μs duty cycle ≤ 2%.

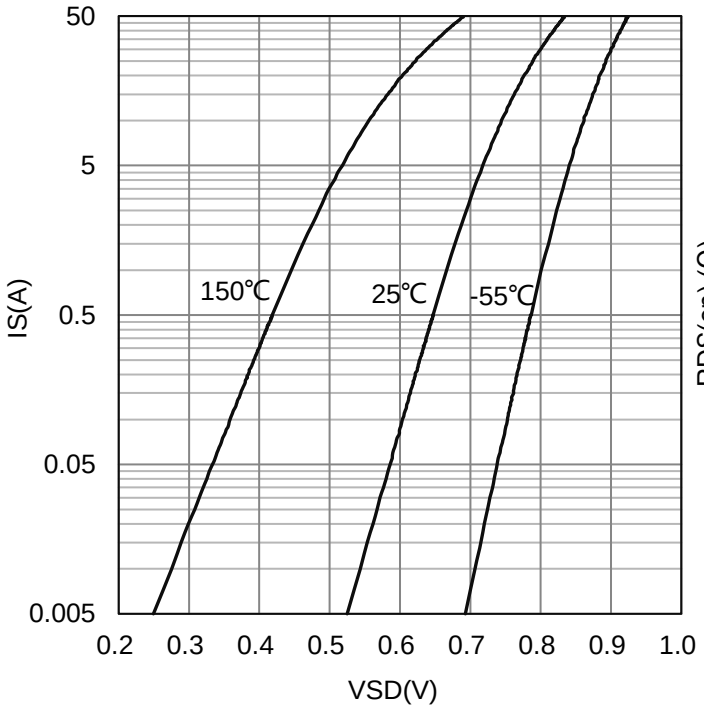
## 7.ELECTRICAL CHARACTERISTICS CURVES



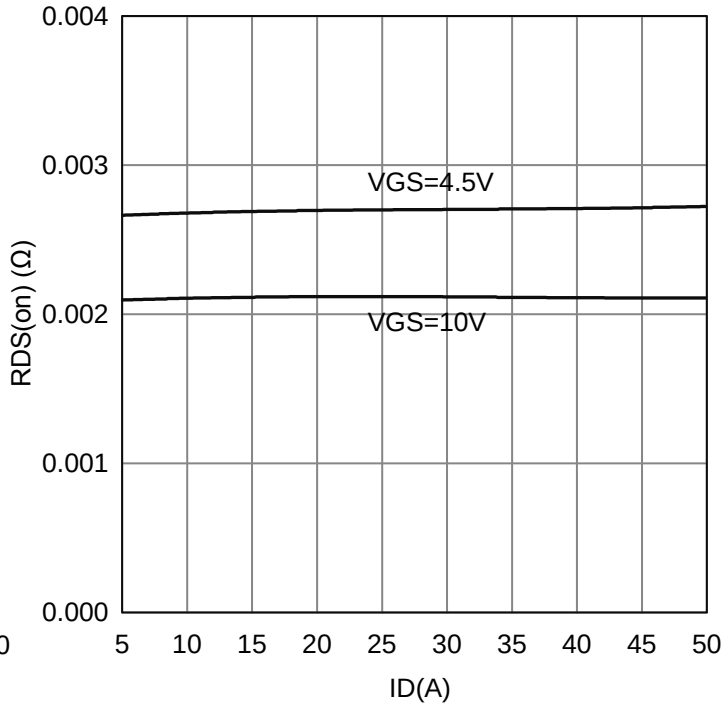

ID vs. VDS




ID vs. VGS

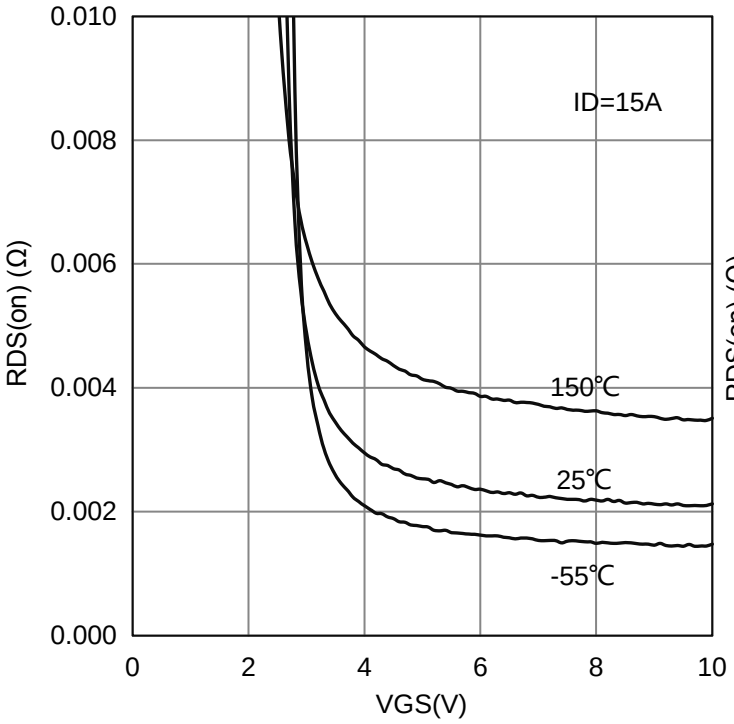



IS vs. VSD

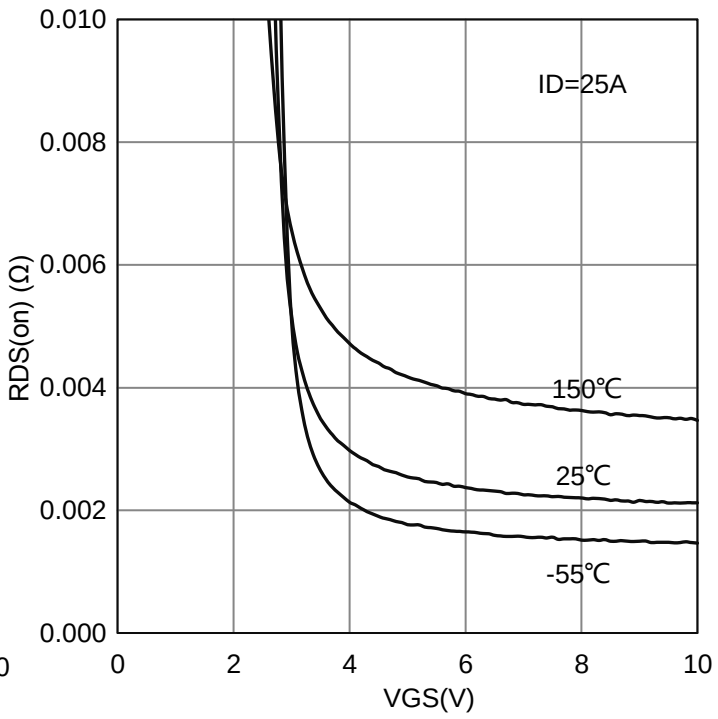



RDS(on) vs. ID

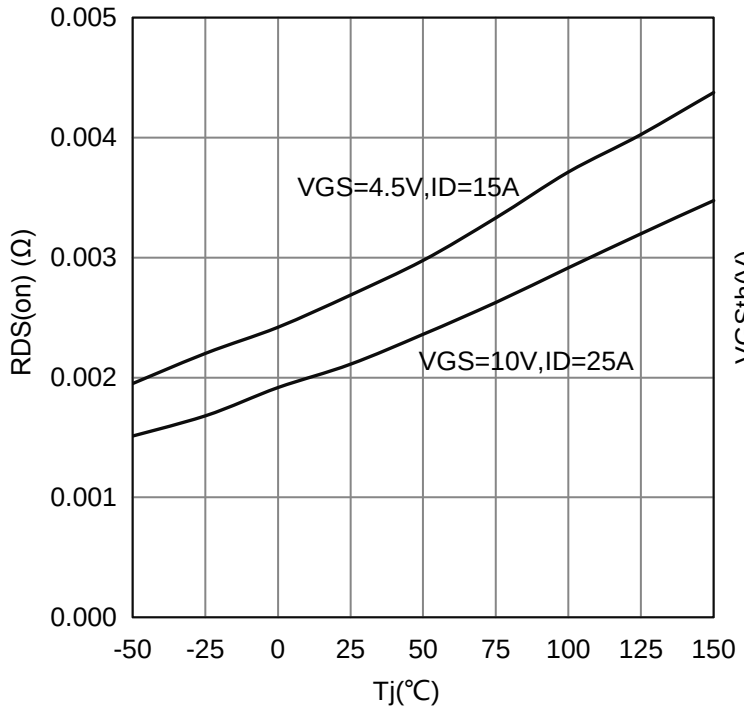
## 7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



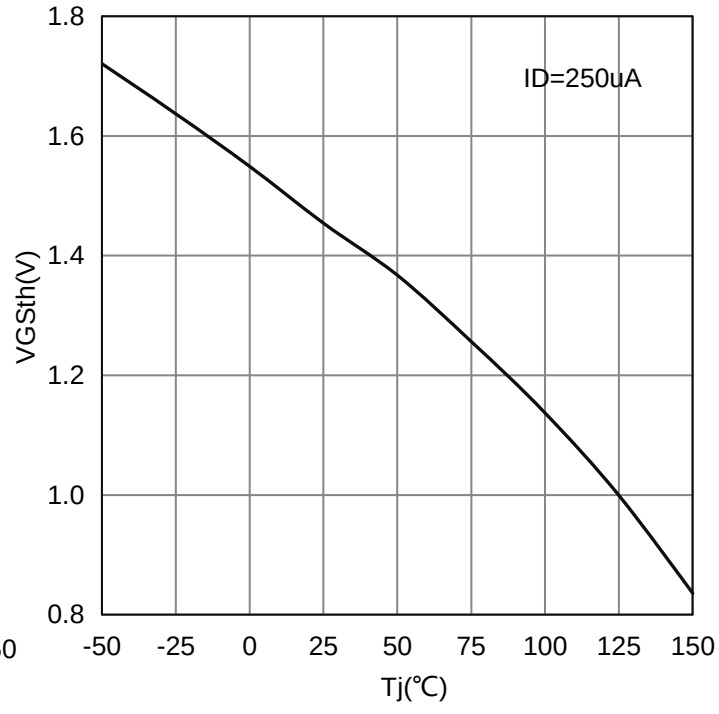

RDS(on) vs. VGS(ID=15A)




RDS(on) vs. VGS(ID=25A)

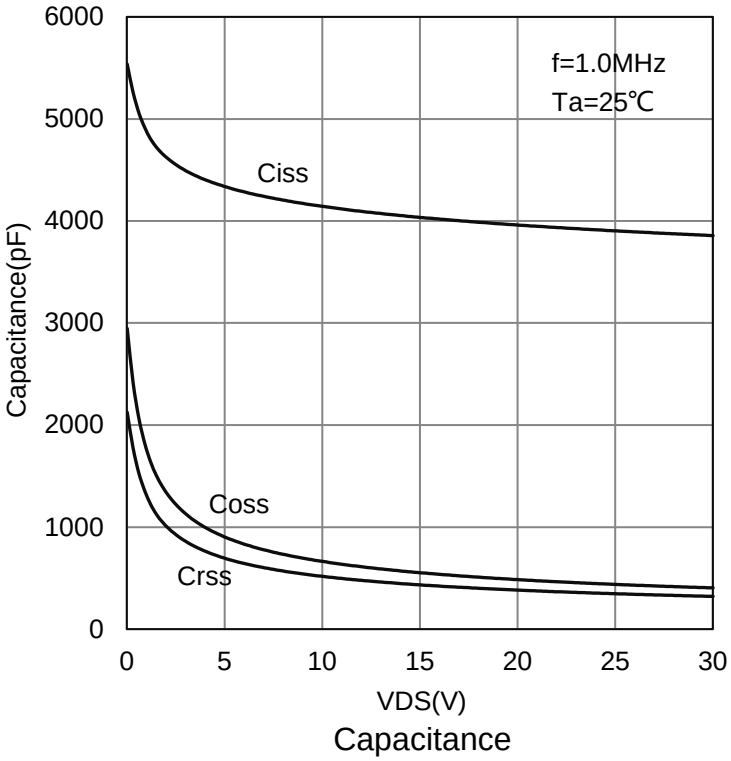



RDS(on) vs. Tj




VGSth vs. Tj

## 7.ELECTRICAL CHARACTERISTICS CURVES(Con.)



Capacitance

## 8.OUTLINE AND DIMENSIONS

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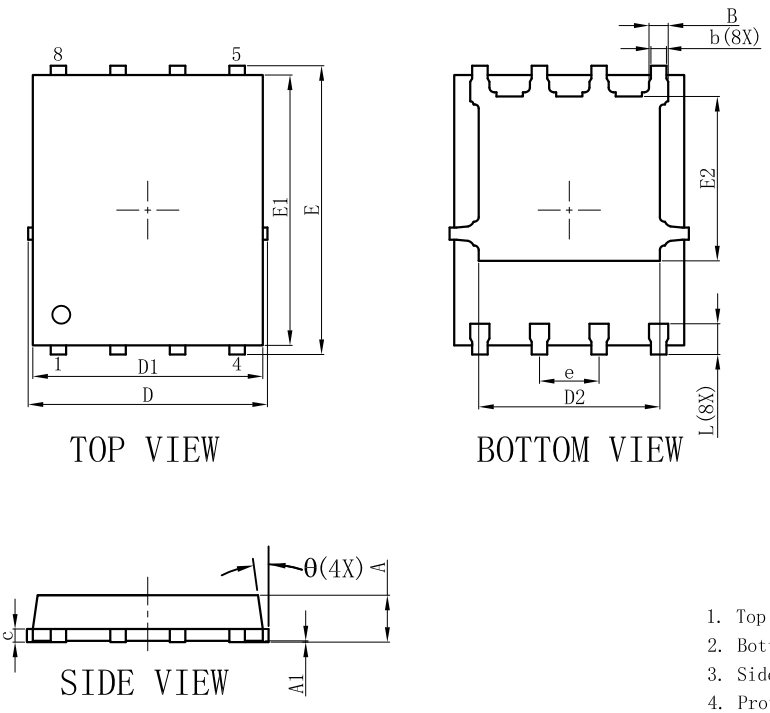
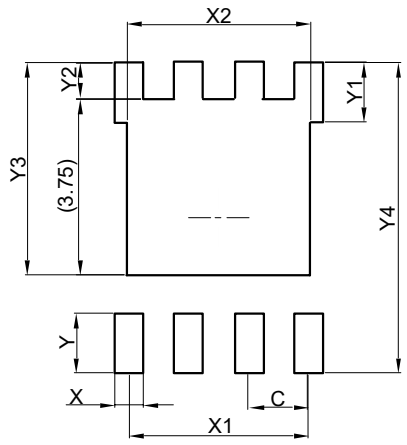



| DFN5060-8B | | | |
|---|---|---|---|
| DIM | MIN | NOR | MAX |
| A | 0.90 | 1.00 | 1.10 |
| A1 | 0.00 | 0.02 | 0.05 |
| E | 6.00 | 6.15 | 6.30 |
| E1 | 5.66 | 5.76 | 5.86 |
| E2 | 3.40 | 3.50 | 3.60 |
| D | 4.95 | 5.10 | 5.25 |
| D1 | 4.80 | 4.90 | 5.00 |
| D2 | 3.76 | 3.86 | 3.96 |
| b | 0.30 | 0.35 | 0.40 |
| B | 0.36 | 0.41 | 0.46 |
| L | 0.56 | 0.66 | 0.76 |
| e | 1.27BSC | | |
| c | 0.254REF. | | |
| θ | 0° | - | 12° |
| All Dimensions in mm | | | |

GENERAL NOTES

1. Top package surface finish Ra0.4±0.2um
2. Bottom package surface finish Ra0.7±0.2um
3. Side package surface finish Ra0.4±0.2um
4. Protrusion or Gate Burrs shall not exceed 0.05mm per side.
5. Offcenter Max0.038mm; Mismatch Max 0.038mm.

## 9.SOLDERING FOOTPRINT




| DFN5060-8B | |
|---|---|
| DIM | (mm) |
| C | 1.27 |
| X | 0.61 |
| X1 | 3.81 |
| X2 | 3.91 |
| Y | 1.27 |
| Y1 | 1.27 |
| Y2 | 0.77 |
| Y3 | 4.52 |
| Y4 | 6.61 |

## DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.

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