

LP3415ELT1G

20V P-Channel Enhancement-Mode MOSFET

1. FEATURES

- $V_{DS} = -20V$
- $R_{DS(ON)}, V_{GS@-4.5V}, I_{DS@-4A} = 60m\Omega$
- $R_{DS(ON)}, V_{GS@-2.5V}, I_{DS@-4A} = 75m\Omega$
- $R_{DS(ON)}, V_{GS@-1.8V}, I_{DS@-2A} = 85m\Omega$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.
- ESD Protected

2. APPLICATIONS

- Advanced trench process technology
- High density cell design for ultra low on-resistance.

3. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3415ELT1G	P15	3000/Tape&Reel
LP3415ELT3G	P15	10000/Tape&Reel

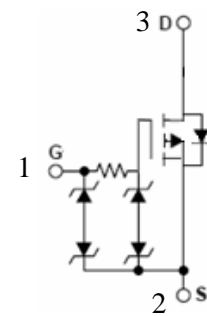
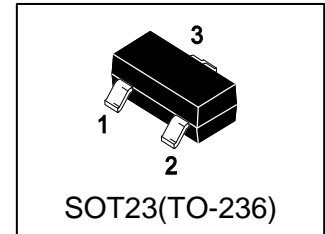
4. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter	Symbol	Limits	Unit
Drain-Source Voltage	V_{DSS}	-20	V
Gate-to-Source Voltage – Continuous	V_{GS}	± 8	V
Drain Current			A
– Continuous $T_a = 25^\circ C$	I_D	-4	
– Pulsed (Note 1)	I_{DM}	-30	

5. THERMAL CHARACTERISTICS

Parameter	Symbol	Limits	Unit
Power Dissipation	PD	1	W
Thermal Resistance, Junction-to-Ambient(Note 2)	$R_{\theta JA}$	150	$^\circ C/W$
Junction-to-Ambient(Note 3)	$R_{\theta JA}$	194	$^\circ C/W$
Junction and Storage temperature	T_J, T_{stg}	$-55 \sim +150$	$^\circ C$

- 1.Repetitive Rating: Pulse width limited by the maximum junction temperature.
- 2.1-in² 2oz Cu PCB board.
- 3.Surface mounted on FR4 board using the minimum recommended pad size.

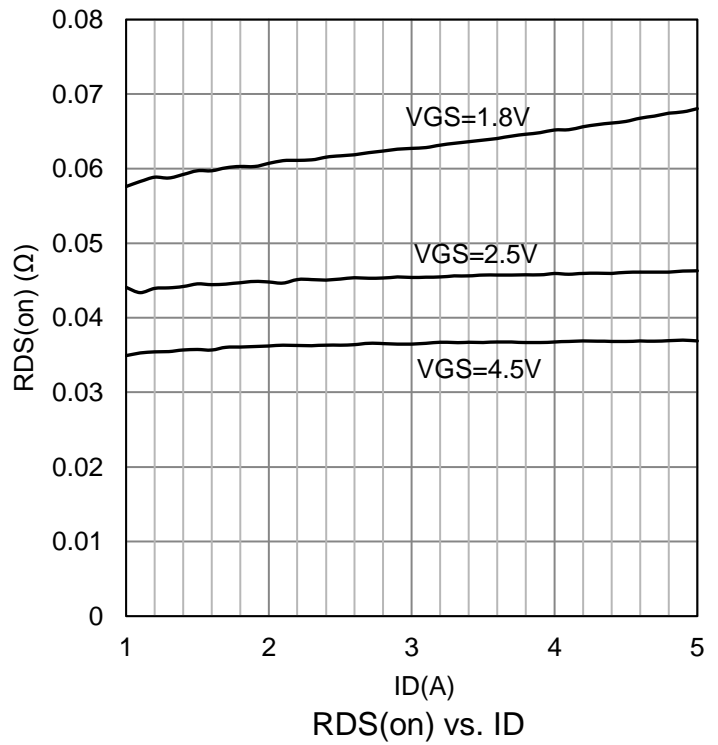
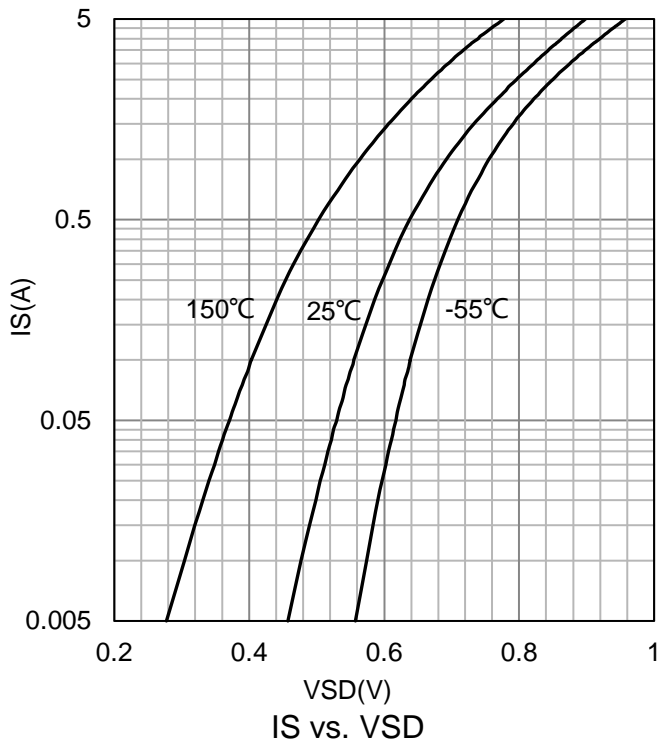
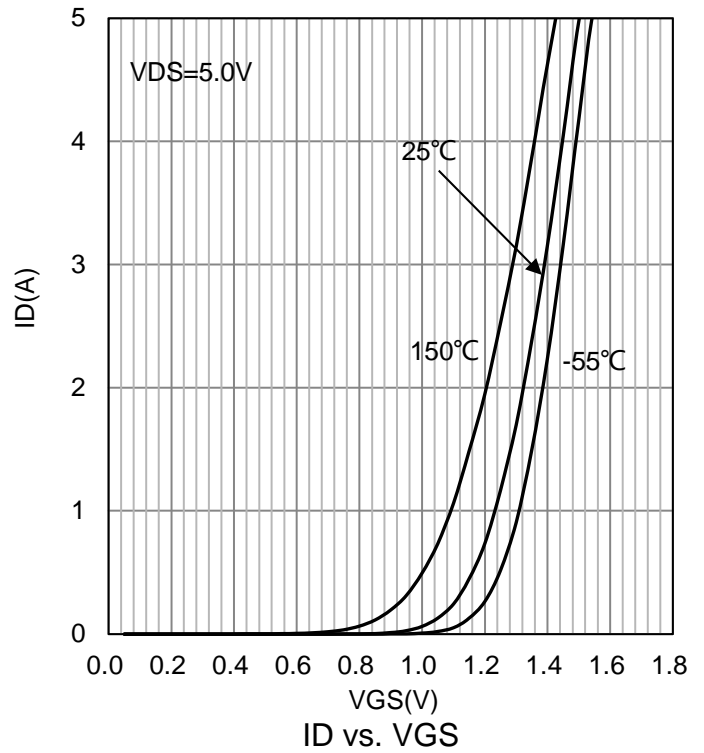
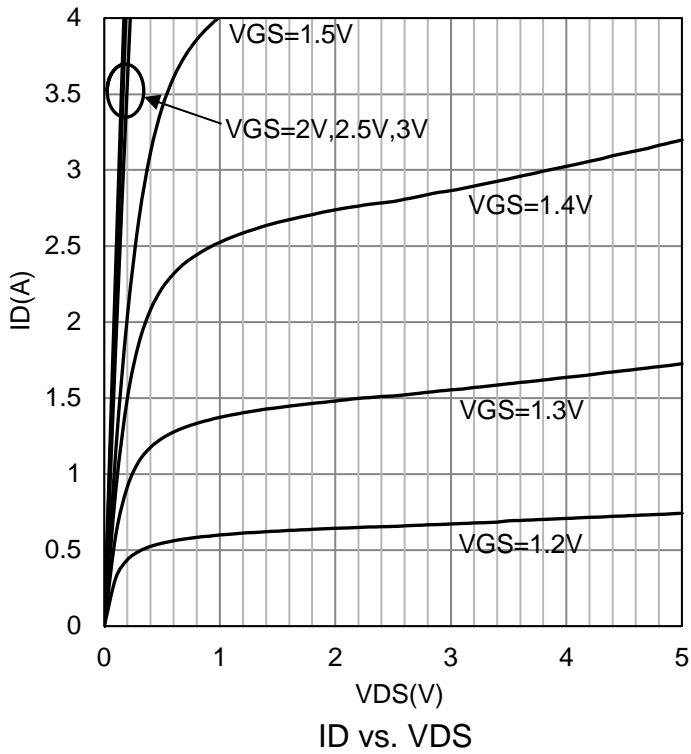


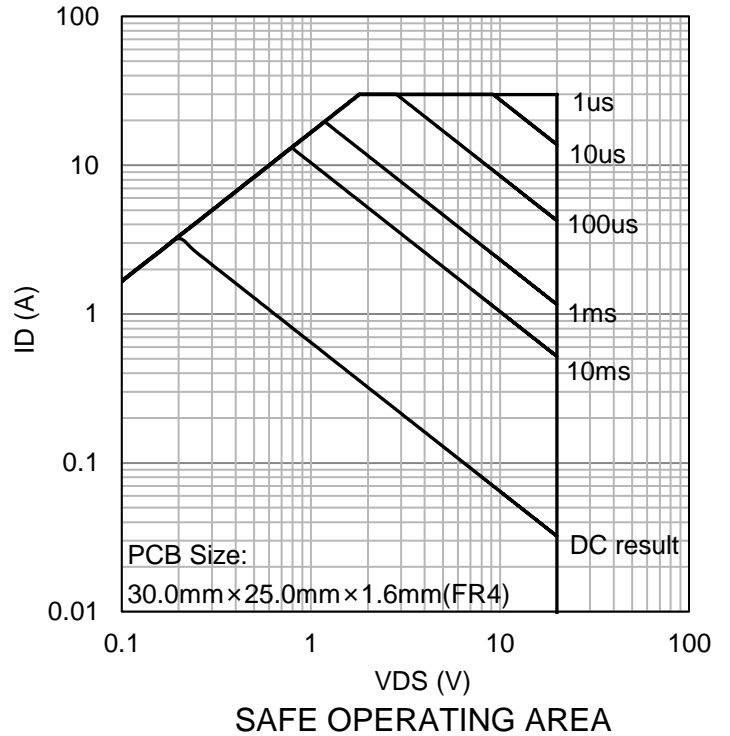
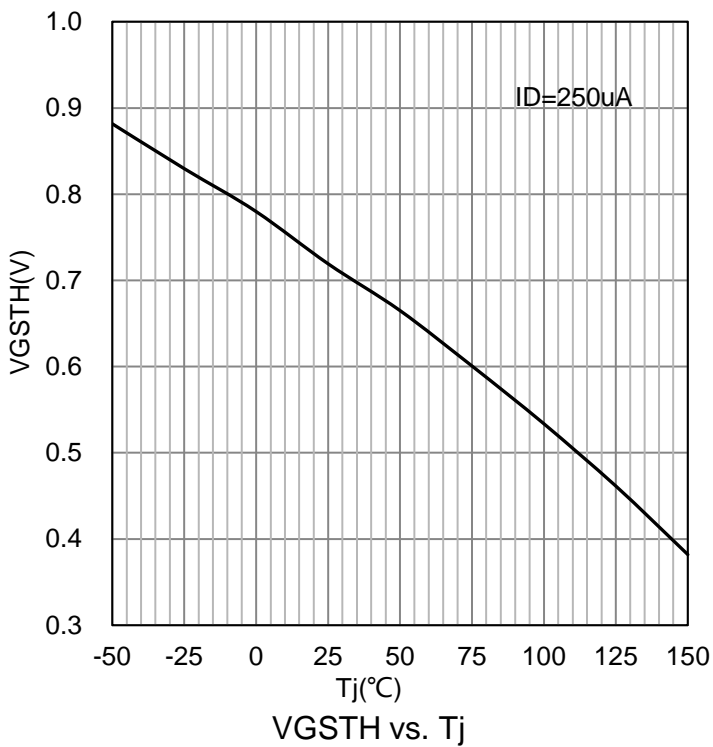
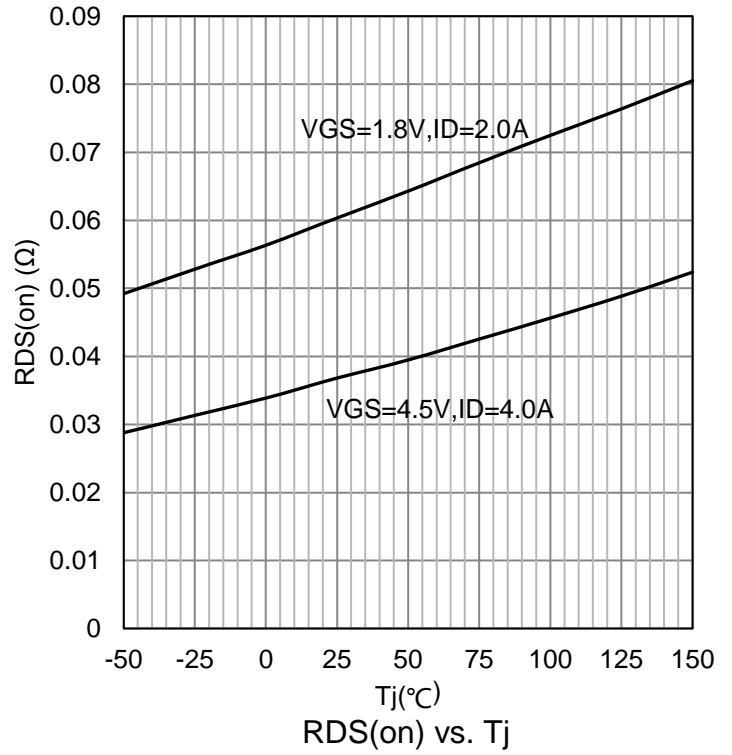
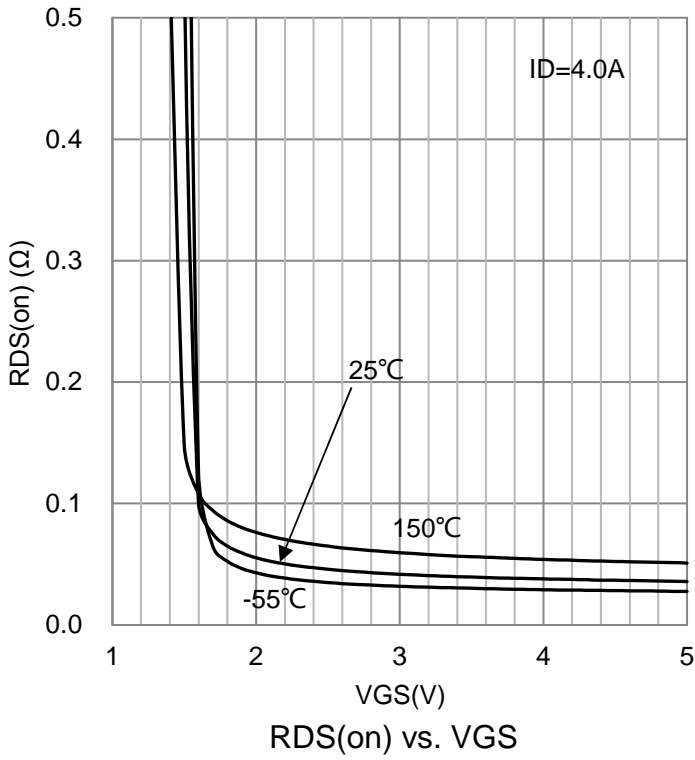
6. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
Static						
Drain–Source Breakdown Voltage (VGS = 0 V, ID = -250 μA)	VBRDSS	-20	-	-	V	
Zero Gate Voltage Drain Current (VGS = 0 V, VDS = -16 V)	IDSS	-	-	-1	μA	
Gate–Body Leakage Current, Forward (VGS = 8 V)	IGSSF	-	-	10	μA	
Gate–Body Leakage Current, Reverse (VGS = - 8 V)	IGSSR	-	-	-10	μA	
Gate Threshold Voltage (VDS = VGS, ID = -250 μA)	VGS(th)	-0.3	-	-1.0	V	
Static Drain–Source On–State Resistance(Note 4) (VGS = -4.5 V, ID = -4 A) (VGS = -2.5 V, ID = -4 A) (VGS = -1.8 V, ID = -2.0 A)	RDS(on)	-	-	60 75 85	mΩ	
Dynamic						
Total Gate Charge (VDS= -10 V, ID = -4 A, VGS = -4.5 V)	Qg	-	10.9	-	nC	
Gate–Source Charge (VDS= -10 V, ID = -4 A, VGS = -4.5 V)	Qgs	-	1.62	-	nC	
Gate–Drain Charge (VDS= -10 V, ID = -4 A, VGS = -4.5 V)	Qgd	-	3.4	-	nC	
Input Capacitance (VDS = -10 V, f= 1.0MHz, VGS = 0 V)	Ciss	-	1091	-	pF	
Output Capacitance (VDS = -10 V, f= 1.0MHz, VGS = 0 V)	Coss	-	93	-	pF	
Reverse Transfer Capacitance (VDS = -10 V, f= 1.0MHz, VGS = 0 V)	Crss	-	88	-	pF	
Turn-On Delay Time	(VDD = -10 V, RL= 10Ω ID = -1 A, VGEN = -4.5 V, RG = 3.1Ω)	td(on)	-	48	-	ns
Rise Time		tr	-	98	-	
Turn-Off Delay Time		td(off)	-	642	-	
Fall Time		tf	-	282	-	
Forward Voltage (VGS = 0 V, ISD = -1.0 A)	VSD	-	-	-1	V	
Max.Forward Current	IS	-	-	-2.2	A	

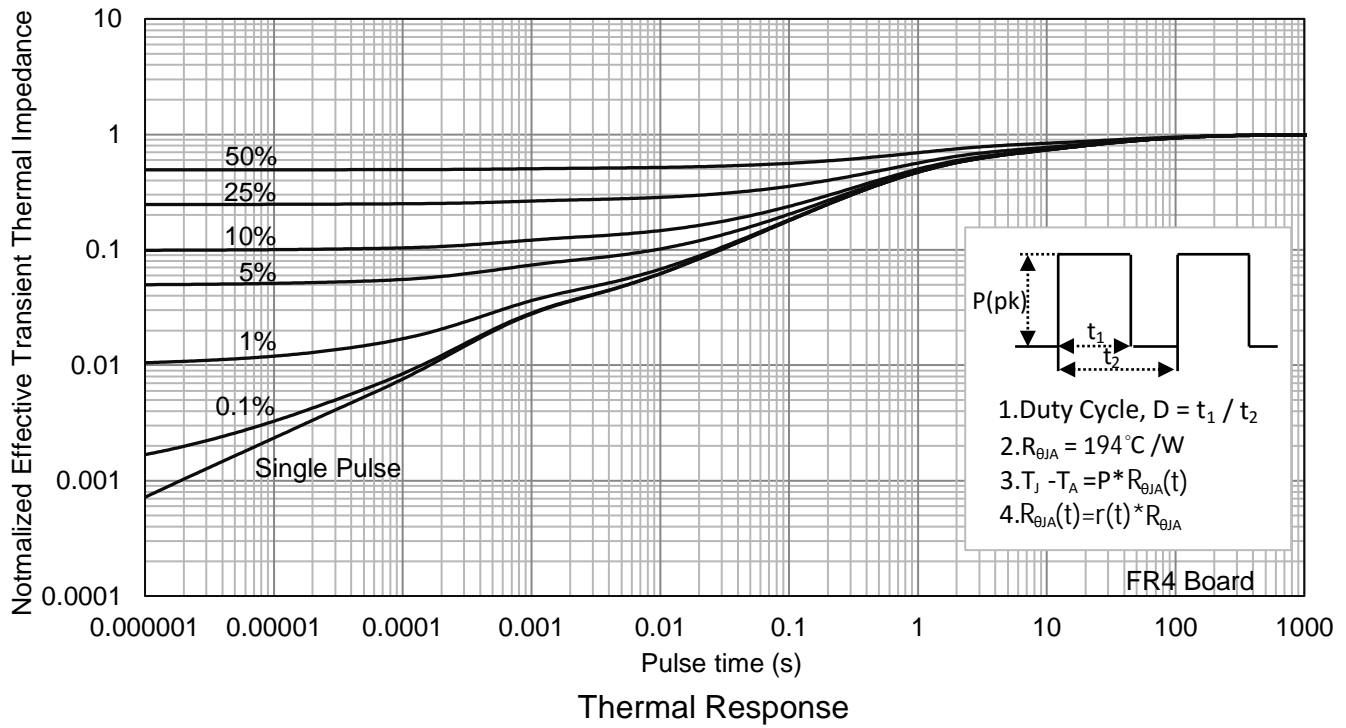
4.Pulse Test: Pulse Width ≤300 μs, Duty Cycle ≤2.0%.

7. ELECTRICAL CHARACTERISTICS CURVES



7.ELECTRICAL CHARACTERISTICS CURVES (Con.)


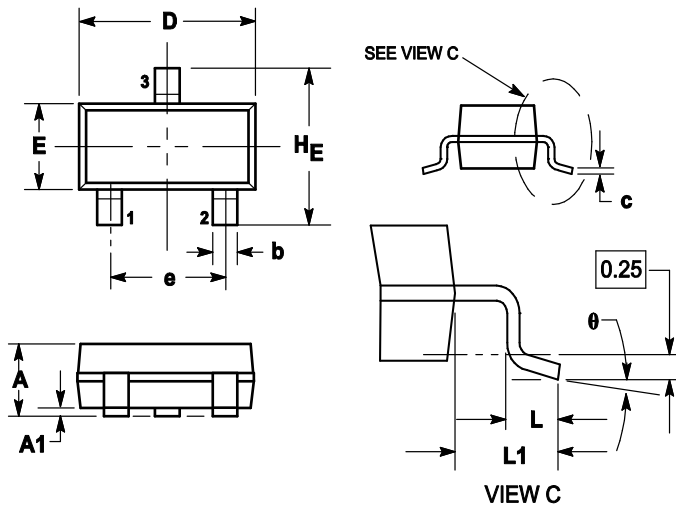
7.ELECTRICAL CHARACTERISTICS CURVES (Con.)



8. OUTLINE AND DIMENSIONS

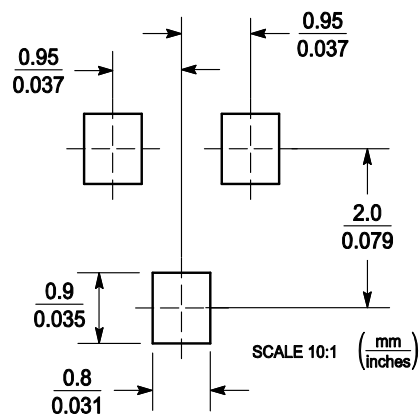
Notes:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. MAXIMUM LEAD THICKNESS INCLUDES LEAD FINISH. MINIMUM LEAD THICKNESS IS THE MINIMUM THICKNESS OF BASE MATERIAL.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.



DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.89	1	1.11	0.035	0.04	0.044
A1	0.01	0.06	0.1	0.001	0.002	0.004
b	0.37	0.44	0.5	0.015	0.018	0.02
c	0.09	0.13	0.18	0.003	0.005	0.007
D	2.80	2.9	3.04	0.11	0.114	0.12
E	1.20	1.3	1.4	0.047	0.051	0.055
e	1.78	1.9	2.04	0.07	0.075	0.081
L	0.10	0.2	0.3	0.004	0.008	0.012
L1	0.35	0.54	0.69	0.014	0.021	0.029
HE	2.10	2.4	2.64	0.083	0.094	0.104
θ	0°	---	10°	0°	---	10°

9. SOLDERING FOOTPRINT



DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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