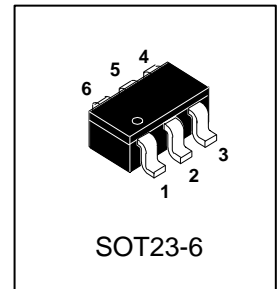


LP3475T1G

30V P-Channel Enhancement-Mode MOSFET

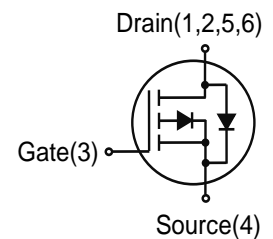
1. FEATURES

- $V_{DS} = -30V$
- $R_{DS(ON)} \leq 65m\Omega @ V_{GS} = -10V$
- $R_{DS(ON)} \leq 90m\Omega @ V_{GS} = -4.5V$
- We declare that the material of product compliance with RoHS requirements and Halogen Free.



2. DEVICE MARKING AND ORDERING INFORMATION

Device	Marking	Shipping
LP3475T1G	A75	3000/Tape&Reel



3. MAXIMUM RATINGS($T_a = 25^\circ C$)

Parameter		Symbol	Limits	Unit
Drain-Source Voltage		V_{DS}	-30	V
Gate-to-Source Voltage		V_{GS}	± 20	V
Continuous Drain Current(Note 1)	$T_a = 25^\circ C$	ID	-4.5	A
	$T_a = 70^\circ C$		-3.5	
Pulsed Drain Current(Note 2)		IDM	-18	
Continuous Drain Current(Note 3)		ID	-2.7	
Pulsed Drain Current(Note 3)		IDM	-11	
Avalanche Current		IAS	11	
Avalanche energy(L=0.1mH)		EAS	6.05	mJ
Power Dissipation(Note 1)	$T_a = 25^\circ C$	PD	1.4	W
	$T_a = 70^\circ C$		0.9	
Power Dissipation(Note 3)		PD	0.8	
Junction and Storage Temperature Range		T_j, T_{stg}	-55~+150	$^\circ C$

4. THERMAL CHARACTERISTICS

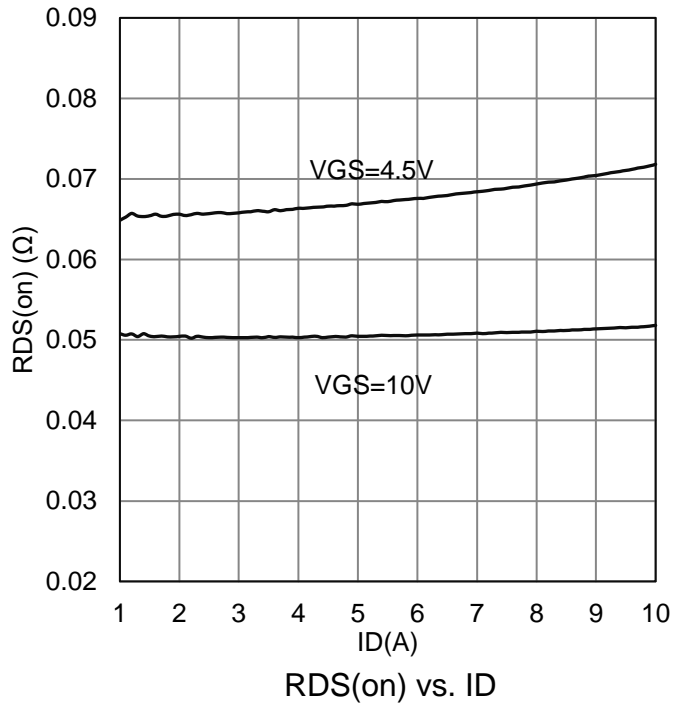
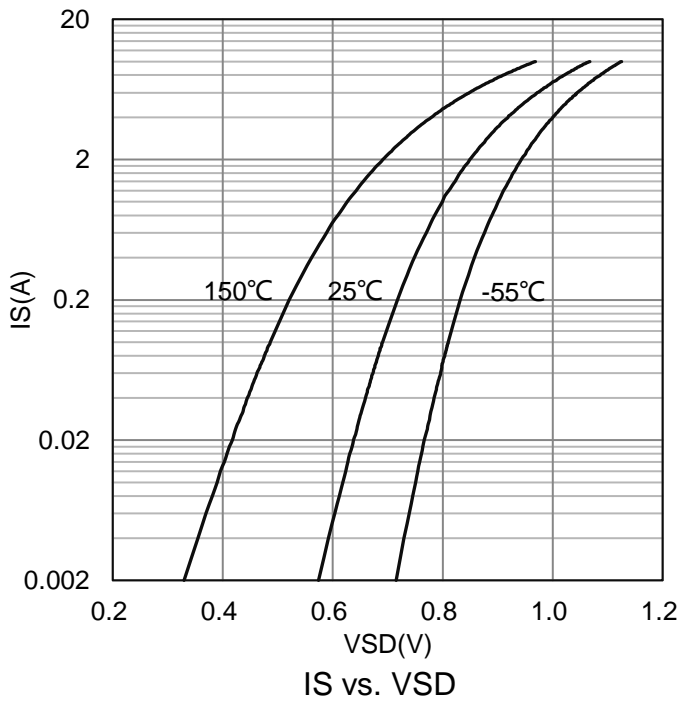
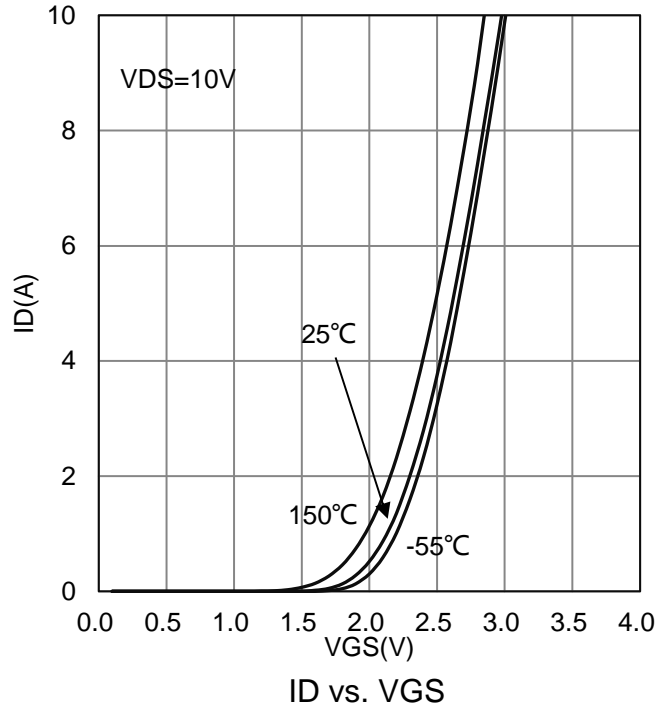
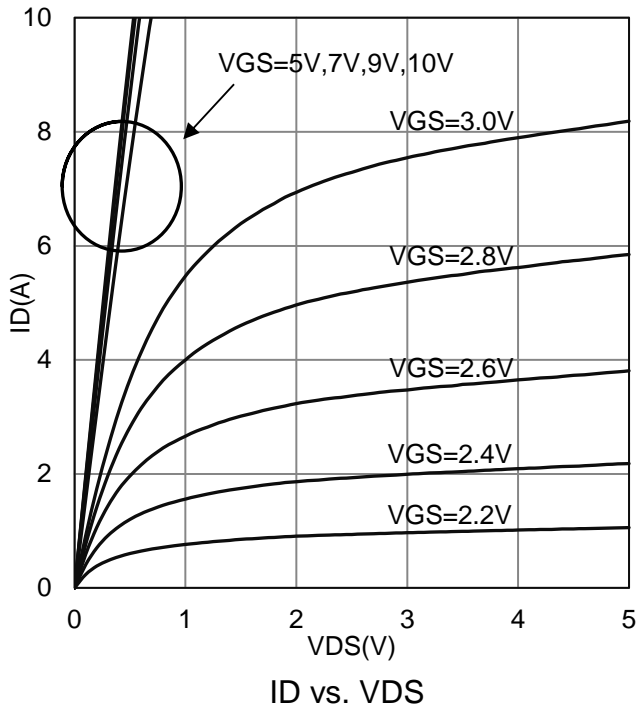
Parameter	Symbol	Limits	Unit
Thermal Resistance, Junction-to-Ambient (Note 1)	$R_{\theta JA}$	89	$^\circ C/W$
Thermal Resistance, Junction-to-Ambient (Note 3)	$R_{\theta JA}$	160	$^\circ C/W$
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	30	$^\circ C/W$

1. Surface mounted on "1.5 x 1.5" FR4 board using 1 sq in pad, 2 oz Cu
2. Pulse width limited by maximum junction temperature.
3. Surface mounted on FR4 board using the minimum recommended pad size.

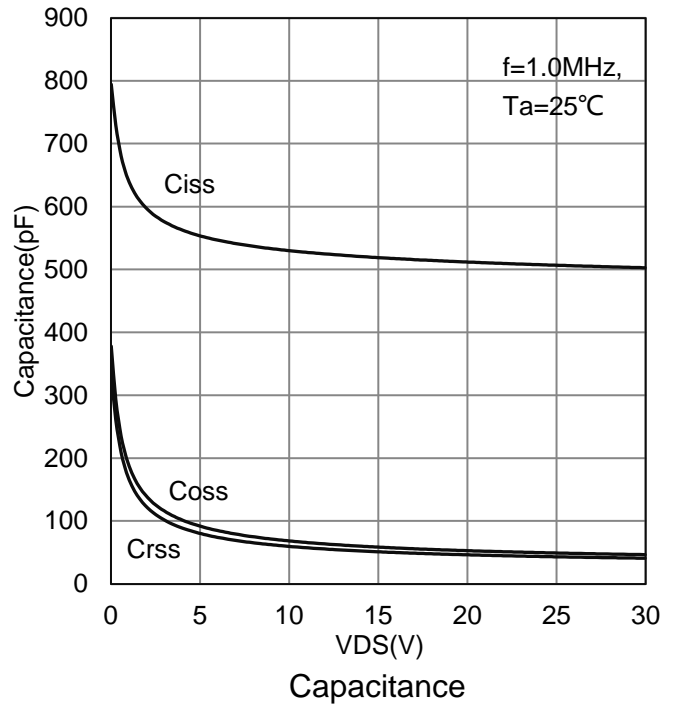
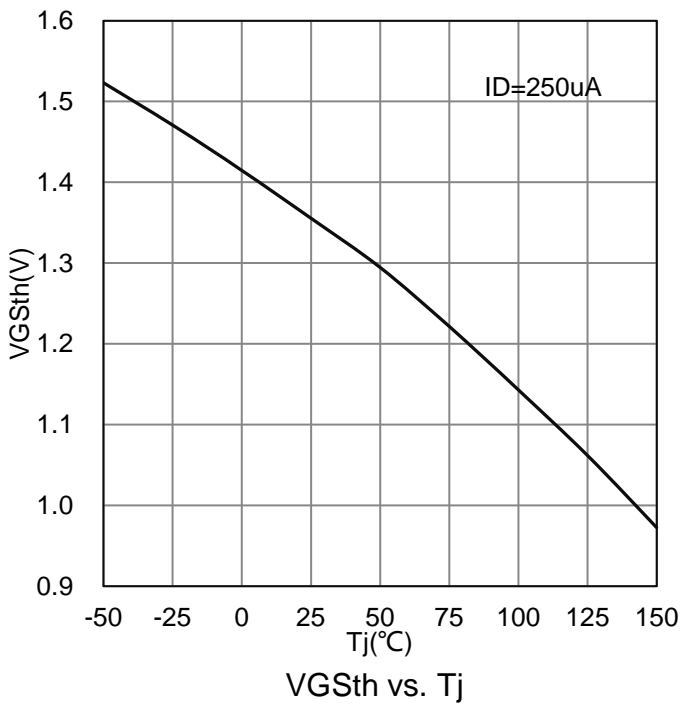
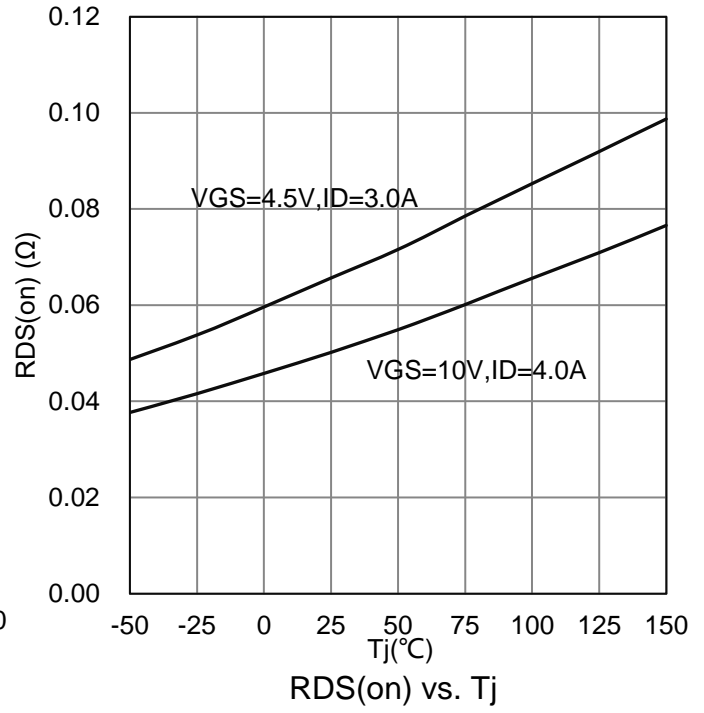
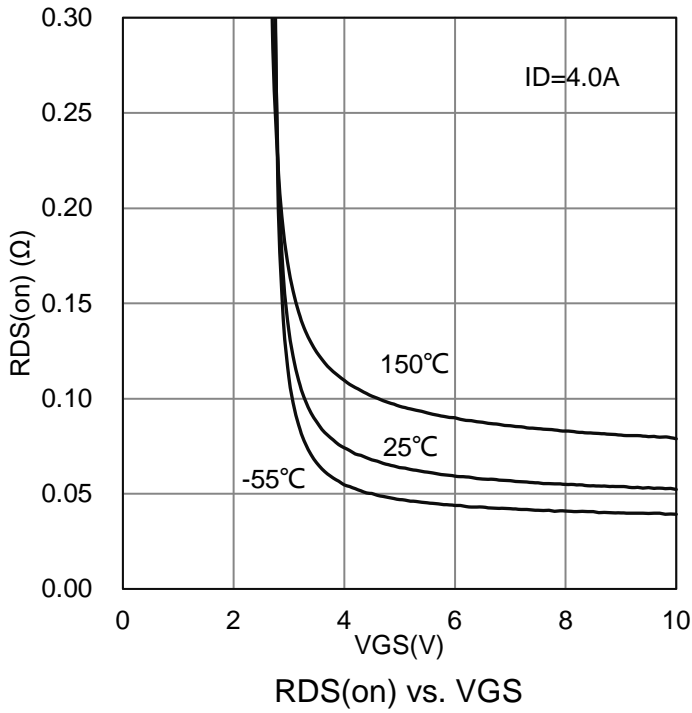
5. ELECTRICAL CHARACTERISTICS (Ta= 25°C)

Characteristic	Symbol	Min.	Typ.	Max.	Unit	
Static						
Drain–Source Breakdown Voltage (VGS = 0, ID = -250μA)	VBRDSS	-30	-	-	V	
Zero Gate Voltage Drain Current (VGS = 0, VDS = -24 V)	IDSS	-	-	-1	μA	
Gate Leakage Current (VDS =0V, VGS =±20V)	IGSS	-	-	±100	nA	
Gate Threshold Voltage (VDS = VGS, ID = -250μA)	VGS(th)	-1	-1.4	-1.6	V	
Static Drain–Source On–State Resistance (VGS =-10V, ID =-4A) (VGS =-4.5V, ID =-3A)	RDS(on)	- -	- -	65 90	mΩ	
Dynamic						
Input Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -15 V)	Ciss	-	534	-	pF	
Output Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -15 V)	Coss	-	60	-		
Reverse Transfer Capacitance (VGS = 0 V, f = 1.0MHz, VDS= -15 V)	Crss	-	52	-		
Gate resistance (VGS =0V, VDS =0V, f=1MHz)	Rg	-	12	-	Ω	
Total Gate Charge	(VDS =-15V, ID =-4A)	Qg(10V)	-	11.4	-	nC
Total Gate Charge		Qg(4.5V)	-	5.6	-	
Gate-Source Charge		Qgs	-	1.3	-	
Gate-Drain Charge		Qgd	-	2.3	-	
Turn-On Delay Time	(VDS = -15V, RL= 3.6 Ω, VGS = -10V, RG = 3Ω)	td(on)	-	3.6	-	ns
Rise Time		tr	-	9.8	-	
Turn-Off Delay Time		td(off)	-	19.2	-	
Fall Time		tf	-	6.7	-	
Forward Voltage (VGS = 0 V, IS = -1A)	VSD	-	-	-1.5	V	

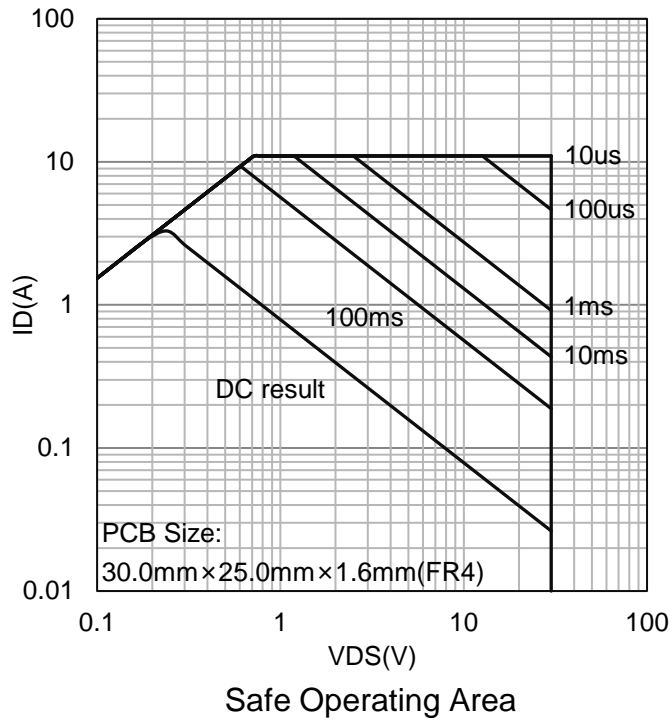
6. ELECTRICAL CHARACTERISTICS CURVES



6. ELECTRICAL CHARACTERISTICS CURVES(Con.)

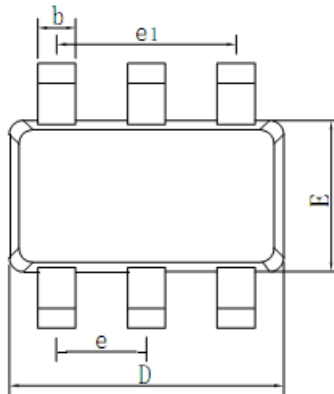
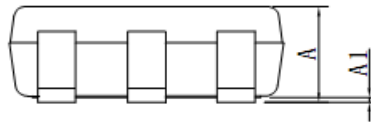
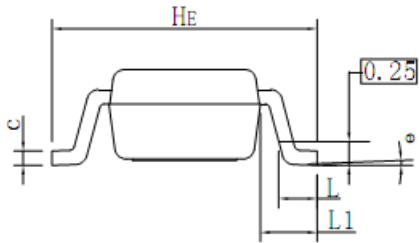


6. ELECTRICAL CHARACTERISTICS CURVES(Con.)



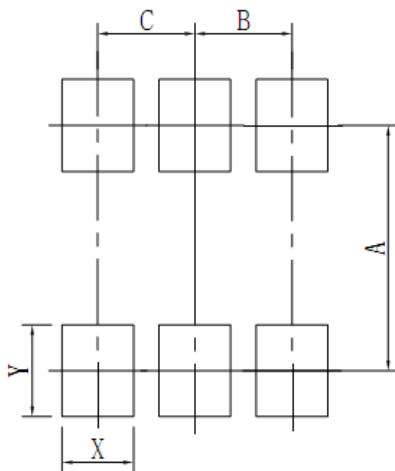
7.OUTLINE AND DIMENSIONS

SOT23-6



SOT23-6			
DIM	MIN	NOR	MAX
A	0.90	1.00	1.10
A1	0.01	0.06	0.10
b	0.25	0.40	0.50
c	0.10	0.17	0.26
D	2.80	2.90	3.10
E	1.30	1.60	1.70
e	0.85	0.95	1.05
e1	1.80	1.90	2.00
L	0.20	0.40	0.60
L1	0.60REF		
HE	2.50	2.80	3.00
θ	0°	-	10°

8.SOLDERING FOOTPRINT



SOT23-6	
DIM	(mm)
X	0.70
Y	0.90
A	2.40
B	0.95
C	0.95

DISCLAIMER

- Curve guarantee in the specification. The curve of test items with electric parameter is used as quality guarantee. The curve of test items without electric parameter is used as reference only.
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