

N-Channel Power MOSFET

Description

The IRFM120ATF uses advanced trench technology and design to provide excellent $R_{DS(ON)}$ with low gate charge. It can be used in a wide variety of applications. It is ESD protected.

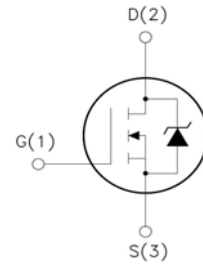
General Features

- | V_{DS} | $R_{DS(ON)}$
@ 10V (typ) | I_D |
|----------|-----------------------------|-------|
| 100V | 125 mΩ | 5A |

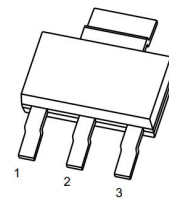
- High density cell design for ultra low $R_{DS(on)}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

Application

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Motor control



Schematic diagram



SOT-223

Absolute Maximum Ratings ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	100	V
Gate-Source Voltage	V_{GS}	± 20	V
Drain Current-Continuous	I_D	5	A
Drain Current-Pulsed (Note 1)	I_{DM}	21	A
Maximum Power Dissipation	P_D	5	W
Operating Junction and Storage Temperature Range	T_J, T_{STG}	-55 To 150	$^\circ\text{C}$

Thermal Characteristic

Thermal Resistance, Junction-to-Ambient (Note 2)	$R_{\theta JA}$	41.7	$^\circ\text{C/W}$
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Electrical Characteristics ($T_A=25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Off Characteristics						
Drain-Source Breakdown Voltage	BV_{DS}	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS}=80V, V_{GS}=0V$	-	-	800	nA

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Gate-Body Leakage Current	I _{GSS}	V _{GS} =±20V, V _{DS} =0V	-	-	±100	nA
On Characteristics (Note 3)						
Gate Threshold Voltage	V _{GS(th)}	V _{DS} =V _{GS} , I _D =250μA	1	1.8	3	V
Drain-Source On-State Resistance	R _{DS(ON)}	V _{GS} =10V, I _D =3A		125	145	mΩ
Forward Transconductance	g _{FS}	V _{DS} =5V, I _D =2.9A	-	8	-	S
Dynamic Characteristics (Note4)						
Input Capacitance	C _{Iss}	V _{DS} =25V, V _{GS} =0V, F=1.0MHz	-	210	-	PF
Output Capacitance	C _{Oss}		-	30	-	PF
Reverse Transfer Capacitance	C _{rss}		-	14	-	PF
Switching Characteristics (Note 4)						
Turn-on Delay Time	t _{d(on)}	V _{DD} =50V, I _D =5A, R _L =15Ω V _{GS} =10V, R _G =2.5Ω	-	15	-	nS
Turn-on Rise Time	t _r		-	3.4	-	nS
Turn-Off Delay Time	t _{d(off)}		-	21	-	nS
Turn-Off Fall Time	t _f		-	3.1	-	nS
Total Gate Charge	Q _g	V _{DS} =50V, I _D =5A, V _{GS} =10V		4.5		nC
Gate-Source Charge	Q _{gs}		-	1.5	-	nC
Gate-Drain Charge	Q _{gd}		-	1.2	-	nC
Drain-Source Diode Characteristics						
Diode Forward Voltage (Note 3)	V _{SD}	V _{GS} =0V, I _S =6A	-	-	1.2	V
Diode Forward Current (Note 2)	I _S		-	-	5	A

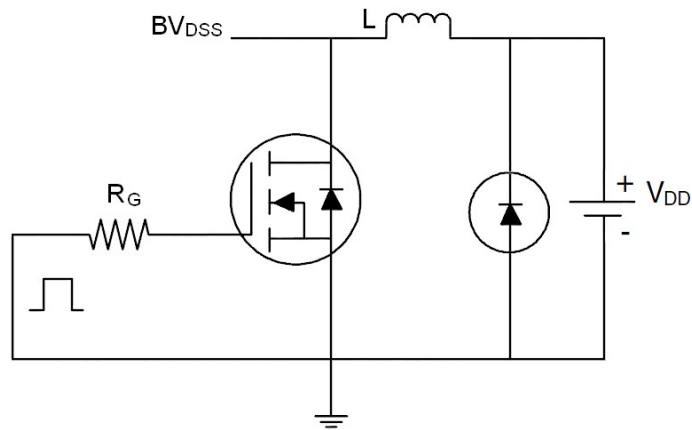
Notes:

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board, $t \leq 10$ sec.
3. Pulse Test: Pulse Width $\leq 300\mu s$, Duty Cycle $\leq 2\%$.
4. Guaranteed by design, not subject to production

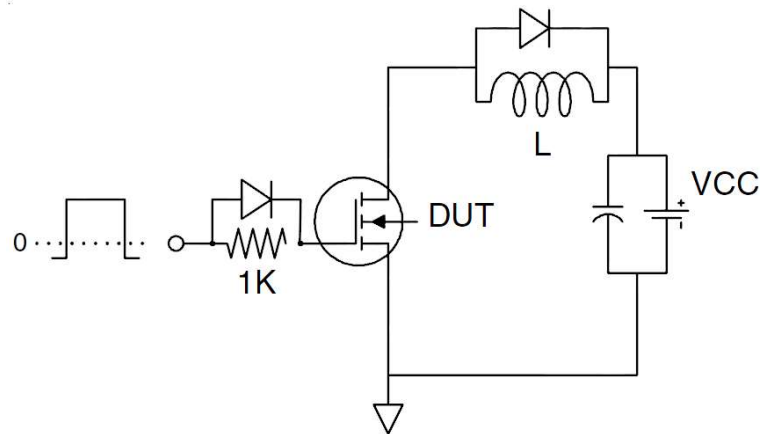
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Test Circuit

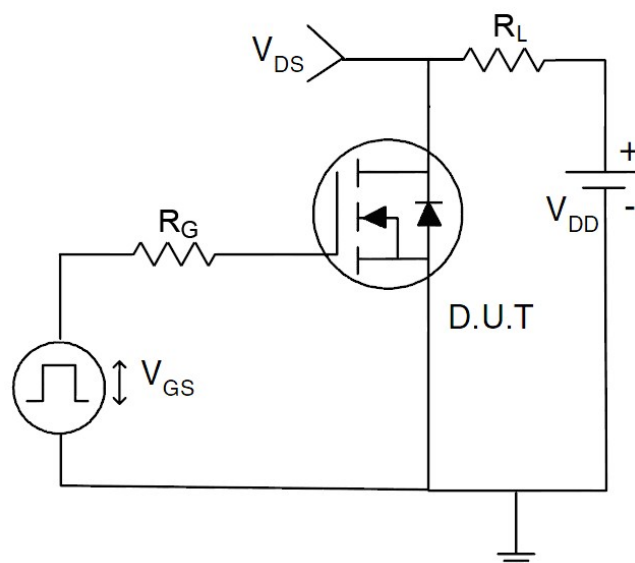
1) E_{AS} test circuit



2) Gate charge test circuit



3) Switch Time Test Circuit



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Typical Electrical and Thermal Characteristics (curves)

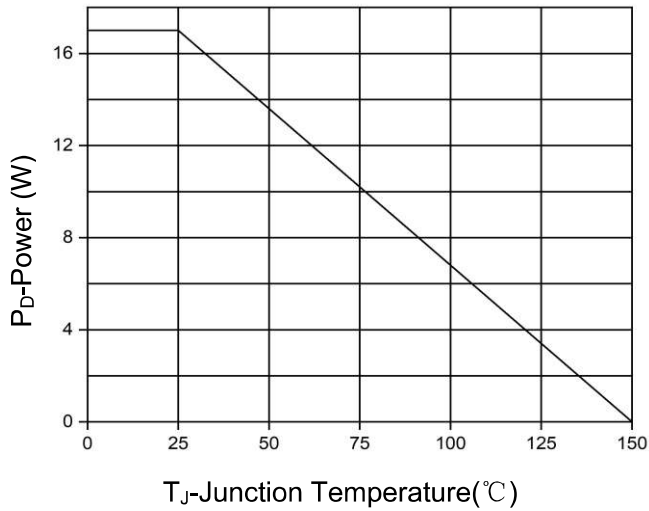


Figure 1. Power Dissipation

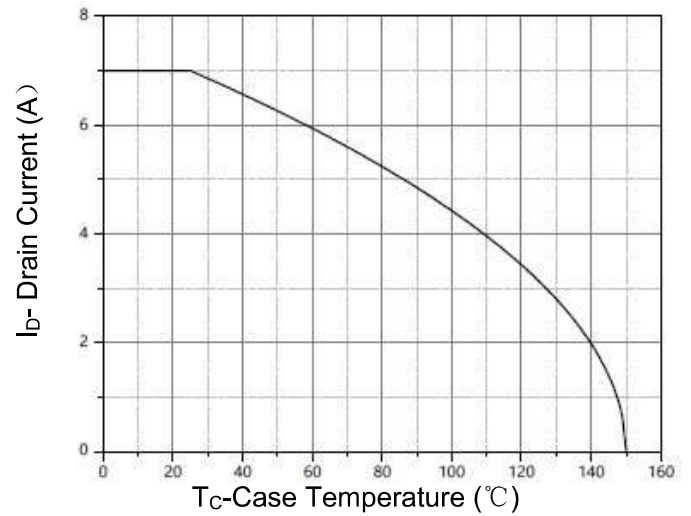


Figure 2. Drain Current

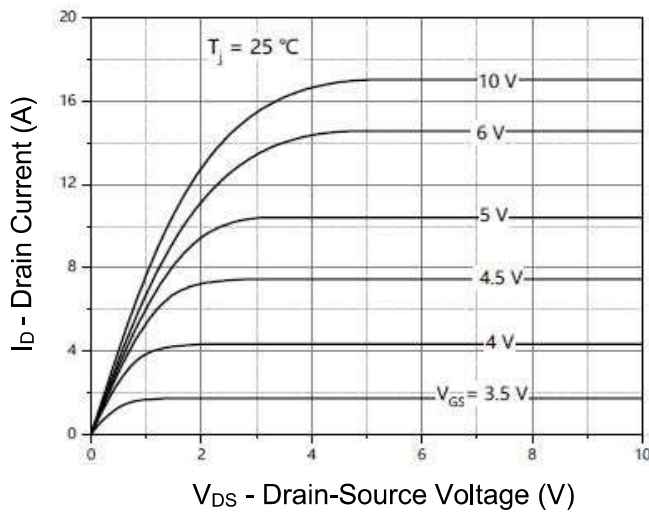


Figure 3. Output characteristics

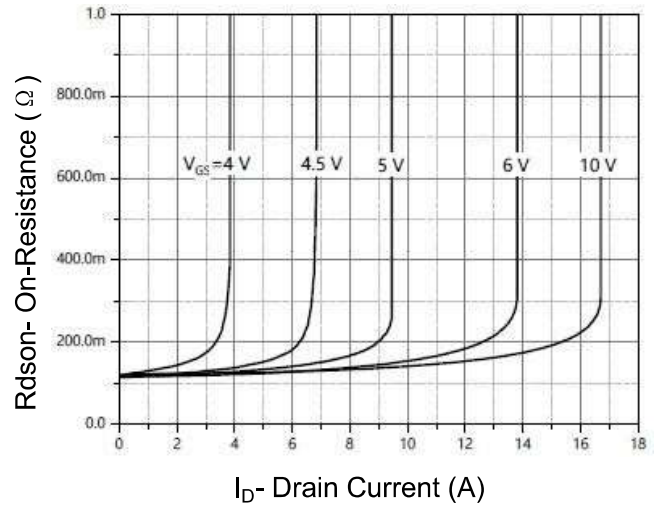


Figure 4. Drain-Source On-state resistance

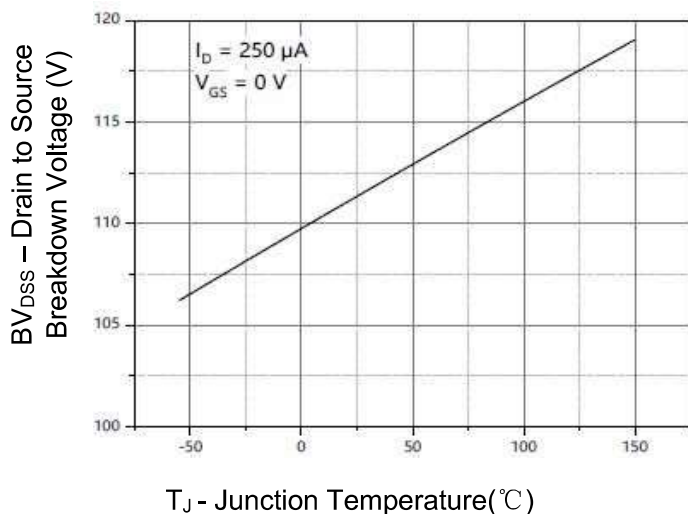


Figure 5. Drain-source breakdown voltage

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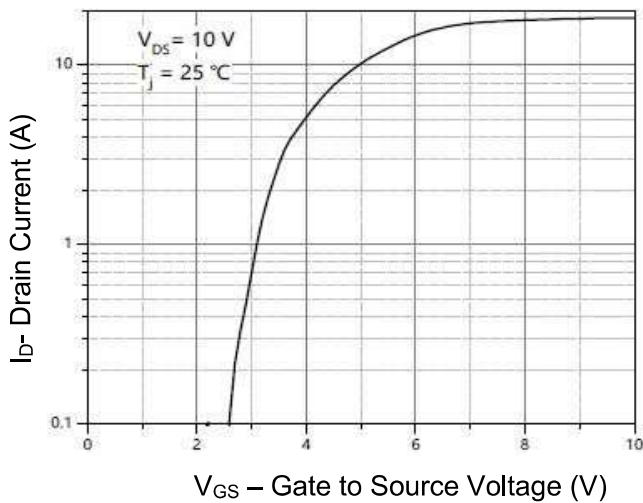


Figure 6. Transfer Characteristics

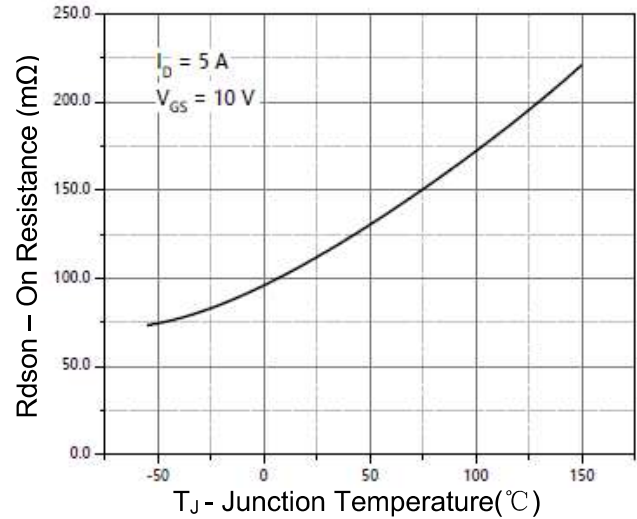


Figure 7. Drain-Source On-State Resistance

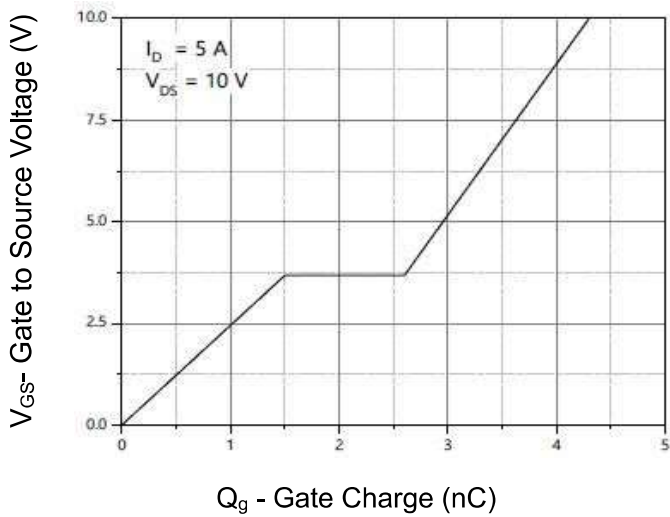


Figure 8. Gate Charge

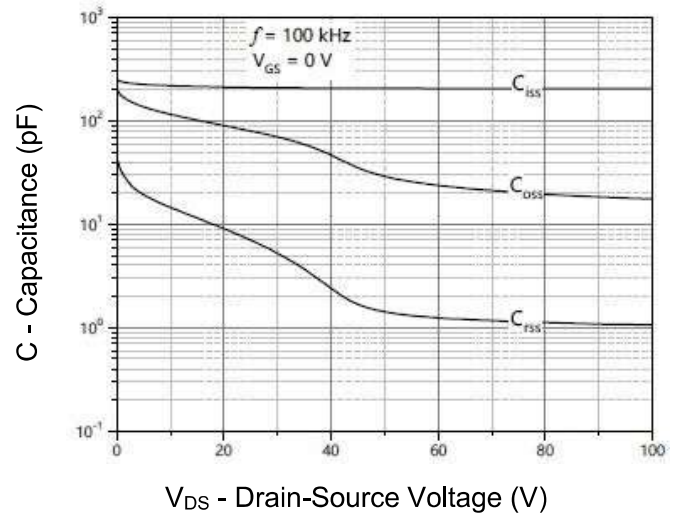


Figure 9 . Capacitance vs Vds

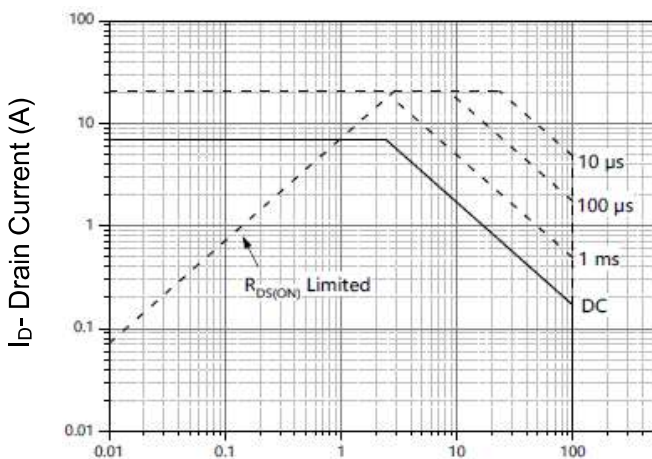


Figure 10. Safe Operation Area

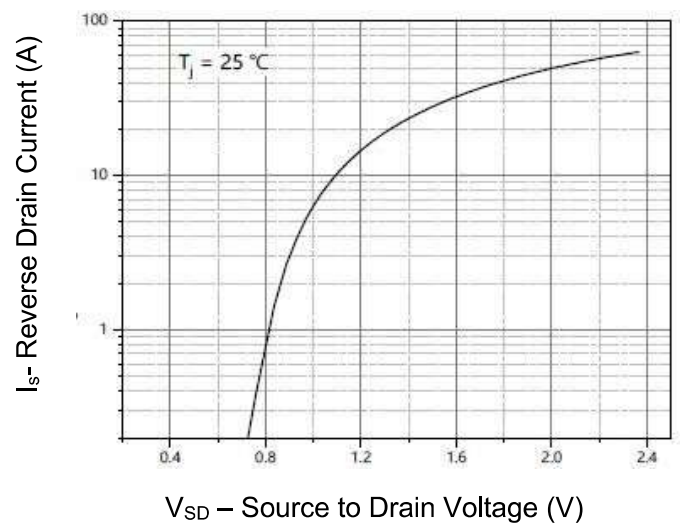


Figure 11. Source- Drain Diode Forward