

**N-Channel Power MOSFET**
**Description**

The IRLL110TRPBF uses advanced trench technology and design to provide excellent  $R_{DS(ON)}$  with low gate charge. It can be used in a wide variety of applications.

It is ESD protected.

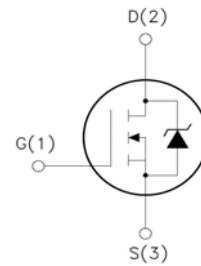
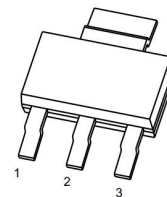
**General Features**

$V_{DSS}$	$R_{DS(ON)}$ @ 10V (typ)	$I_D$
100V	125 m $\Omega$	5A

- High density cell design for ultra low  $R_{dson}$
- Fully characterized avalanche voltage and current
- Excellent package for good heat dissipation

**Application**

- Power switching application
- Hard switched and high frequency circuits
- Uninterruptible power supply
- Motor control


**Schematic diagram**

**SOT-223**
**Absolute Maximum Ratings ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	5	A
Drain Current-Pulsed <sup>(Note 1)</sup>	$I_{DM}$	21	A
Maximum Power Dissipation	$P_D$	5	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

**Thermal Characteristic**

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	41.7	$^\circ\text{C/W}$
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**Electrical Characteristics ( $T_A=25^\circ\text{C}$  unless otherwise noted)**

Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu\text{A}$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=80V, V_{GS}=0V$	-	-	800	nA

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Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	1.8	3	V
Drain-Source On-State Resistance	$R_{DS(ON)}$	$V_{GS}=10V, I_D=3A$		125	145	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=2.9A$	-	8	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=25V, V_{GS}=0V,$ $F=1.0MHz$	-	210	-	PF
Output Capacitance	$C_{oss}$		-	30	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	14	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=5A, R_L=15\Omega$ $V_{GS}=10V, R_G=2.5\Omega$	-	15	-	nS
Turn-on Rise Time	$t_r$		-	3.4	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	21	-	nS
Turn-Off Fall Time	$t_f$		-	3.1	-	nS
Total Gate Charge	$Q_g$	$V_{DS}=50V, I_D=5A,$ $V_{GS}=10V$		4.5		nC
Gate-Source Charge	$Q_{gs}$		-	1.5	-	nC
Gate-Drain Charge	$Q_{gd}$		-	1.2	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=6A$	-	-	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	5	A

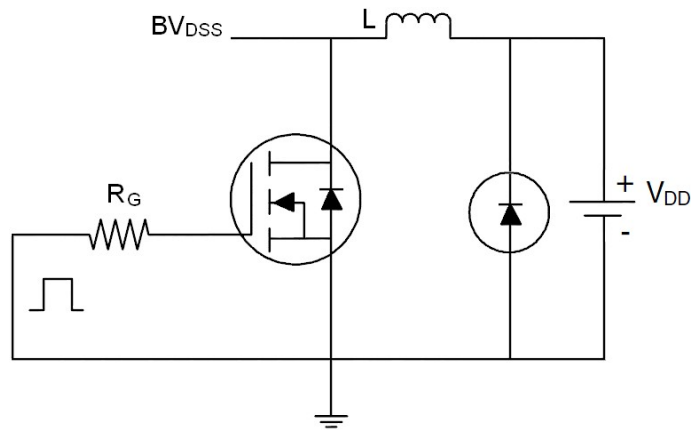
**Notes:**

1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

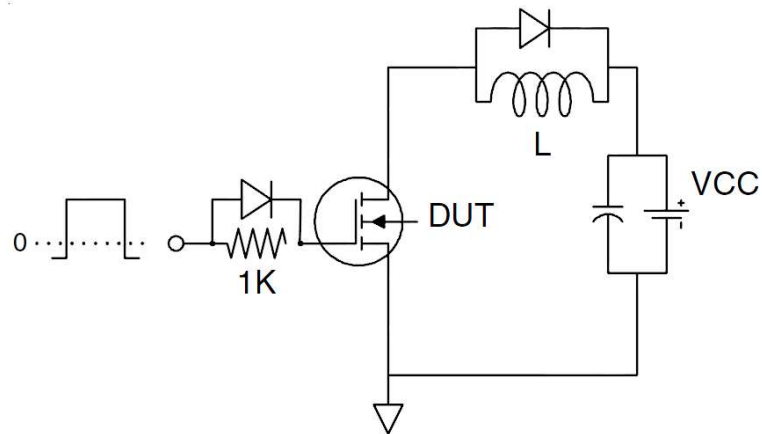
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**Test Circuit**

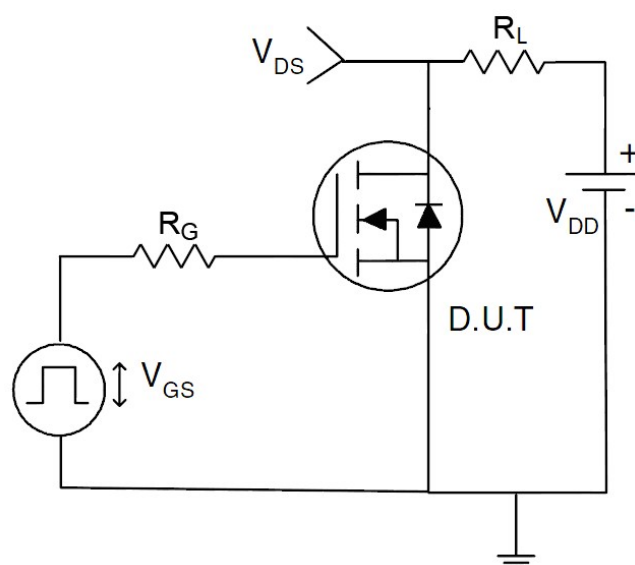
1)  $E_{AS}$  test circuit



2) Gate charge test circuit

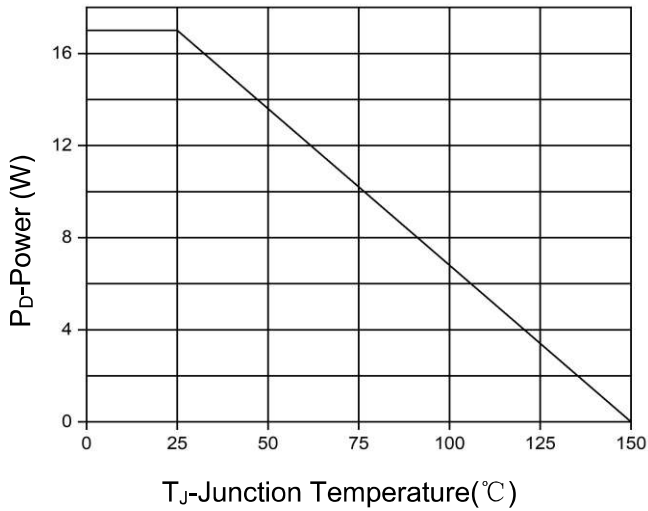


3) Switch Time Test Circuit

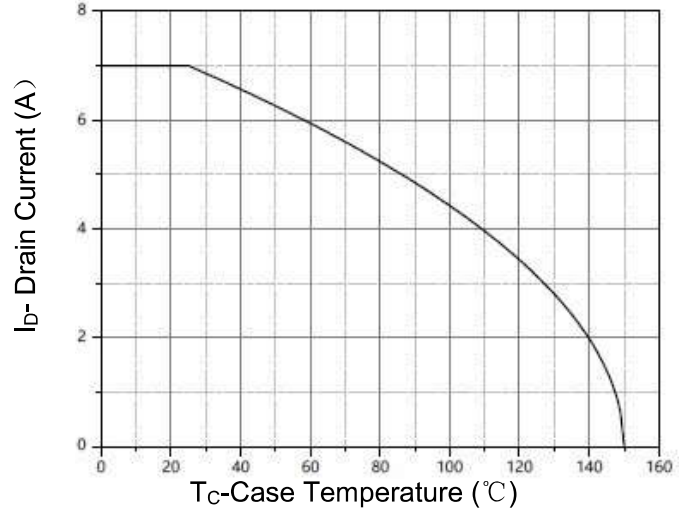


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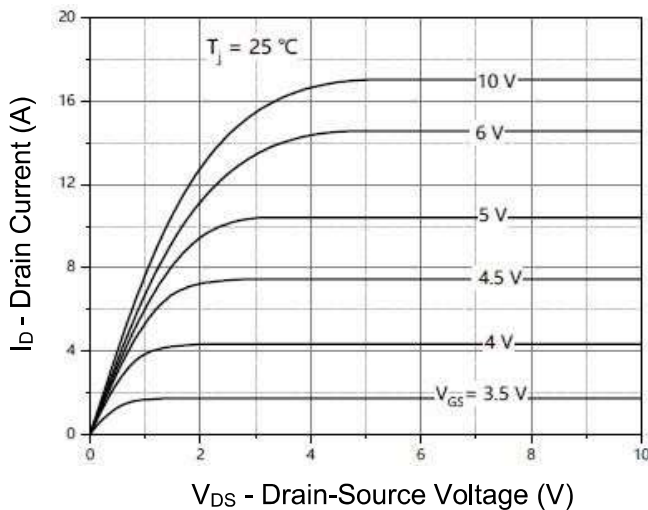
**Typical Electrical and Thermal Characteristics (curves)**



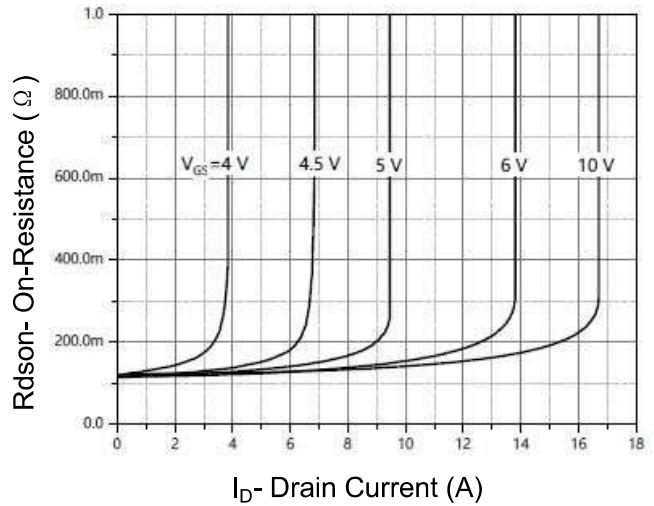
**Figure 1. Power Dissipation**



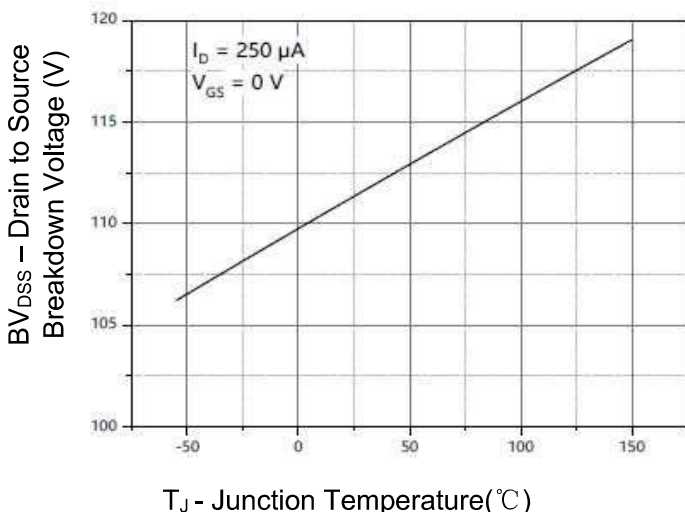
**Figure 2. Drain Current**



**Figure 3. Output characteristics**

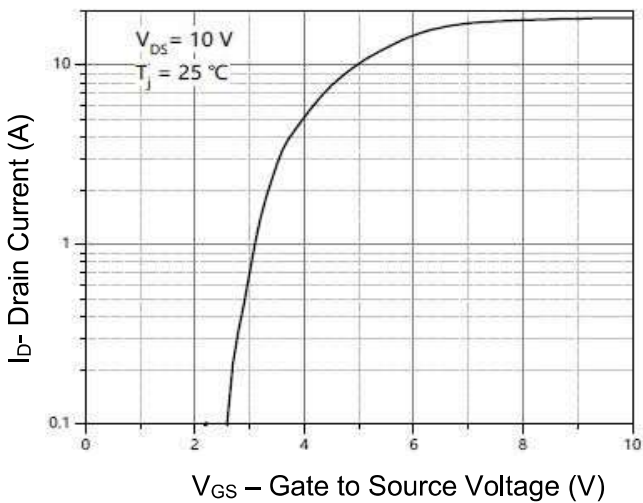


**Figure 4. Drain-Source On-state resistance**

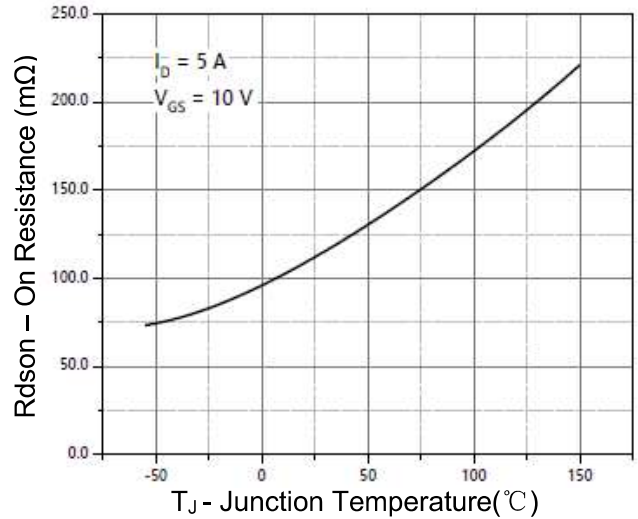


**Figure 5. Drain-source breakdown voltage**

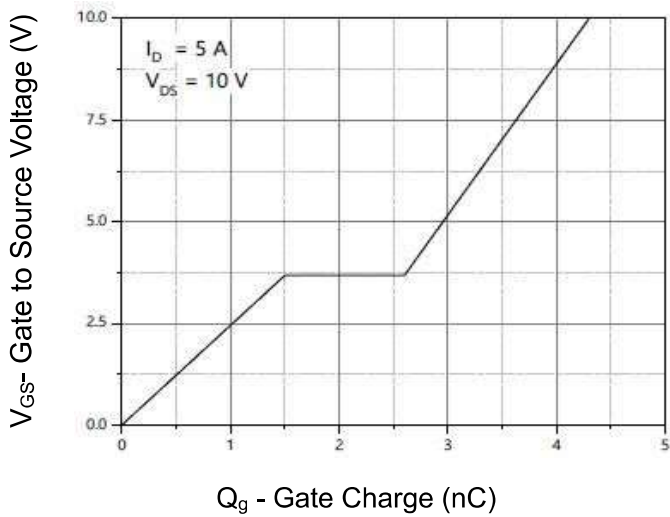
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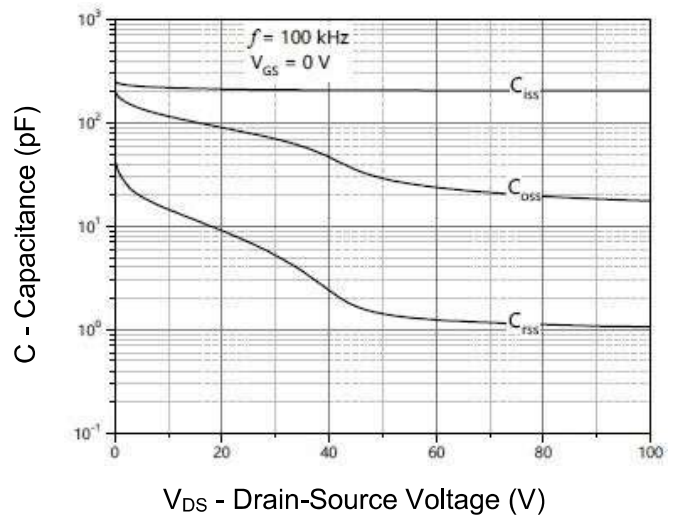
**Figure 6. Transfer Characteristics**



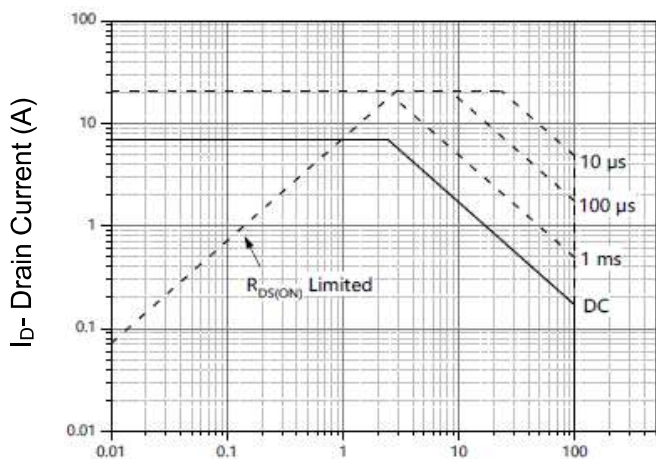
**Figure 7. Drain-Source On-State Resistance**



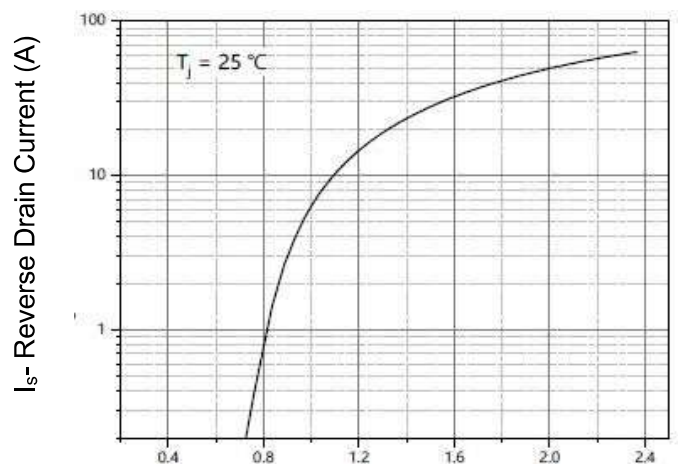
**Figure 8. Gate Charge**



**Figure 9 . Capacitance vs Vds**



**Figure 10. Safe Operation Area**



**Figure 11. Source- Drain Diode Forward**