

## N-Channel and P-Channel Enhancement Mode Power MOSFET

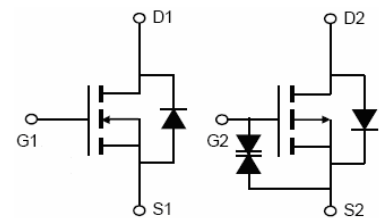
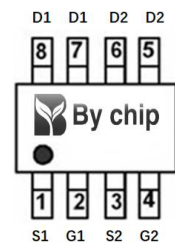
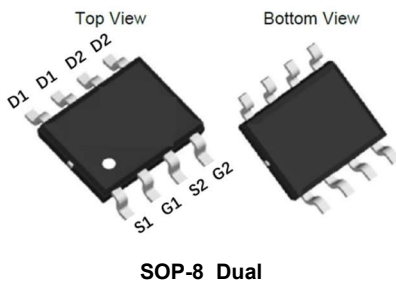
### Features

- N-Channel: 60V, 5A  
 $R_{DS(ON)} < 28 \text{ m}\Omega @ V_{GS} = 10\text{V}$   
 $R_{DS(ON)} < 31 \text{ m}\Omega @ V_{GS} = 4.5\text{V}$
- P-Channel: -60V, -3.1A  
 $R_{DS(ON)} < 62 \text{ m}\Omega @ V_{GS} = -10\text{V}$   
 $R_{DS(ON)} < 72 \text{ m}\Omega @ V_{GS} = -4.5\text{V}$

### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

**100% UIS TESTED!**  
**100%  $\Delta V_{ds}$  TESTED!**



### Absolute Maximum Ratings $T_C = 25^\circ\text{C}$ , unless otherwise noted

Parameter	Symbol	NMOS	PMOS	Unit
Drain-Source Voltage	$V_{DS}$	60	-60	V
Continuous Drain Current	$I_D$	5	-3.1	A
Pulsed Drain Current	$I_{DM}$ (note1)	20	-12.4	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	$\pm 20$	V
Power Dissipation	$P_D$	2.5	1.9	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 To 150	-55 To 150	$^\circ\text{C}$

### Thermal Resistance

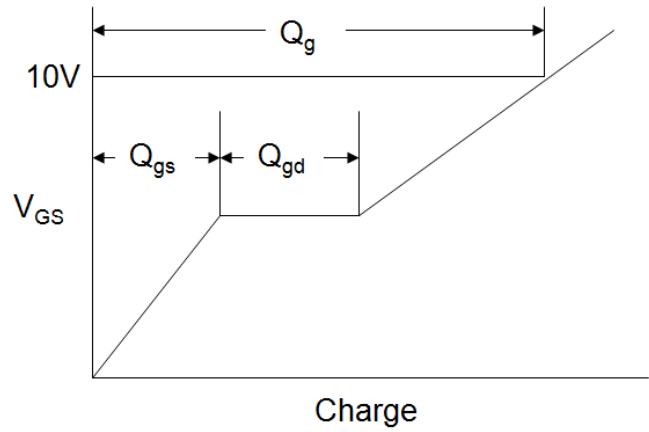
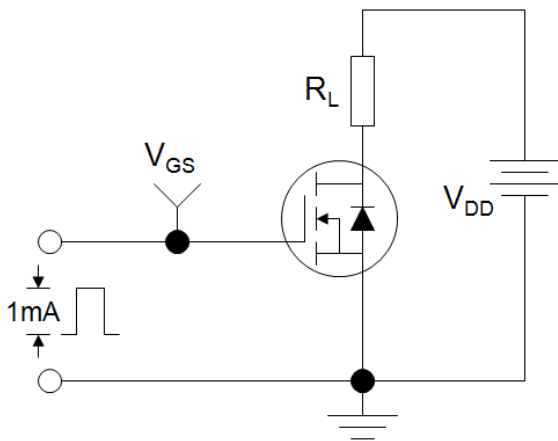
Parameter	Symbol	NMOS	PMOS	Unit
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	50	65	$^\circ\text{C}/\text{W}$

NMOS Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = 250\mu A$	60	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 60V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	1	$\mu A$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.0		2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = 10V, I_D = 4.3A$	--		28	m $\Omega$
		$V_{GS} = 4.5V, I_D = 3.9A$	--		31	
Forward Transconductance	$g_{FS}$	$V_{DS}=5V, I_D=4.3A$	--	9.6	--	S
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = 30V,$ $f = 1.0\text{MHz}$	--	1336	--	pF
Output Capacitance	$C_{oss}$		--	56	--	
Reverse Transfer Capacitance	$C_{rss}$		--	52	--	
Total Gate Charge	$Q_g$	$V_{DS} = 30V,$ $I_D = 5A,$ $V_{GS} = 10V$	--	22	--	nC
Gate-Source Charge	$Q_{gs}$		--	3.3	--	
Gate-Drain Charge	$Q_{gd}$		--	5.2	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 30V,$ $I_D = 5A,$ $R_G = 3\Omega$	--	5.2	--	ns
Turn-on Rise Time	$t_r$		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	17	--	
Turn-off Fall Time	$t_f$		--	2.5	--	
<b>Drain-Source Body Diode Characteristics</b>						
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = 1.7A, V_{GS} = 0V$	--	--	1.2	V
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	5	A

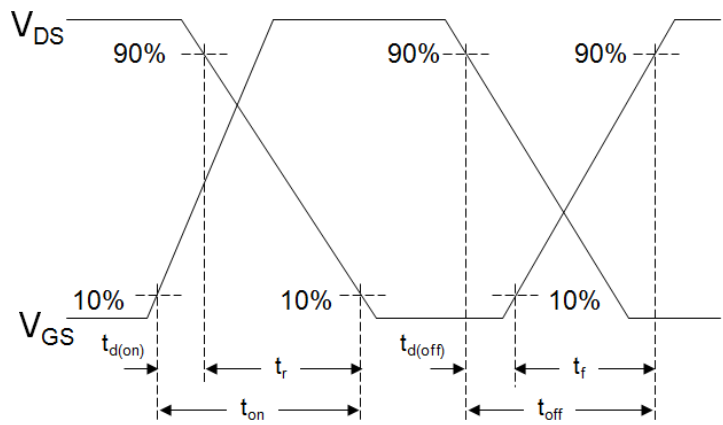
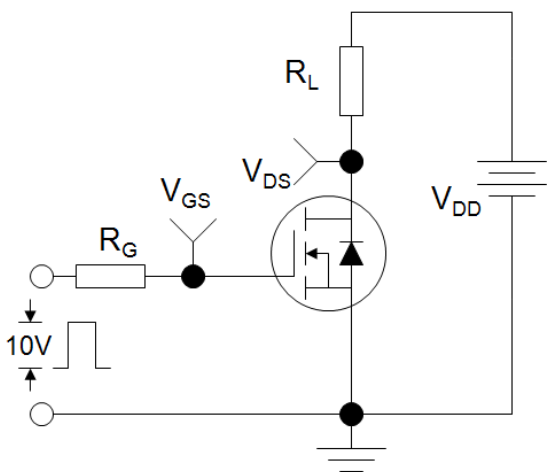
**Notes**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical  $R_G$

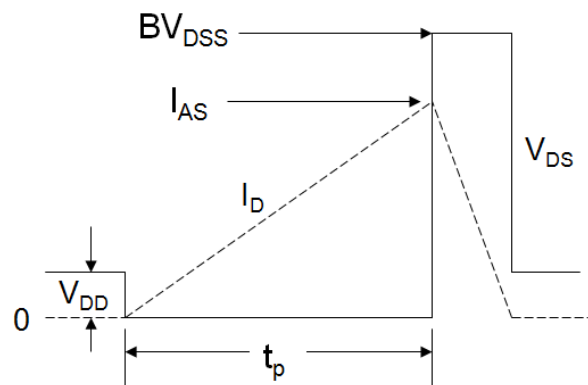
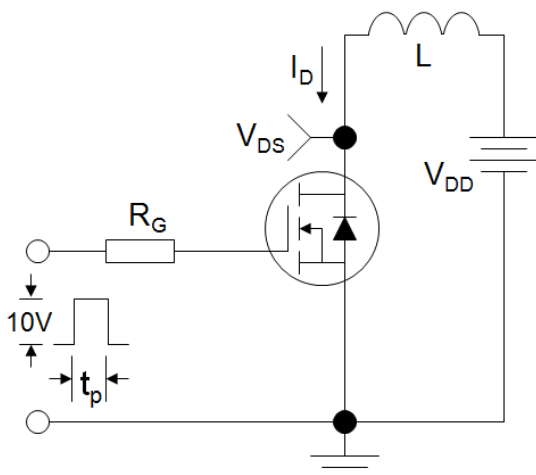
Gate Charge Test Circuit



Switch Time Test Circuit

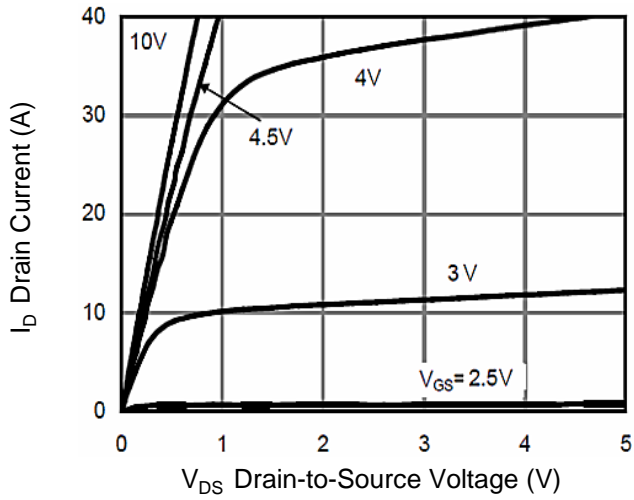


EAS Test Circuit

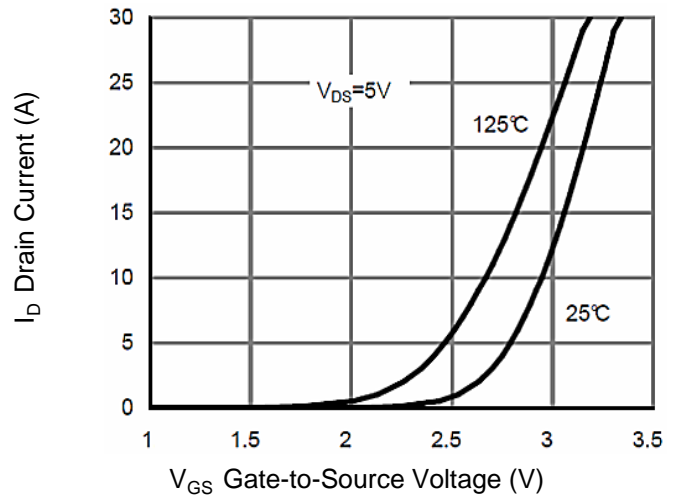


**NMOS Typical Characteristics**  $T_J = 25^\circ\text{C}$ , unless otherwise noted

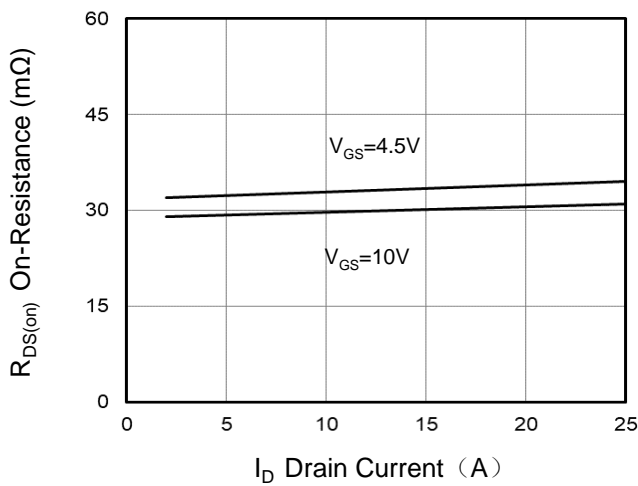
**Figure 1. Output Characteristics**



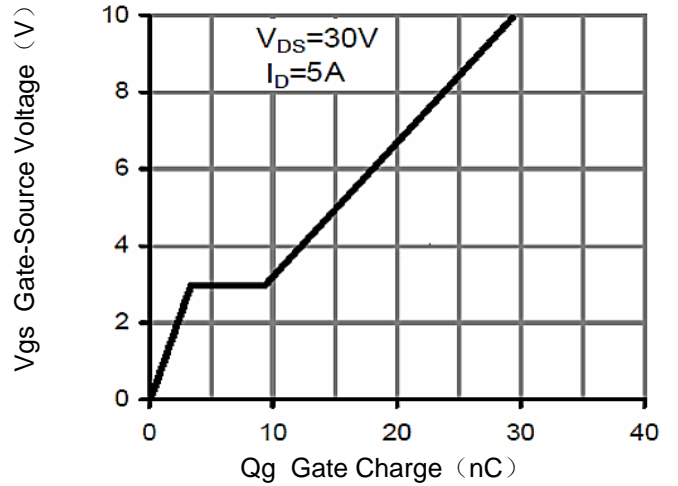
**Figure 2. Transfer Characteristics**



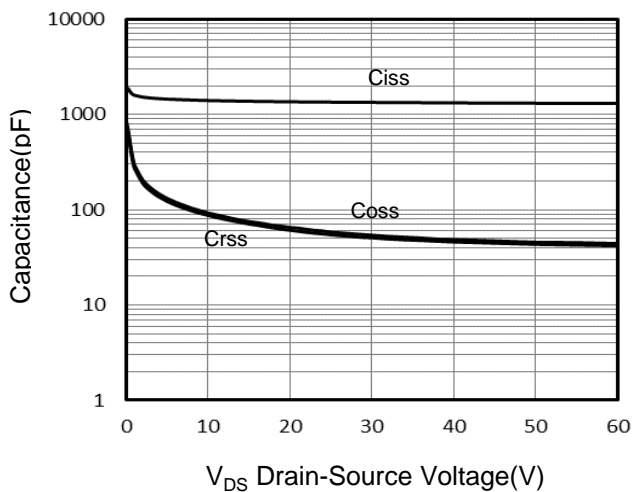
**Figure 3. Drain-Source On-Resistance**



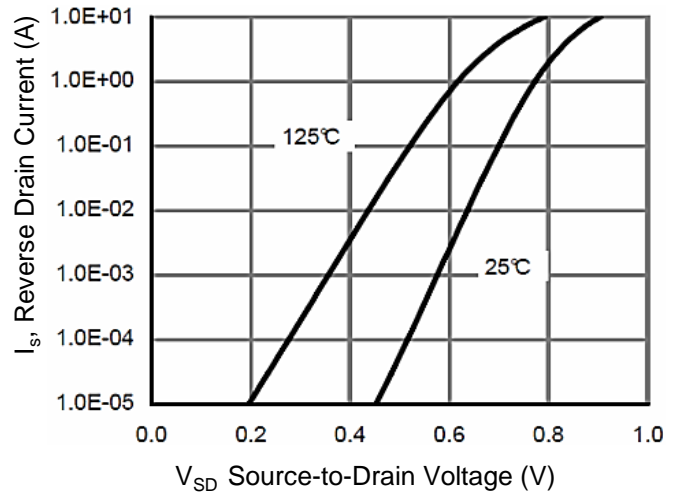
**Figure 4. Gate Charge**



**Figure 5. Capacitance**



**Figure 6. Source-Drain Diode Forward**



NMOS Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Drain-Source On-Resistance

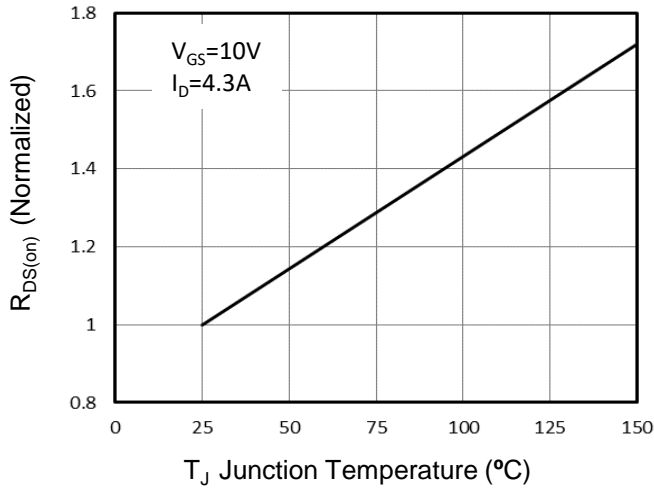


Figure 8. Safe Operation Area

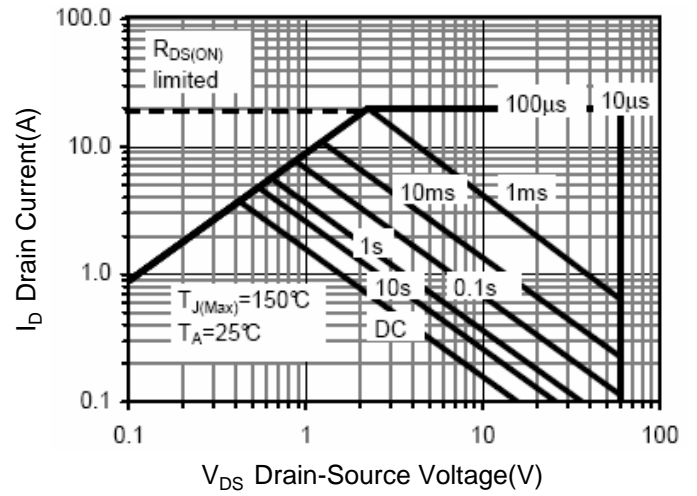
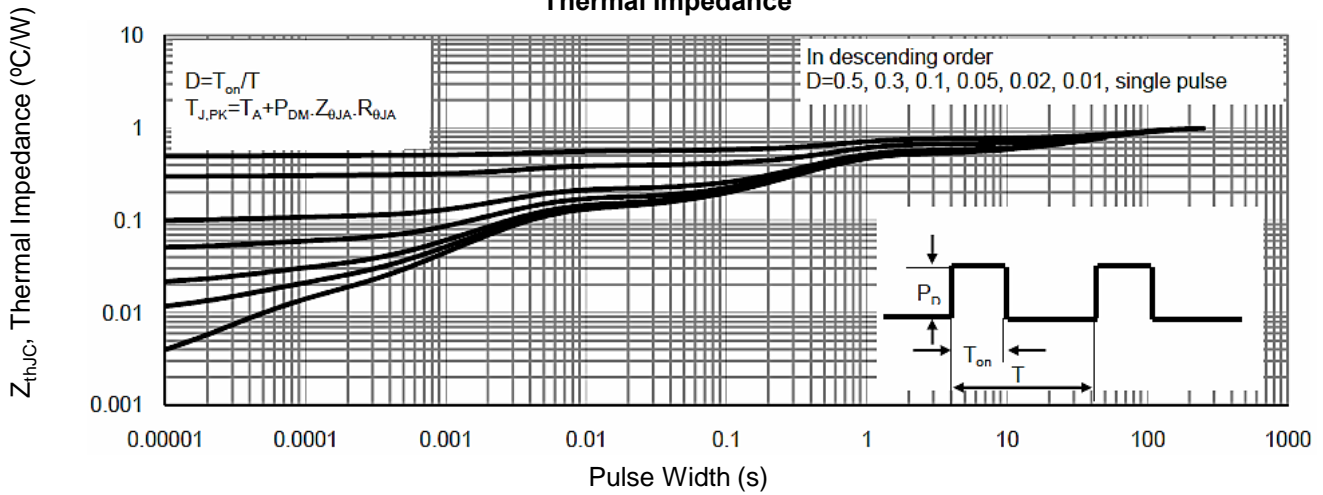


Figure 9. Normalized Maximum Transient Thermal Impedance

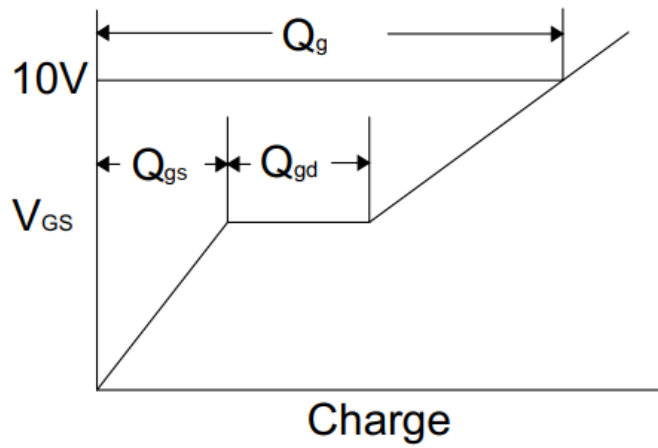
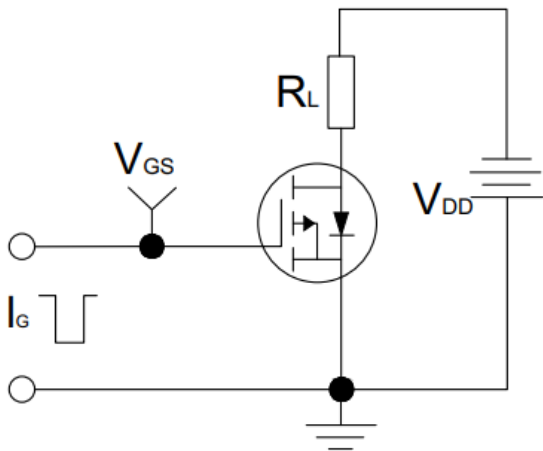


PMOS Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-60	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -60V, V_{GS} = 0V, T_J = 25^\circ\text{C}$	--	--	-1	$\mu\text{A}$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1.0		-2.5	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -3.1A$	--		62	m $\Omega$
		$V_{GS} = -4.5V, I_D = -0.2A$	--		72	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5V, I_D = -3.1A$	--	6.6	--	S
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = -30V,$ $f = 1.0\text{MHz}$	--	1454	--	pF
Output Capacitance	$C_{oss}$		--	62	--	
Reverse Transfer Capacitance	$C_{rss}$		--	58	--	
Total Gate Charge	$Q_g$	$V_{DD} = -30V,$ $I_D = -3A,$ $V_{GS} = -10V$	--	37	--	nC
Gate-Source Charge	$Q_{gs}$		--	4.5	--	
Gate-Drain Charge	$Q_{gd}$		--	10.5	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -30V,$ $I_D = -3A,$ $R_G = 3\Omega$	--	8	--	ns
Turn-on Rise Time	$t_r$		--	4	--	
Turn-off Delay Time	$t_{d(off)}$		--	32	--	
Turn-off Fall Time	$t_f$		--	7	--	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	-3.1	A
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = -2A, V_{GS} = 0V$	--	--	-1.2	V

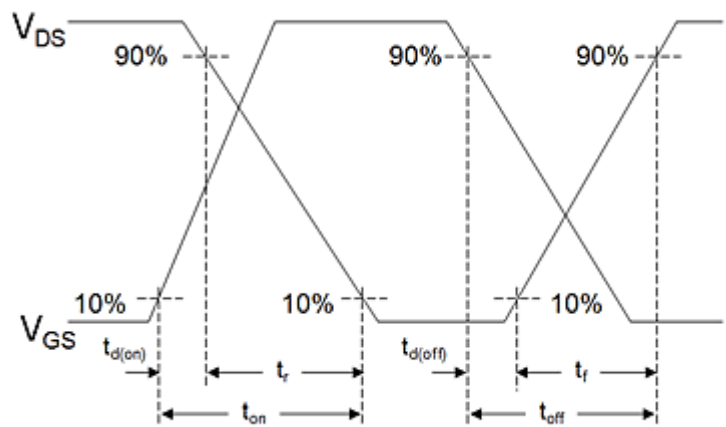
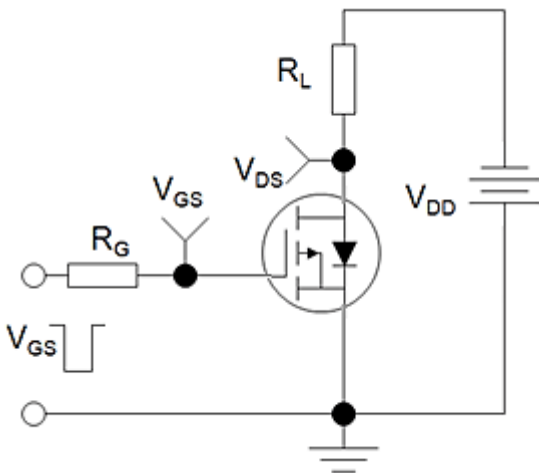
**Notes**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical  $R_G$

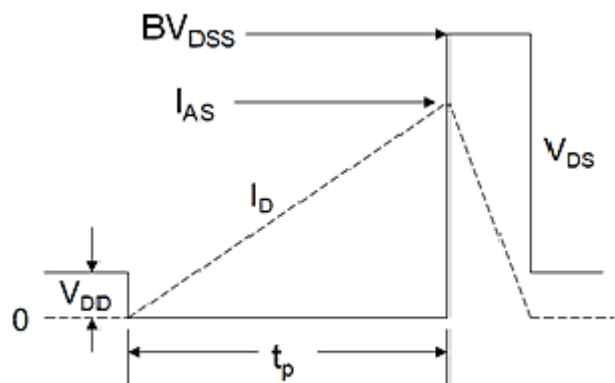
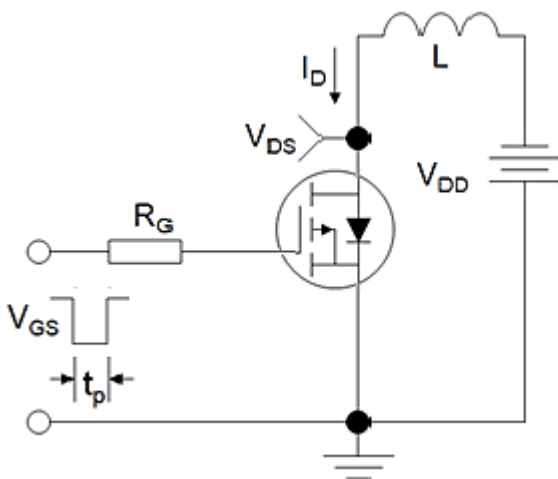
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



PMOS Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 1. Output Characteristics

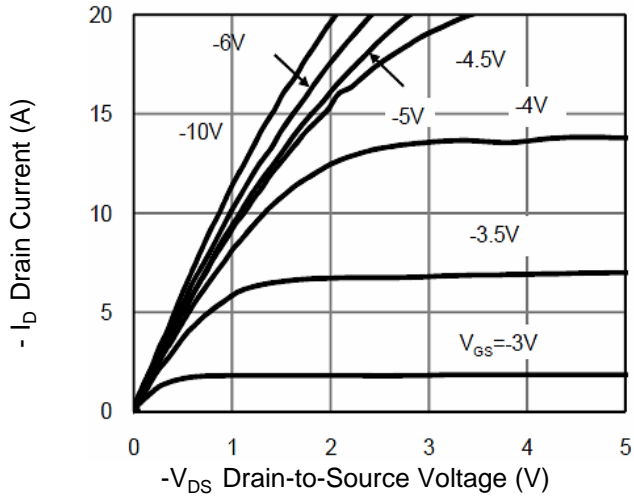


Figure 2. Transfer Characteristics

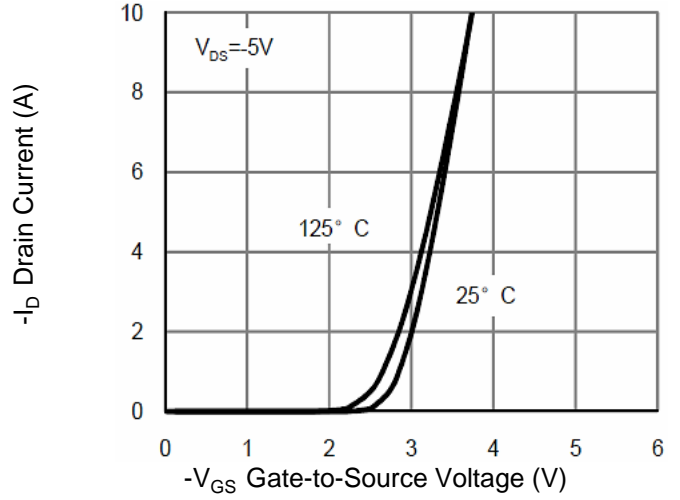


Figure 3.  $R_{DS(on)}$ -Drain Current

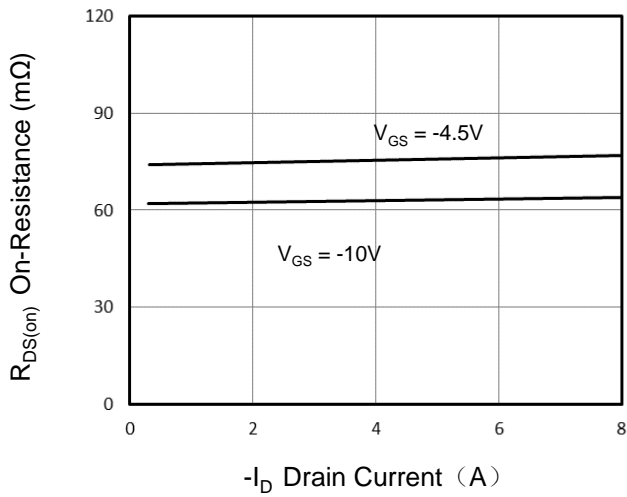


Figure 4. Gate Charge

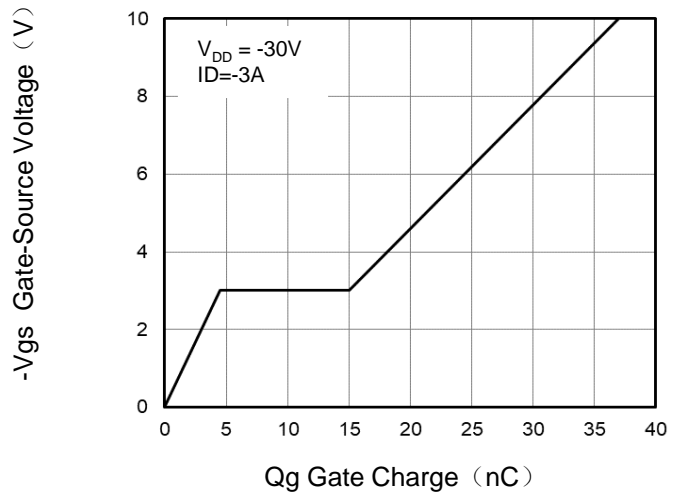


Figure 5. Capacitance

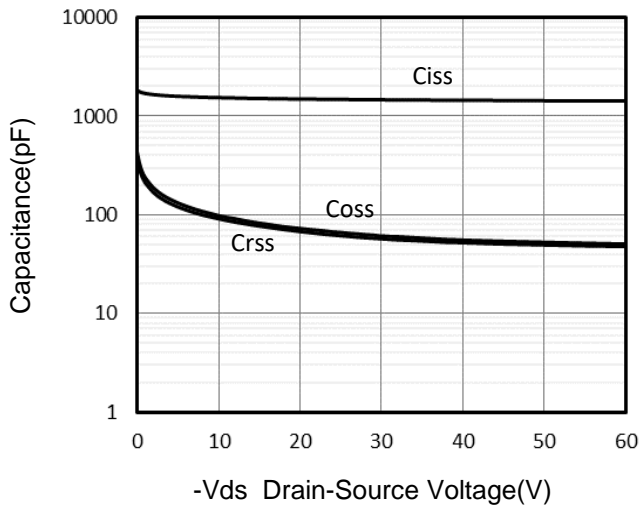
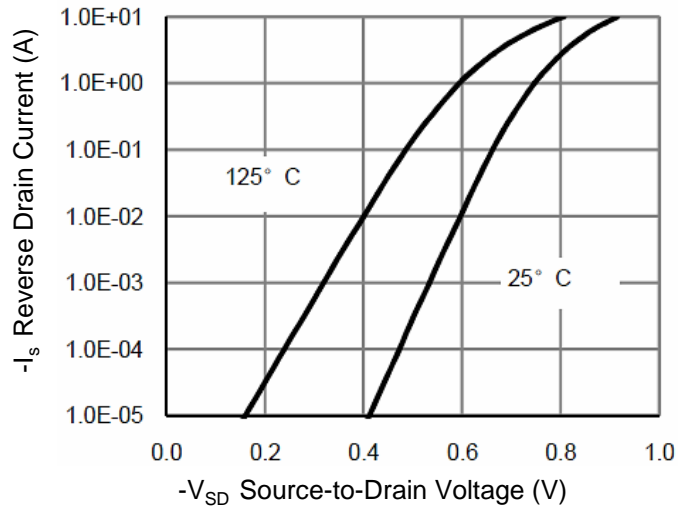


Figure 6. Source-Drain Diode Forward





PMOS Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Drain-Source On-Resistance

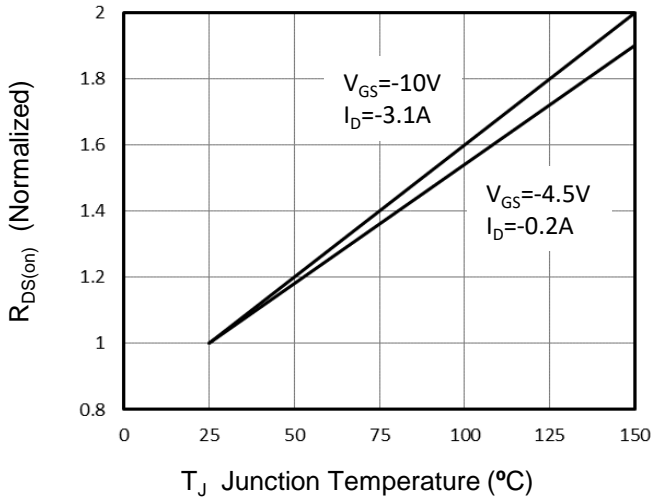


Figure 8. Safe Operation Area

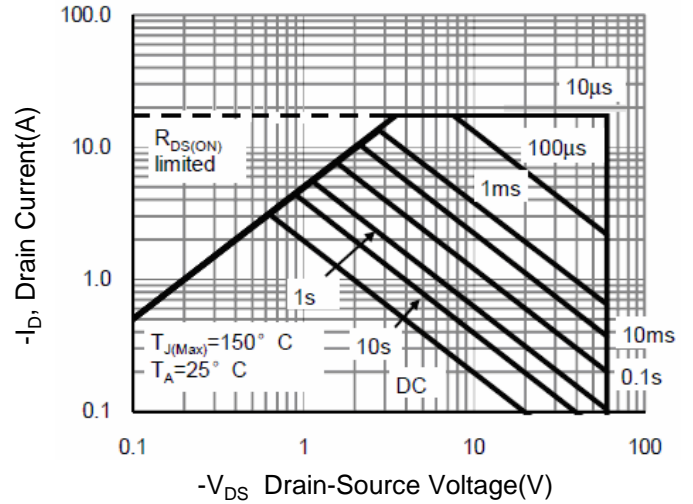


Figure 9. Normalized Maximum Transient Thermal Impedance

