

## N-Channel Enhancement Mode Power MOSFET

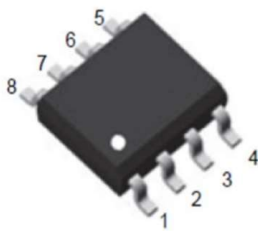
### Features

- $V_{DS} = 100V$ ,  $I_D = 10A$   
 $R_{DS(ON)} < 20\text{ m}\Omega$  @  $V_{GS} = 10V$   
 $R_{DS(ON)} < 22\text{ m}\Omega$  @  $V_{GS} = 4.5V$

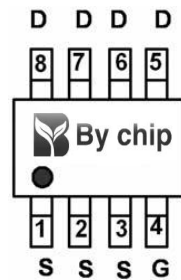
### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

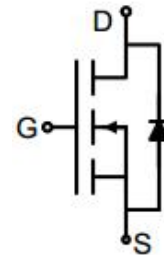
100% UIS TESTED!  
 100%  $\Delta V_{ds}$  TESTED!



SOP-8



pin assignment



Schematic diagram

### Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	$V_{DS}$	100	V
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Drain Current-Continuous	$I_D$	10	A
Drain Current-Continuous ( $T_C = 100^\circ\text{C}$ )	$I_D(100^\circ\text{C})$	7	A
Pulsed Drain Current	$I_{DM}$	70	A
Maximum Power Dissipation	$P_D$	3.1	W
Operating Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 To 150	$^\circ\text{C}$

### Thermal Characteristic

Thermal Resistance, Junction-to-Ambient <sup>(Note 2)</sup>	$R_{\theta JA}$	40	$^\circ\text{C}/\text{W}$
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**Electrical Characteristics ( $T_A=25^{\circ}\text{C}$  unless otherwise noted)**

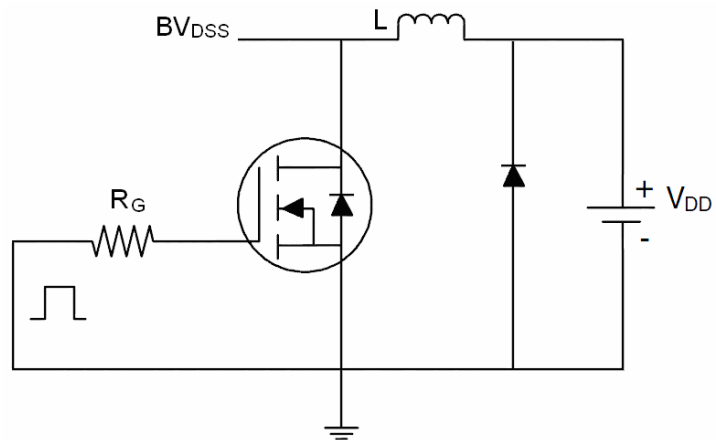
Parameter	Symbol	Condition	Min	Typ	Max	Unit
<b>Off Characteristics</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	100	110	-	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=100V, V_{GS}=0V$	-	-	1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 20V, V_{DS}=0V$	-	-	$\pm 100$	nA
<b>On Characteristics</b> <sup>(Note 3)</sup>						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1.0		2.0	V
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=10A$	-		20	m $\Omega$
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$	-		22	m $\Omega$
Forward Transconductance	$g_{FS}$	$V_{DS}=10V, I_D=10A$	-	26	-	S
<b>Dynamic Characteristics</b> <sup>(Note 4)</sup>						
Input Capacitance	$C_{iss}$	$V_{DS}=50V, V_{GS}=0V,$ $F=1.0\text{MHz}$	-	2600	-	PF
Output Capacitance	$C_{oss}$		-	590	-	PF
Reverse Transfer Capacitance	$C_{rss}$		-	291	-	PF
<b>Switching Characteristics</b> <sup>(Note 4)</sup>						
Turn-on Delay Time	$t_{d(on)}$	$V_{DD}=50V, I_D=10A, R_L=5\Omega,$ $R_G=1\Omega, V_{GS}=10V$	-	13	-	nS
Turn-on Rise Time	$t_r$		-	14	-	nS
Turn-Off Delay Time	$t_{d(off)}$		-	25	-	nS
Turn-Off Fall Time	$t_f$		-	10	-	nS
Total Gate Charge	$Q_g$	$I_D=10A, V_{DD}=50V, V_{GS}=10V$	-	90	-	nC
Gate-Source Charge	$Q_{gs}$		-	16	-	nC
Gate-Drain Charge	$Q_{gd}$		-	24	-	nC
<b>Drain-Source Diode Characteristics</b>						
Diode Forward Voltage <sup>(Note 3)</sup>	$V_{SD}$	$V_{GS}=0V, I_S=10A$	-	0.85	1.2	V
Diode Forward Current <sup>(Note 2)</sup>	$I_S$		-	-	10	A
Reverse Recovery Time	$t_{rr}$	$T_J = 25^{\circ}\text{C}, I_F = 10A$ $di/dt = 100A/\mu s$ <sup>(Note 3)</sup>	-	33	-	nS
Reverse Recovery Charge	$Q_{rr}$		-	54	-	nC

**Notes:**

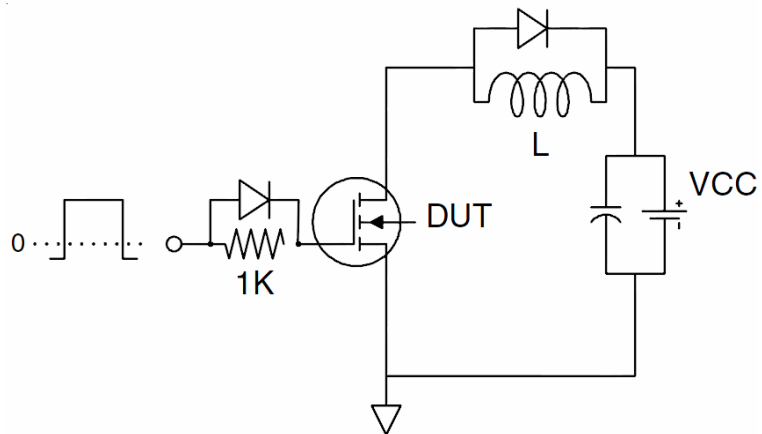
1. Repetitive Rating: Pulse width limited by maximum junction temperature.
2. Surface Mounted on FR4 Board,  $t \leq 10$  sec.
3. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty Cycle  $\leq 2\%$ .
4. Guaranteed by design, not subject to production

**Test Circuit**

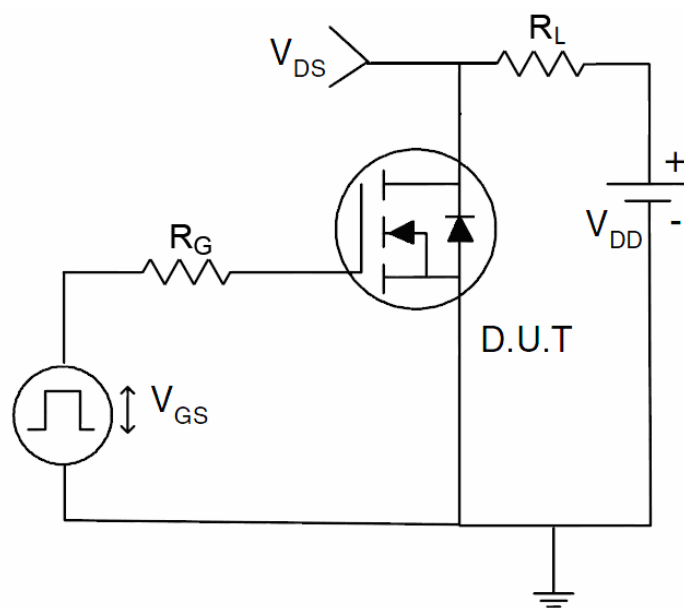
**1)  $E_{AS}$  test Circuit**



**2) Gate charge test Circuit**



**3) Switch Time Test Circuit**



Typical Electrical and Thermal Characteristics (Curves)

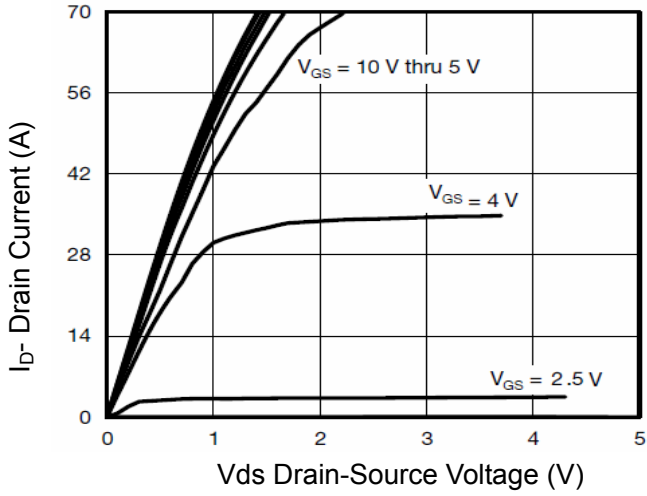


Figure 1 Output Characteristics

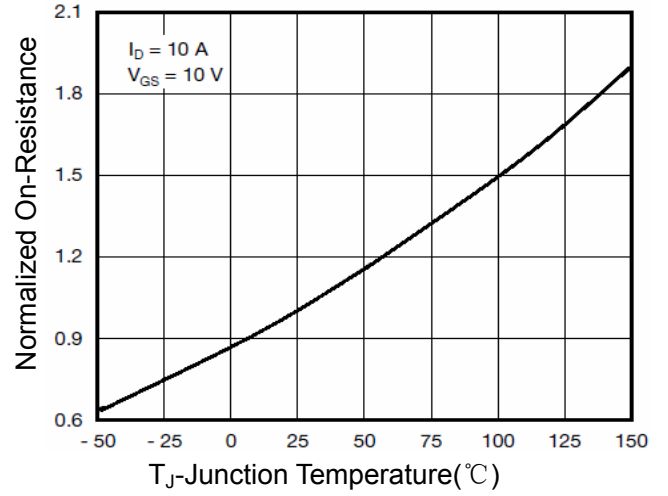


Figure 4 Rds(on)-Junction Temperature

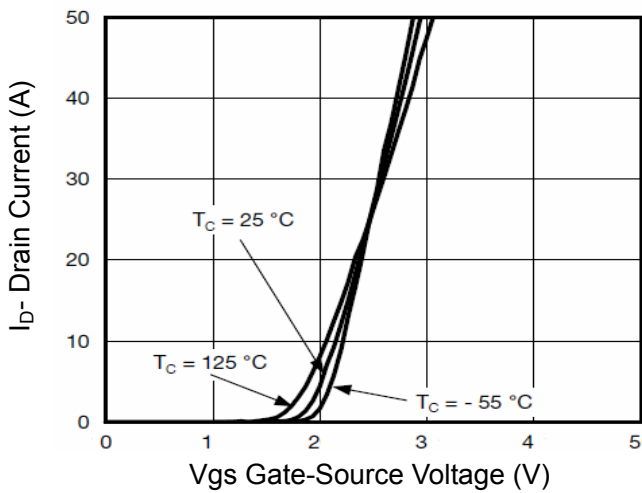


Figure 2 Transfer Characteristics

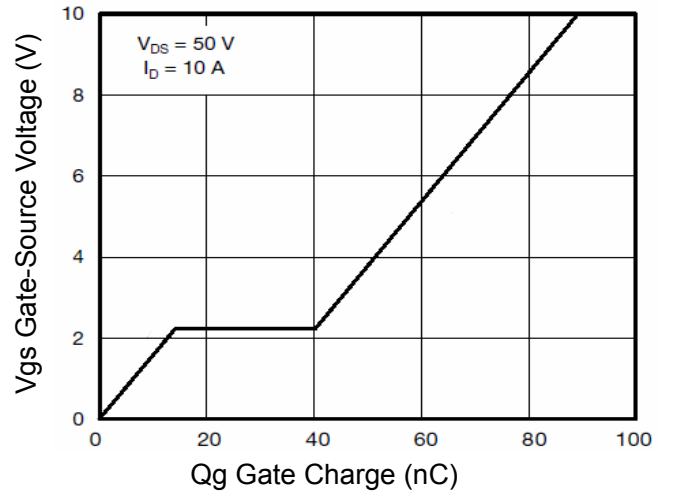


Figure 5 Gate Charge

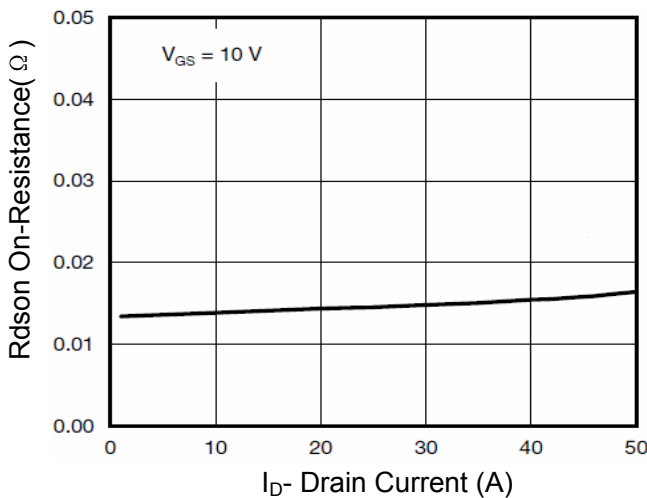


Figure 3 Rds(on)- Drain Current

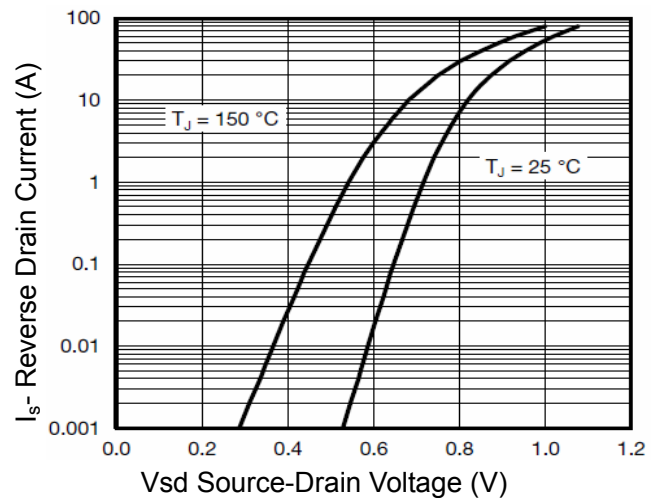


Figure 6 Source- Drain Diode Forward

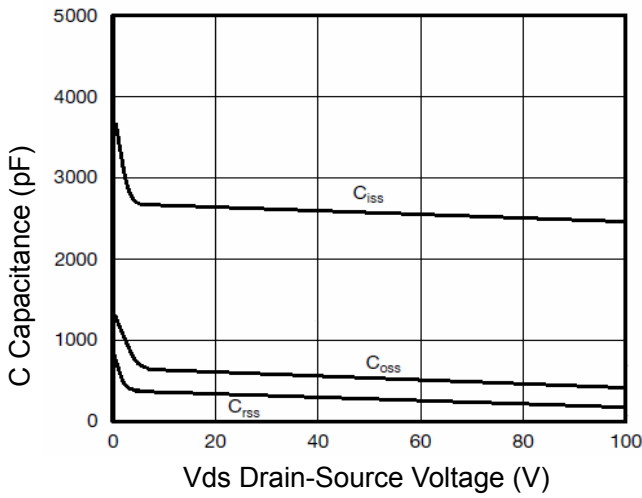


Figure 7 Capacitance vs Vds

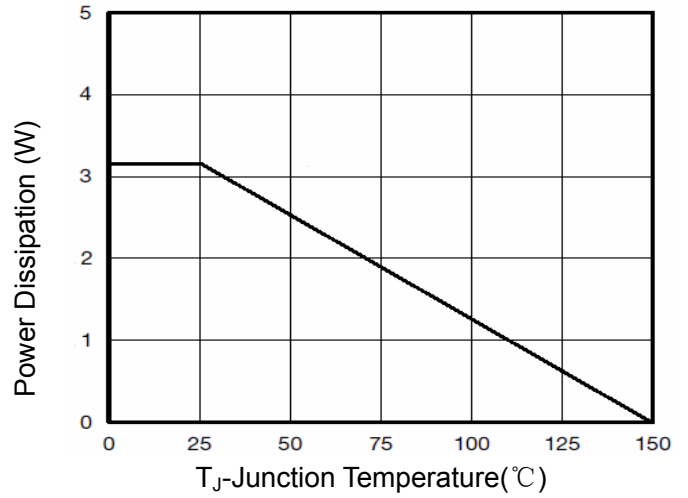


Figure 9 Power De-rating

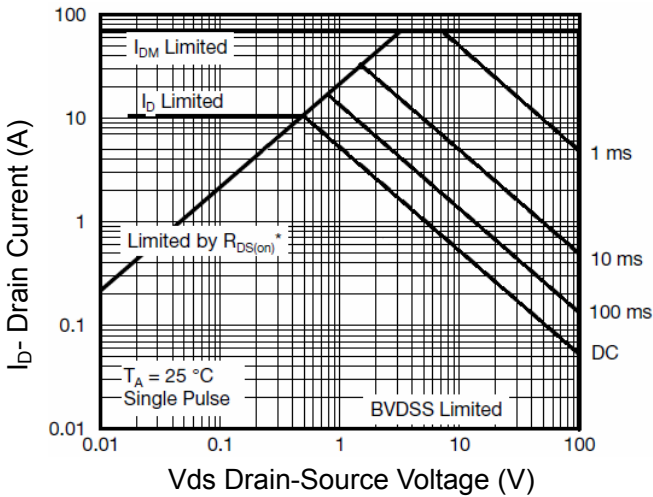


Figure 8 Safe Operation Area

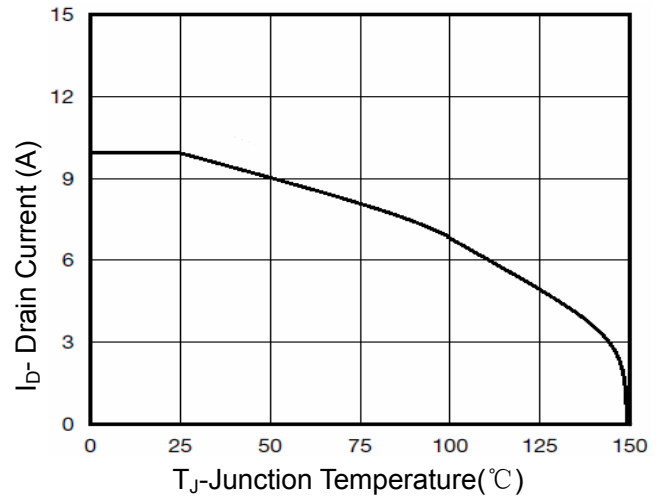


Figure 10 Current De-rating

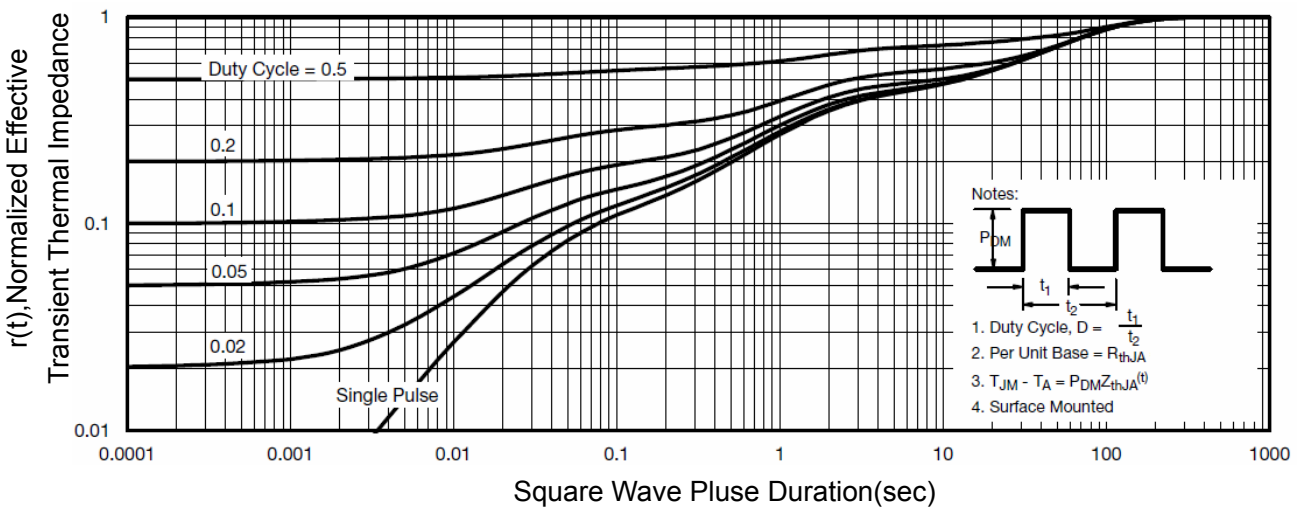


Figure 11 Normalized Maximum Transient Thermal Impedance