

## Dual P-channel Enhancement Mode Power MOSFET

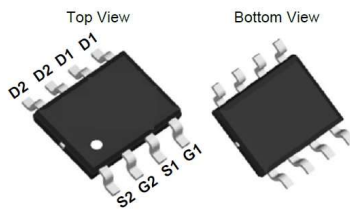
### Features

- $V_{DS} = -30V$ ,  $I_D = -9A$   
 $R_{DS(ON)} < 15m\Omega @ V_{GS} = -10V$   
 $R_{DS(ON)} < 20m\Omega @ V_{GS} = -4.5V$

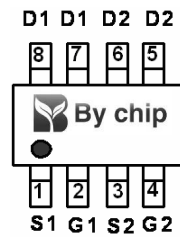
### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

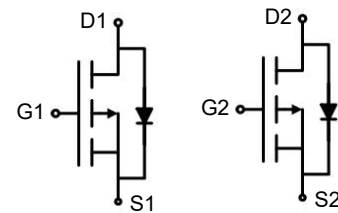
100% UIS TESTED!  
 100%  $\Delta V_{ds}$  TESTED!



SOP-8 (Dual)



Pin assignment



Schematic diagram

Absolute Maximum Ratings $T_C = 25^\circ C$ , unless otherwise noted			
Parameter	Symbol	Value	Unit
Drain-Source Voltage	$V_{DS}$	-30	V
Continuous Drain Current	$I_D$	-9	A
Pulsed Drain Current (note1)	$I_{DM}$	-36	A
Gate-Source Voltage	$V_{GS}$	$\pm 20$	V
Power Dissipation	$P_D$	1.4	W
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	-55 To 150	$^\circ C$

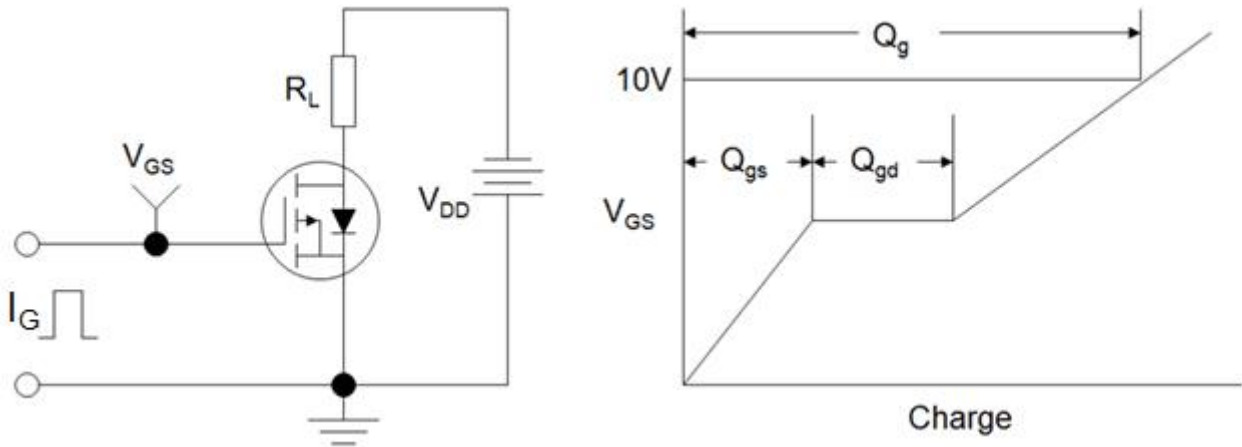
Thermal Resistance			
Parameter	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{thJA}$	90	$^\circ C/W$

Specifications $T_J = 25^\circ\text{C}$ , unless otherwise noted						
Parameter	Symbol	Test Conditions	Value			Unit
			Min.	Typ.	Max.	
<b>Static Parameters</b>						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0V, I_D = -250\mu\text{A}$	-30	--	--	V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = -30V, V_{GS} = 0V$	--	--	-1	$\mu\text{A}$
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 20V$	--	--	$\pm 100$	nA
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250\mu\text{A}$	-1		-3.0	V
Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS} = -10V, I_D = -5A$	--		15	m $\Omega$
		$V_{GS} = -4.5V, I_D = -5A$	--		20	
Forward Transconductance	$g_{FS}$	$V_{DS} = -5V, I_D = -5A$	--	12	--	S
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{GS} = 0V,$ $V_{DS} = -4.5V,$ $f = 1.0\text{MHz}$	--	1786	--	pF
Output Capacitance	$C_{oss}$		--	237	--	
Reverse Transfer Capacitance	$C_{rss}$		--	208	--	
Total Gate Charge	$Q_g$	$V_{DD} = -15V,$ $I_D = -4.5A,$ $V_{GS} = -10V$	--	18	--	nC
Gate-Source Charge	$Q_{gs}$		--	3.4	--	
Gate-Drain Charge	$Q_{gd}$		--	3	--	
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = -15V,$ $I_D = -4.5A,$ $R_G = 1\Omega$	--	6	--	ns
Turn-on Rise Time	$t_r$		--	3	--	
Turn-off Delay Time	$t_{d(off)}$		--	21	--	
Turn-off Fall Time	$t_f$		--	3	--	
<b>Drain-Source Body Diode Characteristics</b>						
Continuous Body Diode Current	$I_S$	$T_C = 25^\circ\text{C}$	--	--	-9	A
Body Diode Voltage	$V_{SD}$	$T_J = 25^\circ\text{C}, I_{SD} = -5A, V_{GS} = 0V$	--	--	-1.2	V
Reverse Recovery Charge	$Q_{rr}$	$I_F = -4.5A, V_{GS} = 0V$ $di/dt = -500A/\mu\text{s}$	--	13	--	nC
Reverse Recovery Time	$T_{rr}$		--	8.5	--	ns

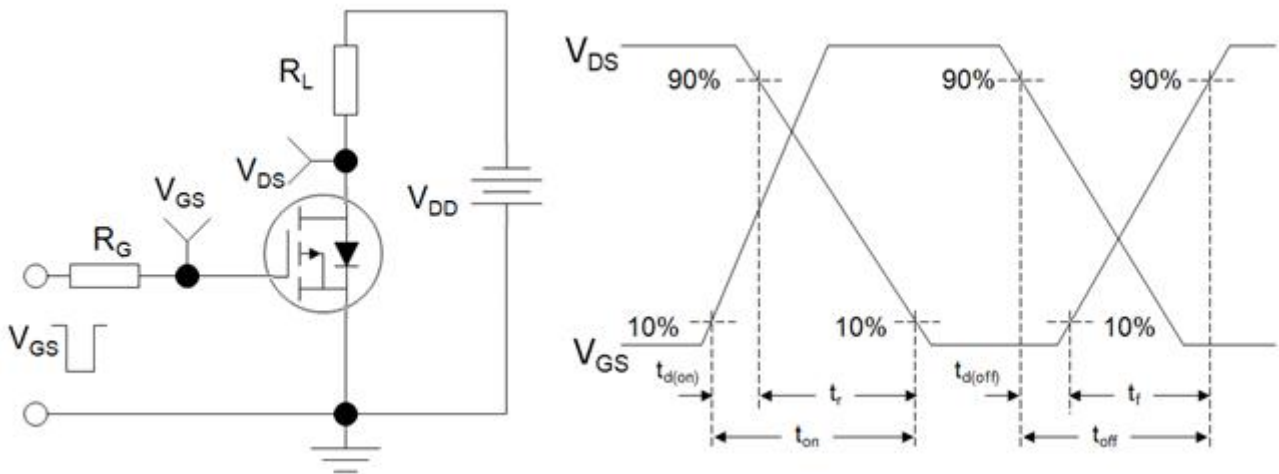
**Notes**

1. Repetitive Rating: Pulse width limited by maximum junction temperature
2. Identical low side and high side switch with identical  $R_G$

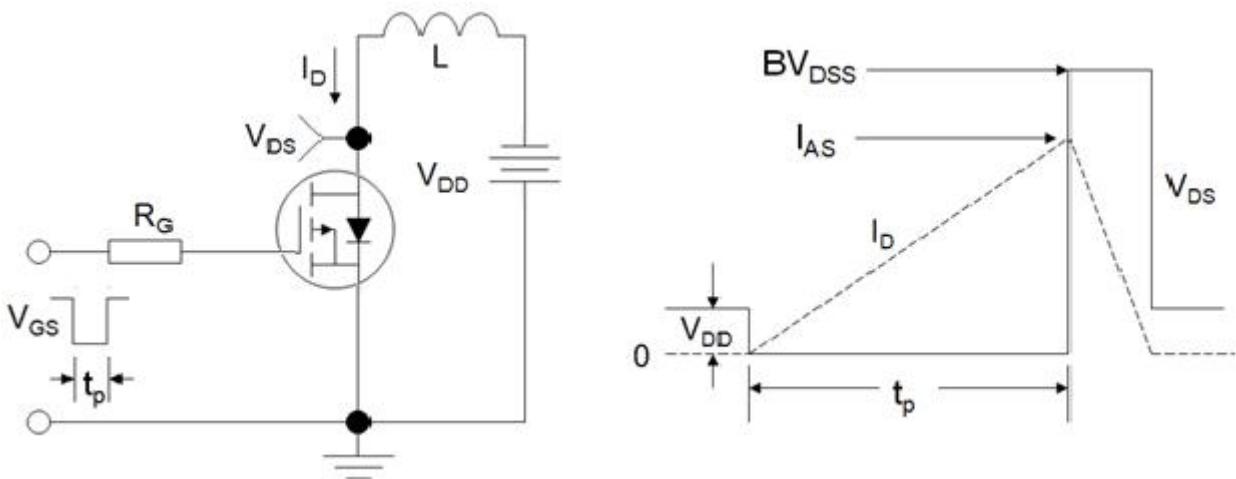
Gate Charge Test Circuit



Switch Time Test Circuit



EAS Test Circuit



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 1. Output Characteristics

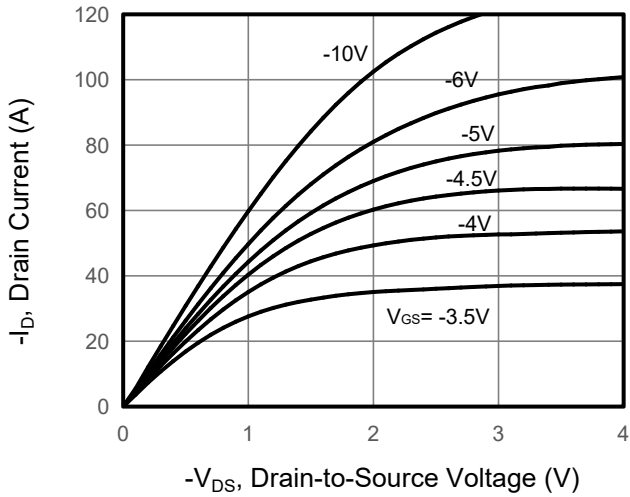


Figure 2. Transfer Characteristics

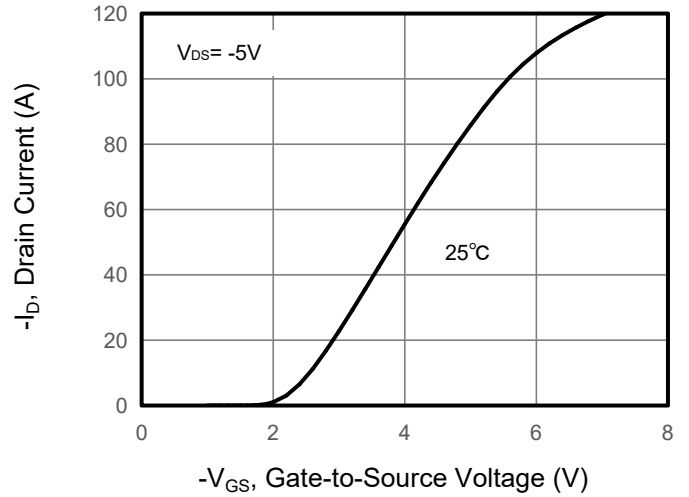


Figure 3. Drain Source On Resistance

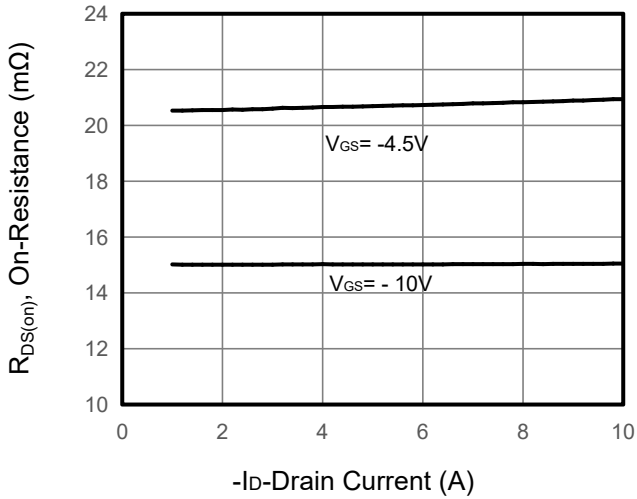


Figure 4. Gate Charge

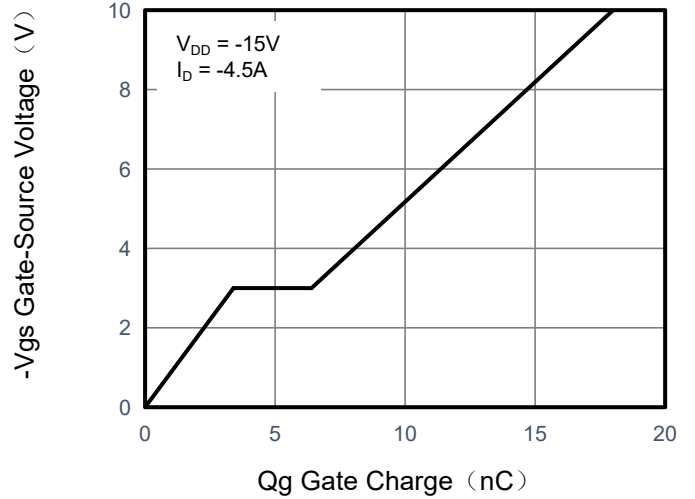


Figure 5. Capacitance

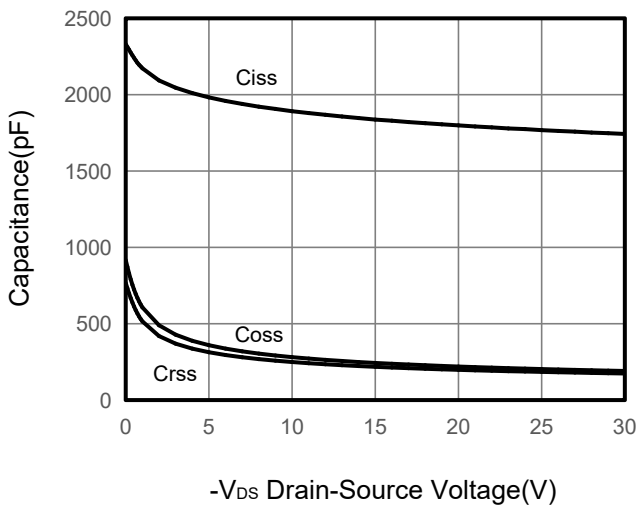
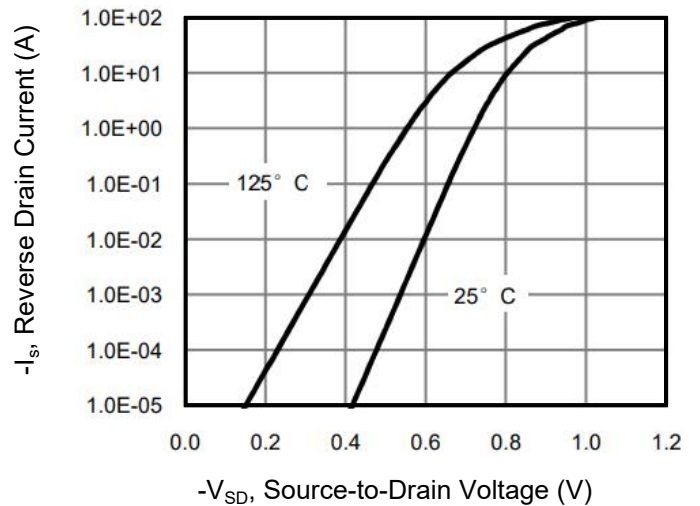


Figure 6. Source-Drain Diode Forward



Typical Characteristics  $T_J = 25^\circ\text{C}$ , unless otherwise noted

Figure 7. Drain-Source On-Resistance

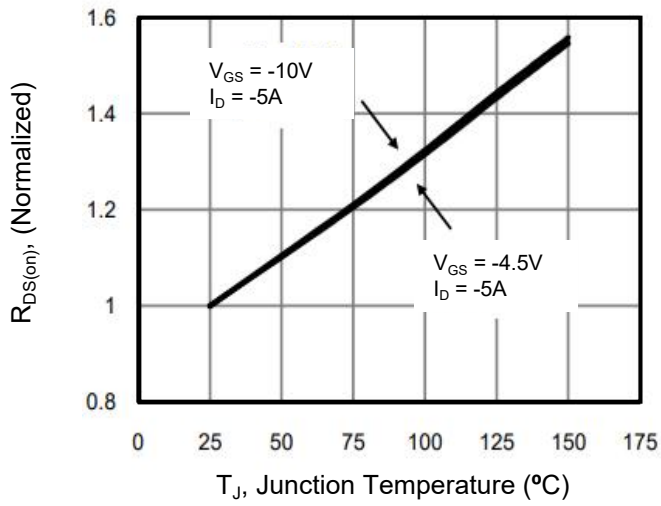


Figure 10. Safe Operation Area

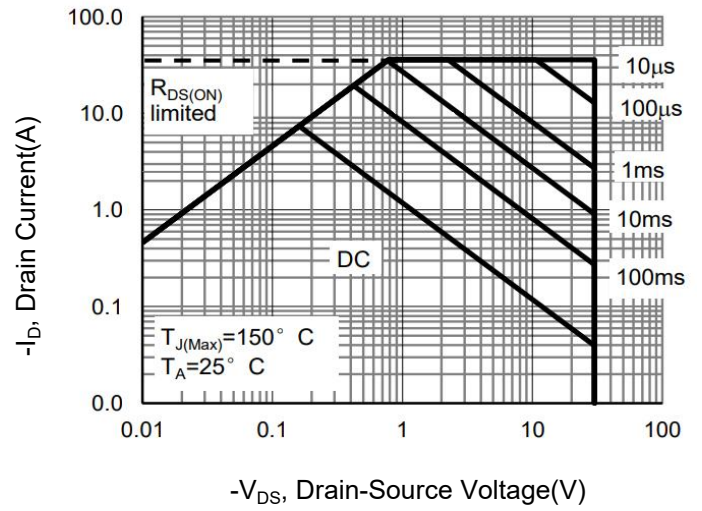


Figure 9. Normalized Maximum Transient Thermal Impedance

