

## N-Channel Enhancement Mode Power MOSFET

### Features

- $V_{DS} = 20V$ ,  $I_D = 10A$   
 $R_{DS(ON)} < 11\text{ m}\Omega$  @  $V_{GS} = 4.5V$   
 $R_{DS(ON)} < 14\text{ m}\Omega$  @  $V_{GS} = 2.5V$

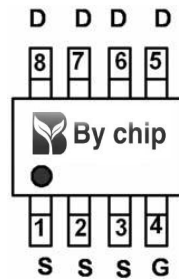
### General Features

- Advanced Trench Technology
- Provide Excellent  $R_{DS(ON)}$  and Low Gate Charge
- Lead Free and Green Available

100% UIS TESTED!  
 100%  $\Delta V_{ds}$  TESTED!



SOP-8



pin assignment



Schematic diagram

### ■ Absolute Maximum Ratings ( $T_A = 25^\circ\text{C}$ unless otherwise noted)

Parameter	Symbol	Limit	Unit
Drain-source Voltage	$V_{DS}$	20	V
Gate-source Voltage	$V_{GS}$	$\pm 10$	V
Drain Current	$I_D$	$T_A = 25^\circ\text{C}$	10
		$T_A = 70^\circ\text{C}$	8
Pulsed Drain Current <sup>A</sup>	$I_{DM}$	45	A
Total Power Dissipation	$P_D$	$T_A = 25^\circ\text{C}$	1.9
		$T_A = 70^\circ\text{C}$	1.2
Thermal Resistance Junction-to-Ambient <sup>B</sup>	$R_{\theta JA}$	66	$^\circ\text{C}/\text{W}$
Junction and Storage Temperature Range	$T_J, T_{STG}$	-55 ~ +150	$^\circ\text{C}$

**■ Electrical Characteristics** ( $T_J=25^{\circ}\text{C}$  unless otherwise noted)

Parameter	Symbol	Conditions	Min	Typ	Max	Units
<b>Static Parameter</b>						
Drain-Source Breakdown Voltage	$BV_{DSS}$	$V_{GS}=0V, I_D=250\mu A$	20			V
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=20V, V_{GS}=0V$			1	$\mu A$
Gate-Body Leakage Current	$I_{GSS}$	$V_{GS}=\pm 10V, V_{DS}=0V$			$\pm 100$	nA
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	0.5		2.0	V
Static Drain-Source On-Resistance	$R_{DS(on)}$	$V_{GS}=4.5V, I_D=10A$			11	m $\Omega$
		$V_{GS}=2.5V, I_D=4A$			14	
		$V_{GS}=1.8V, I_D=2A$			18.2	
Diode Forward Voltage	$V_{SD}$	$I_S=10A, V_{GS}=0V$			1.2	V
<b>Dynamic Parameters</b>						
Input Capacitance	$C_{iss}$	$V_{DS}=10V, V_{GS}=0V, f=1\text{MHZ}$		888		pF
Output Capacitance	$C_{oss}$			133		
Reverse Transfer Capacitance	$C_{rss}$			117		
<b>Switching Parameters</b>						
Total Gate Charge	$Q_g$	$V_{GS}=4.5V, V_{DS}=10V, I_D=6.8A$		11.05		nC
Gate-Source Charge	$Q_{gs}$			1.73		
Gate-Drain Charge	$Q_{gd}$			3.1		
Turn-on Delay Time	$t_{D(on)}$	$V_{GS}=4.5V, V_{DS}=10V, I_D=6.8A$ $R_{GEN}=3\Omega$		7		ns
Turn-on Rise Time	$t_r$			46		
Turn-off Delay Time	$t_{D(off)}$			30		
Turn-off fall Time	$t_f$			52		

A. Pulse Test: Pulse Width  $\leq 300\mu s$ , Duty cycle  $\leq 2\%$ .

B.  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance, where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design, while  $R_{\theta JA}$  is determined by the board design. The maximum rating presented here is based on mounting on a 1 in 2 pad of 2oz copper.

■ Typical Performance Characteristics



Figure1. Output Characteristics



Figure2. Transfer Characteristics



Figure 3: On-Resistance vs. Drain Current and Gate Voltage

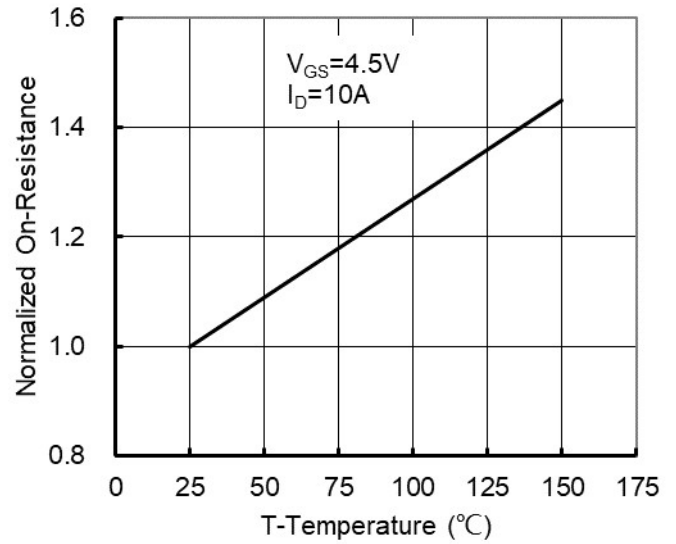


Figure 4: On-Resistance vs. Junction Temperature



Figure5. Capacitance Characteristics

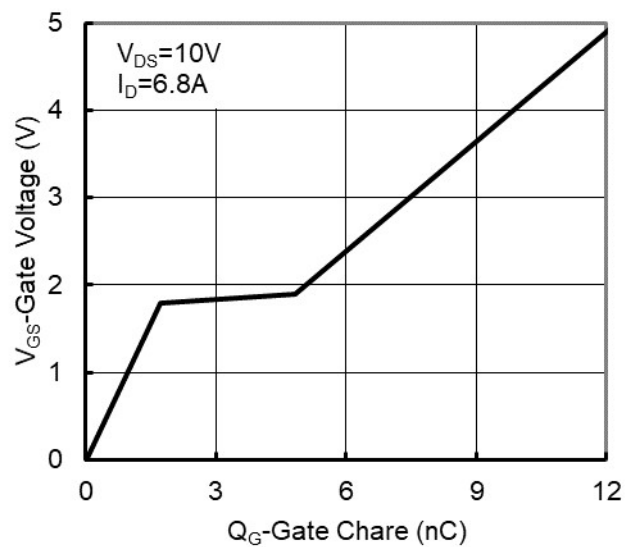


Figure6. Gate Charge



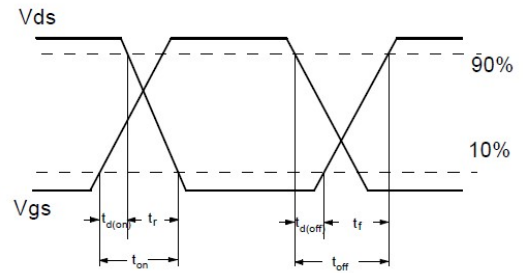
Figure7. Safe Operation Area



Figure8. Maximum Continuous Drain Current vs Ambient Temperature



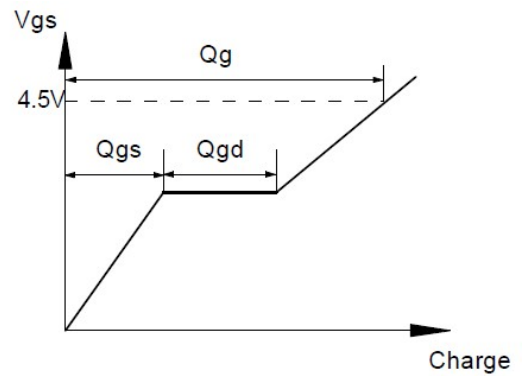
Figure9. Normalized Maximum Transient Thermal Impedance



**Resistive Switching Test Circuit & Waveforms**



**Diode Recovery Test Circuit & Waveforms**



**Gate Charge Test Circuit & Waveform**



**Unclamped Inductive Switching (UIS) Test Circuit & Waveforms**