ZTM160HXXE6601-C2

Final Product Specification

Rev. 0

REVISION HISTORY

Revision No.	Page	Description of Changes	Date	Prepared
P0	32	Release	2023.12.07	

Contents

1.0 GENERAL DESCRIPTION

1.1 Introduction

ZTM160HXXE6601-C2 is a color active matrix TFT LCD module using amorphous silicon TFT's (Thin Film Transistors) as an active switching devices. This module has a 16.0 inch diagonally measured active area with WUXGA resolutions (1920 horizontal by 1200 vertical pixel array). Each pixel is divided into RED, GREEN, BLUE dots which are arranged in vertical stripe and this module can display 16.7M(8bit) colors. The TFT-LCD panel used for this module is a low reflection and higher color type. Therefore, this module is suitable for Notebook PC. The LED driver for back-light driving is built in this model.

All input signals are eDP1.2 interface compatible.

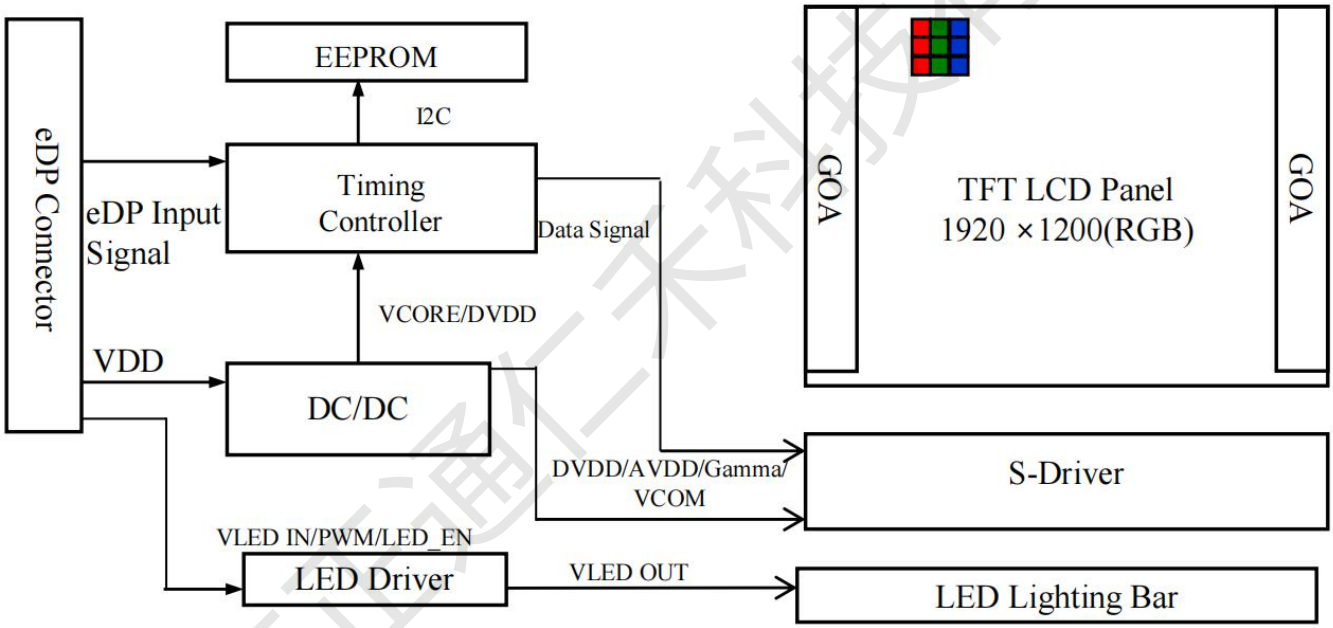


Figure 1. Drive Architecture

1.2 Features

2 lane eDP interface with 2.7Gbps link rates
16.7M(8 bit) color depth
Single LED lighting bar (Bottom side/Horizontal Direction)
Data enable signal mode
Green product (RoHS & Halogen free product)
On board LED driving circuit
Low driving voltage and low power consumption
On board EDID chip
Side mounting frame

1.3 Application

Drawing Board

1.4 General Specification

The followings are general specifications at the model ZTM160HXXE6601-C2(listed in Table 1)

<Table 1. General Specifications>

Parameter	Specification	Unit	Remarks
Active area	344.68(H) x215.42(V)	mm	
Number of pixels	1920(H) x RGB(3) x1200 (V)	pixels	
Pixel pitch	179.52(H) x59.84(V)	um	
Pixel arrangement	RGB Vertical stripe		
Display colors	16.7M(8bit)		
Color gamut	45% typ		NTSC
Display mode	Normally Black		
Dimensional outline	349.68 (H)*233.22(V) *2.9(D)	mm	
Weight	-(max)	g	
Surface treatment	AG		
Surface hardness	-		
Power consumption	P_D :0.65(Max)@60Hz	W	@Mosaic
	P_{BL} : 4.104	W	
	P_{Total} : 4.754	W	

2.0 ABSOLUTE MAXIMUM RATINGS

The followings are maximum values which, if exceed, may cause faulty operation or damage to the unit.The operational and non-operational maximum voltage and current values are listed in Table 2.

< Table 2. Absolute Maximum Ratings>

Ta=25+/-2°C

Parameter	Symbol	Min.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	-0.3	4.0	V	Note 1
eDP input Voltage	V_{eDP}	0	2.0	V	
Logic Supply Voltage	V_{IN}	Vss-0.3	V_{DD}+0.3	V	
Operating Temperature	T_{OP}	0	+50	°C	Note 2
Storage Temperature	T_{ST}	-20	+60	°C	

Notes :
1. Permanent damage to the device may occur if maximum values are exceeded functional operation should be restricted to the condition described under normal operating conditions.
2. Temperature and relative humidity range are shown in the figure below.
90 % RH Max. (40 °C ≥ Ta) Maximum wet - bulb temperature at 39 °C or less. (Ta > 40 °C)
No condensation.

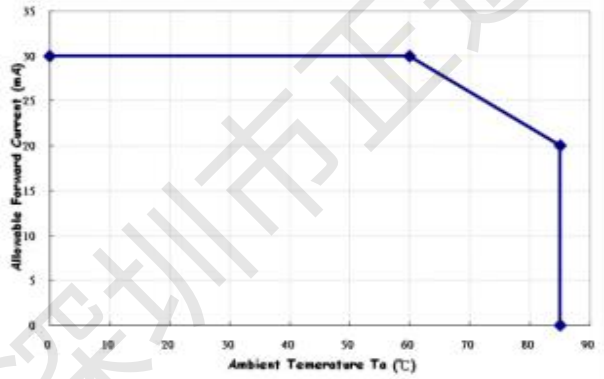


Figure 2. forward current vs ambient temperature

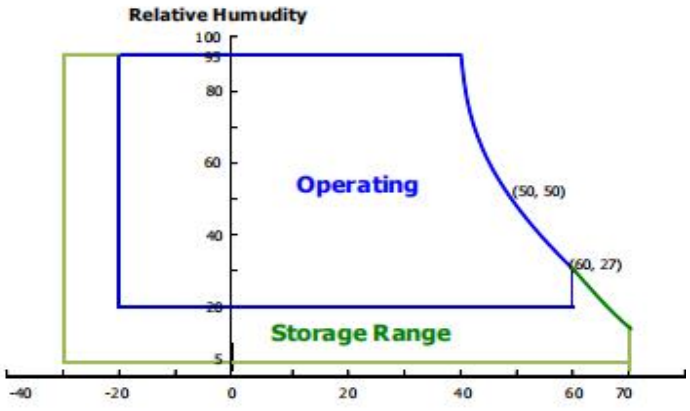


Figure 3. Operation temperature vs Humudity

3.0 ELECTRICAL SPECIFICATIONS

3.1 Electrical Specifications

< Table 3. Electrical Specifications > Ta=25+/-2°C

Parameter		Min.	Typ.	Max.	Unit	Remarks
Power Supply Voltage	V_{DD}	3.0	3.3	3.6	V	Note 1
Permissible Input Ripple Voltage	V_{RF}	-10% VDD	-	+10% VDD	V	@ V_{DD} = 3.3V
BIST Control Level	High Level	2.2	-	3.6	V	@ V_{DD} = 3.3V
	Low Level	0	-	0.5	V	
Power Supply Current	I_{DD}	-	151	196	mA	Note 1
Power Supply Inrush Current	Inrush	-	-	1.5	A	Note 2
Power Consumption	P_D	-	0.5	0.65	W	Note 1
	P_{BL}	-	-	4.104	W	-
	P_{total}	-	-	4.754	W	Note 1

Notes :

1.The supply voltage is measured and specified at the interface connector of LCM.
The current draw and power consumption specified is for 3.3V at 25℃.

A)

2.Measure condition(Figure 4)

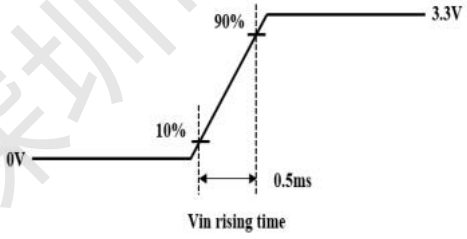


Figure 4. Inrush Measure Condition

3.2 Backlight Unit

< Table 4. LED Driving Guideline Specifications > Ta=25+/-2°C

Parameter			Min.	Typ.	Max.	Unit	Remarks
LED Forward Voltage		V_F	-	-	3.2	V	-
LED Forward Current		I_F	-	20	-	mA	-
LED Power Consumption		P_{LED}	-	4.104	-	W	Note 1
LED Life-Time		N/A	-	-	-	Hour	I_F = 20mA
Power Supply Voltage for LED Driver		V_{LED}	5	12	21	V	-
Power Supply Voltage for LED Driver Inrush		Iled inrush	-	-	1.5	A	Note 4
EN Control Level	Backlight On	V_{BL_EN}	1.5	-	3.6	V	-
	Backlight Off		0	-	0.5	V	-
PWM Control Level	High Level	V_{BL_PWM}	1.5	-	3.6	V	-
	Low Level		0	-	0.5	V	-
PWM Control Frequency		F_{PWM}	200	-	2,000	Hz	-
Duty Ratio			1	-	100	%	Note 3

Notes :

1. Power supply voltage 12V for LED driver.
   Calculator value for reference IF × VF ×66 /driver efficiency = PLED
2. The LED life-time define as the estimated time to 50% degradation of initial luminous.
3. Measure condition (Figure 5)

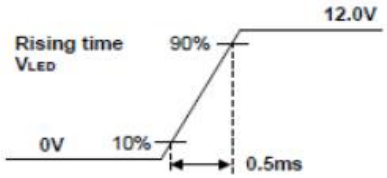


Figure 5. Inrush Measure Condition

3.3 LED Structure

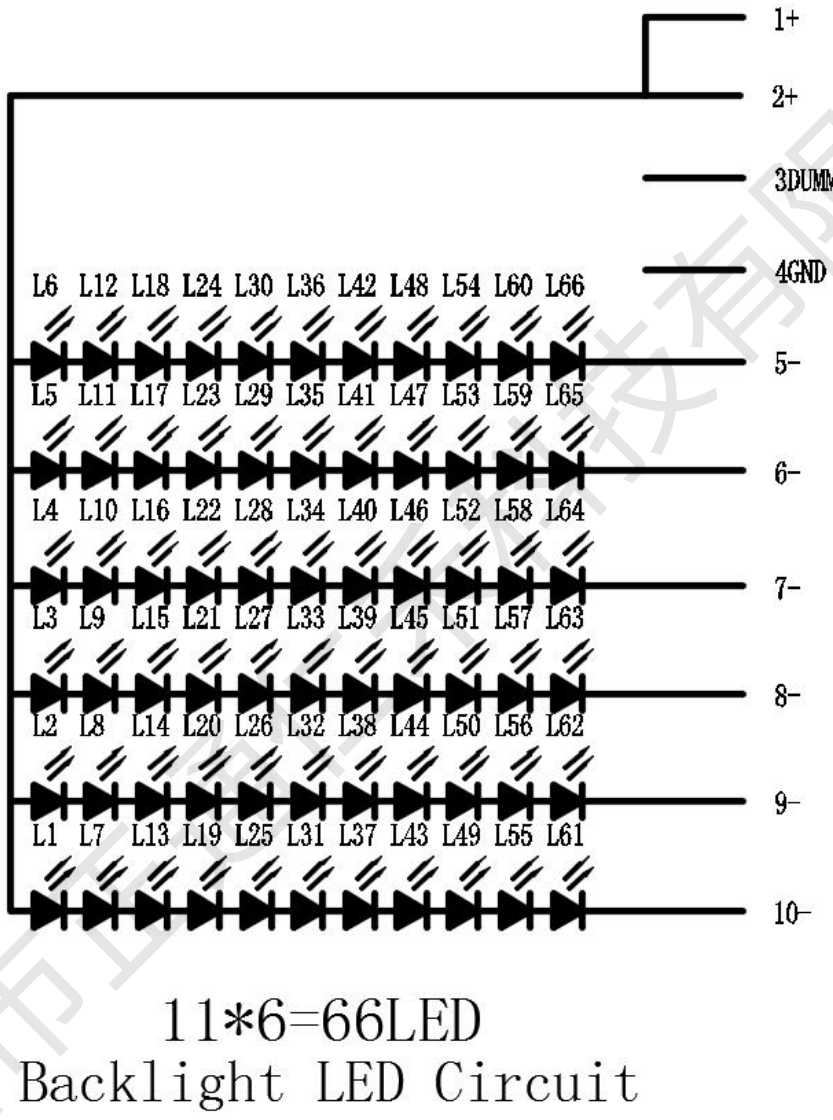


Figure 6. LED Structure

4.0 OPTICAL SPECIFICATION

4.1 Overview

The test of optical specifications shall be measured in a dark room (ambient luminance ≤ 1 lux and temperature = 25±2℃) with the equipment of luminance meter system (CA310) and test unit shall be located at an approximate distance 50cm from the LCD surface at a viewing angle of θ and Φ equal to 0°. We refer to θØ=0 (=θ3) as the 3 o'clock direction (the "right"), θØ=90 (= θ12) as the 12 o'clock direction ("upward"), θØ=180 (= θ9) as the 9 o'clock direction ("left") and θØ=270(= θ6) as the 6 o'clock direction ("bottom"). While scanning θand/or Ø, the center of the measuring spot on the display surface shall stay fixed. The backlight should be operating for 30 minutes prior to measurement. VDD shall be 3.3+/- 0.3V at 25°C. Optimum viewing angle direction is 6 'clock.

4.2 Optical Specifications

<Table 5. Optical Specifications>

Parameter		Symbol	Condition	Min.	Typ.	Max.	Unit	Remark
Viewing Angle Range	Horizontal	Θ_3	CR > 10	85	89	-	Deg.	Note 1
		Θ_9		85	89	-	Deg.	
	Vertical	Θ_{12}		85	89	-	Deg.	
		Θ_6		85	89	-	Deg.	
Luminance Contrast Ratio		CR	Θ = 0°	1000	1200	-		Note 2
Luminance of White(centre)	9 Points	Y_w	Θ = 0° I_{LED} = 20mA	280	300	-	cd/m²	Note 3
White Luminance Uniformity	9 Points	ΔY9		75	80	-	%	Note 4
	13 Points	ΔY13		60.5	-	-	%	
White Chromaticity		W_x	Θ = 0°	0.29	0.33	0.35	-	Note 5
		W_y		0.31	0.34	0.37	-	
Reproduction of Color	Red	R_x	Θ = 0°	Typ.-0.03	0.598	Typ.+0.03	-	-
		R_y			0.349		-	-
	Green	G_x			0.370		-	-
		G_y			0.568		-	-
	Blue	B_x			0.152		-	-
		B_y			0.138		-	-
Color Gamut		-	-	-	45	-	%	-
Response Time (Rising + Falling)		T_{RT}	Ta= 25℃ Θ = 0°	-	20	25	ms	Note 6
Cross Talk		CT	Θ = 0°	-	-	2.0	%	Note 7

Notes :

1. Viewing angle is the angle at which the contrast ratio is greater than 10. The viewing angles are determined for the horizontal or 3, 9 o'clock direction and the vertical or 6, 12 o'clock direction with respect to the optical axis which is normal to the LCD surface (see Figure 7).

2. Contrast measurements shall be made at viewing angle of Θ= 0 and at the center of the LCD surface. Luminance shall be measured with all pixels in the view field set first to white, then to the dark (black) state . (see Figure 7) Luminance Contrast Ratio (CR) is defined mathematically.

$$CR = \frac{\text{Luminance when displaying a white raster}}{\text{Luminance when displaying a black raster}}$$

3. Center Luminance of white is defined as luminance values of 5 point average across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 8 for a total of the measurements per display.

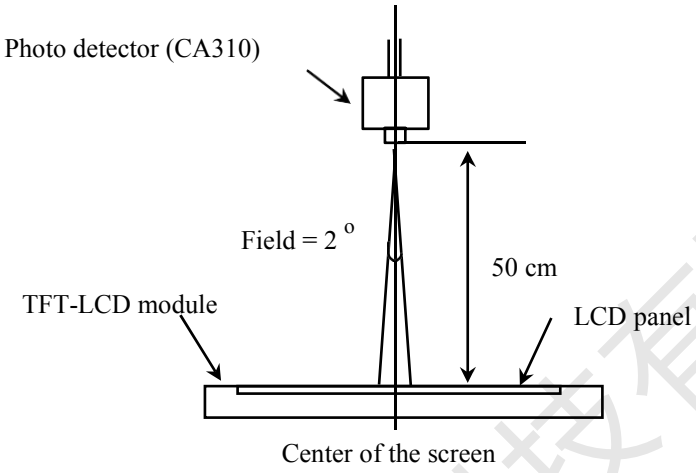
4. The White luminance uniformity on LCD surface is then expressed as : ΔY =Minimum Luminance of 9(or 13) points / Maximum Luminance of 9(or 13) points.(see Figure 8 and Figure 9).

5. The color chromaticity coordinates specified in Table 5 shall be calculated from the spectral data measured with all pixels first in red, green, blue and white. Measurements shall be made at the center of the panel.

6. The electro-optical response time measurements shall be made as Figure 10 by switching the "data" input signal ON and OFF. The times needed for the luminance to change from 10% to 90% is T_f, and 90% to 10% is T_r.

7. Cross-Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 10±1mm diameter area, with all display pixels set to gray 127(of 0 to 255), to the luminance (YB) of that same area when any adjacent area is driven dark.The luminance ratio shall not exceed 1:1.05 (See Figure 11).

4.3 Optical Measurements



Optical characteristics measurement setup

Figure 7. Measurement Set Up

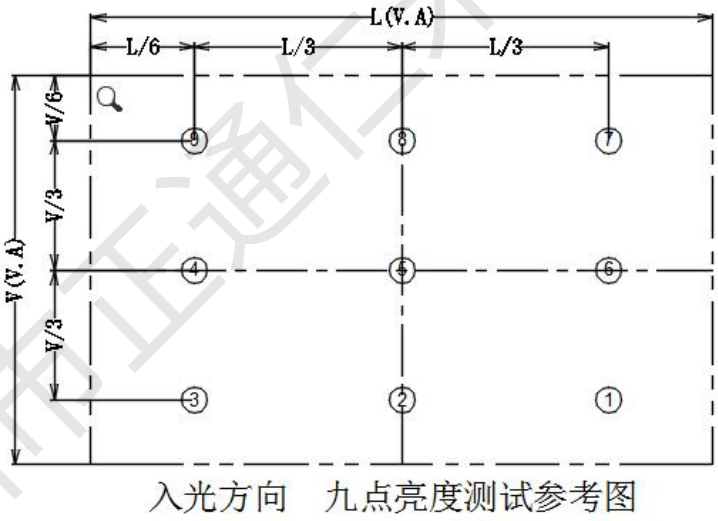


Figure 8. White Luminance and Uniformity Measurement Locations (5 points)

Center Luminance of white is defined as luminance values of center 5 points across the LCD surface. Luminance shall be measured with all pixels in the view field set first to white. This measurement shall be taken at the locations shown in Figure 7 for a total of the measurements per display.

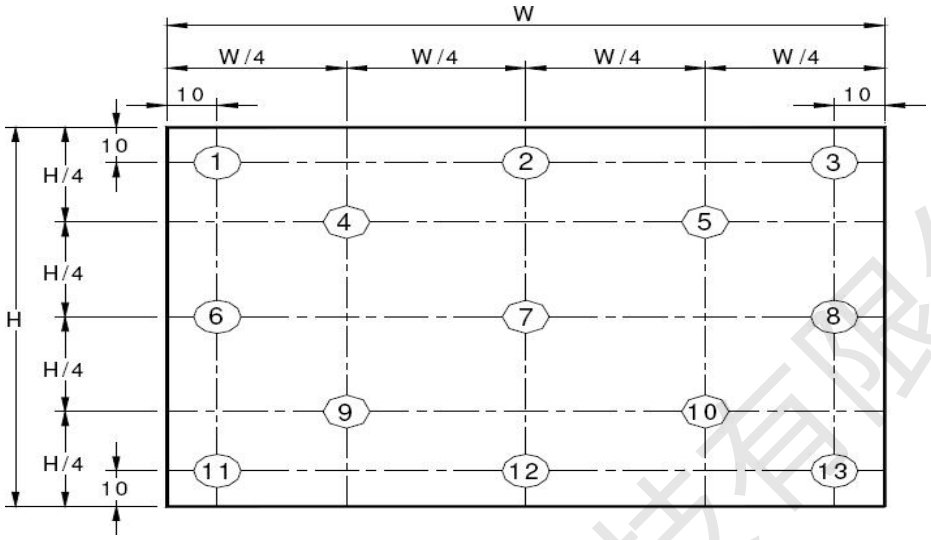


Figure 9. Uniformity Measurement Locations (13 points)

The White luminance uniformity on LCD surface is then expressed as : ΔY5 = Minimum Luminance of five points / Maximum Luminance of five points (see Figure 8) , ΔY13 = Minimum Luminance of 13 points /Maximum Luminance of 13 points (see Figure 9).

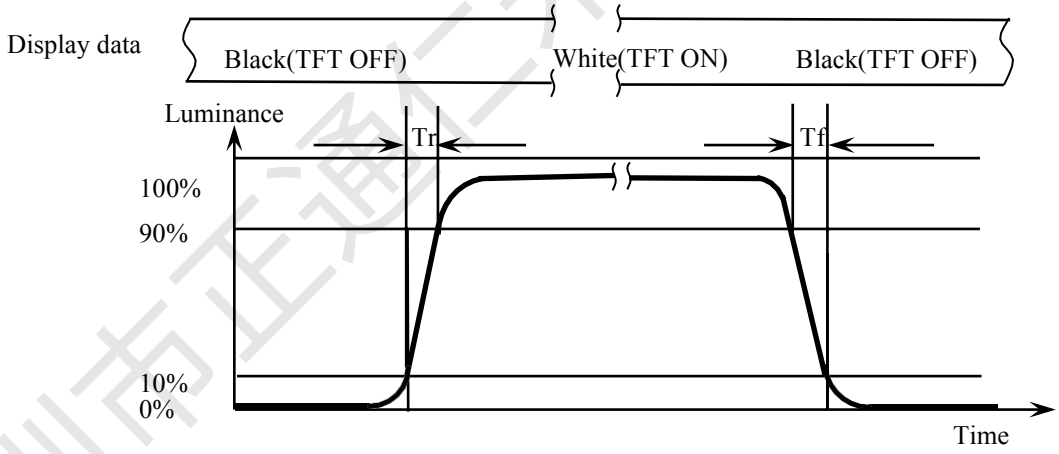
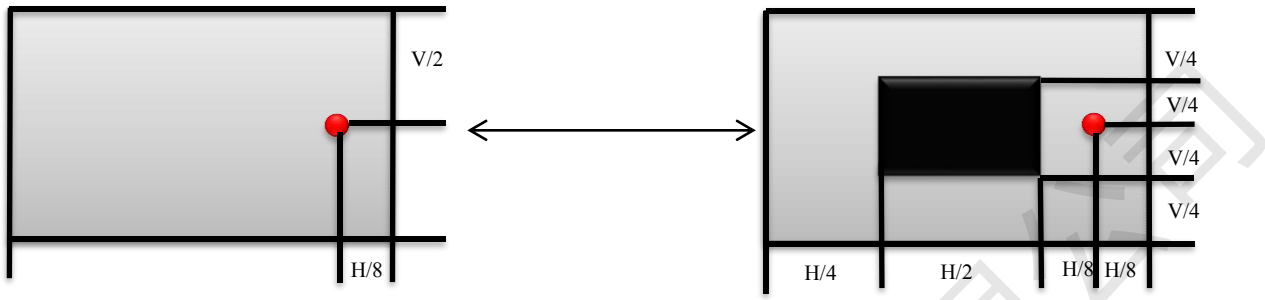


Figure 10. Response Time Testing

The electro-optical response time measurements shall be made as shown in Figure 10 by switching the "data" input signal ON and OFF. Tr: The luminance to change from 10% to 90% ,Tf: The luminance to change from 90% to 10% .

The test system : CA310



$$\text{Cross Talk (\%)} = \left| \frac{Y_B - Y_A}{Y_B} \right| \times 100$$

Figure 11. Cross Talk Modulation Test Description

Where:

Y_A = Initial luminance of measured area (cd/m^2)

Y_B = Subsequent luminance of measured area (cd/m^2)

The location measured will be exactly the same in both patterns. The test background gray is L127.

Cross Talk of one area of the LCD surface by another shall be measured by comparing the luminance (YA) of a 10±1mm diameter area, with all display pixels set to a gray level 127, to the luminance (YB) of that same area when any adjacent area is driven dark.(Refer to Figure 11)
The test system: CA310

5.0 INTERFACE CONNECTION

5.1 Electrical Interface Connection

The electronics interface connector is -. The connector interface pin assignments are listed in Table 6.

<Table 6. Pin Assignments for the Interface Connector>

Pin	Symbol	Description	Note
1	SCL	I2C SCL	
2	H_GND	High Speed Ground	
3	ML1-	Complement Signal-Lane 1	
4	ML1+	True Signal-Main Lane 1	
5	H_GND	High Speed Ground	
6	ML0-	Complement Signal-Lane 0	
7	ML0+	True Signal-Main Lane 0	
8	H_GND	High Speed Ground	
9	AUX+	True Signal-Auxiliary Channel	
10	AUX-	Complement Signal-Auxiliary Channel	
11	H_GND	High Speed Ground	
12	VCCS	Power Supply +3.3V (typical)	
13	VCCS	Power Supply +3.3V (typical)	
14	BIST	Built-In Self Test (active high)	
15	GND	Ground	
16	GND	Ground	
17	HPD	Hot Plug Detect	
18	BL_GND	BL Ground	3.0~3.6V@3.3V(Typ)
19	BL_GND	BL Ground	
20	BL_GND	BL Ground	
21	BL_GND	BL Ground	

22	LED_EN	BL_Enable Signal of LED Converter	
23	LED_PWM	PWM Dimming Control Signal of LED Converter	
24	SDA	I2C SDA	
25	NC	No Connection	
26	LED_VCCS	LED Power Supply	
27	LED_VCCS	LED Power Supply	
28	LED_VCCS	LED Power Supply	
29	LED_VCCS	LED Power Supply	
30	NC	No Connection (Reserve)	
31	#31	BL_GND	
32	#32	BL_Enable	
33	#33	BL_PWM_DIM	
34	#34	NC	
35	#35	NC	
36	#36	BL_PWR	5V~12V@12V（Typ）
37	#37	BL_PWR	
38	#38	BL_PWR	
39	#39	BL_PWR	
40	#40	NC	

5.2 eDP Interface

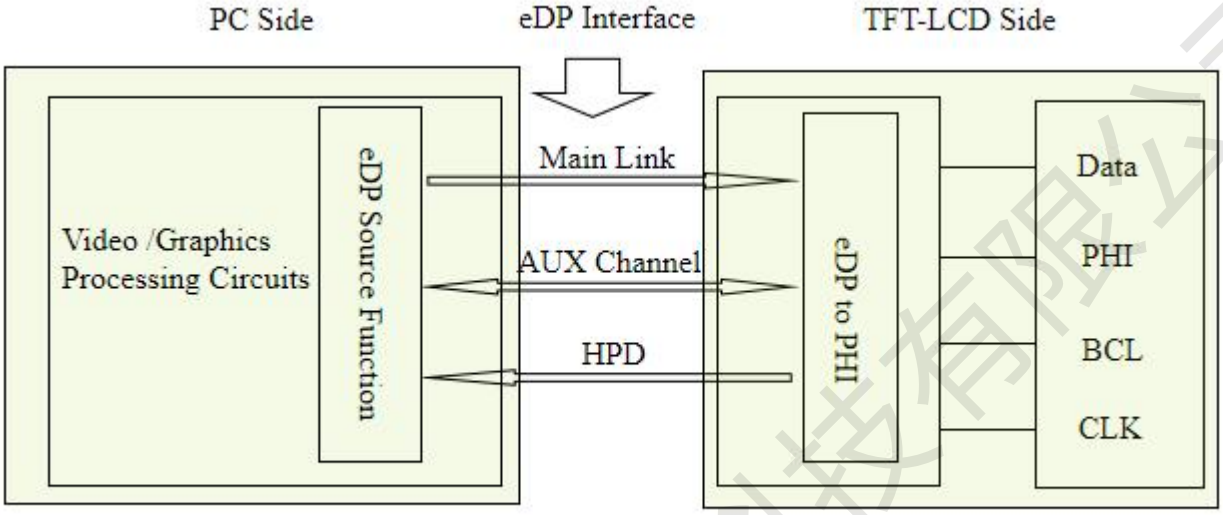


Figure 9. eDP Interface Architecture

5.3 Data Input Format

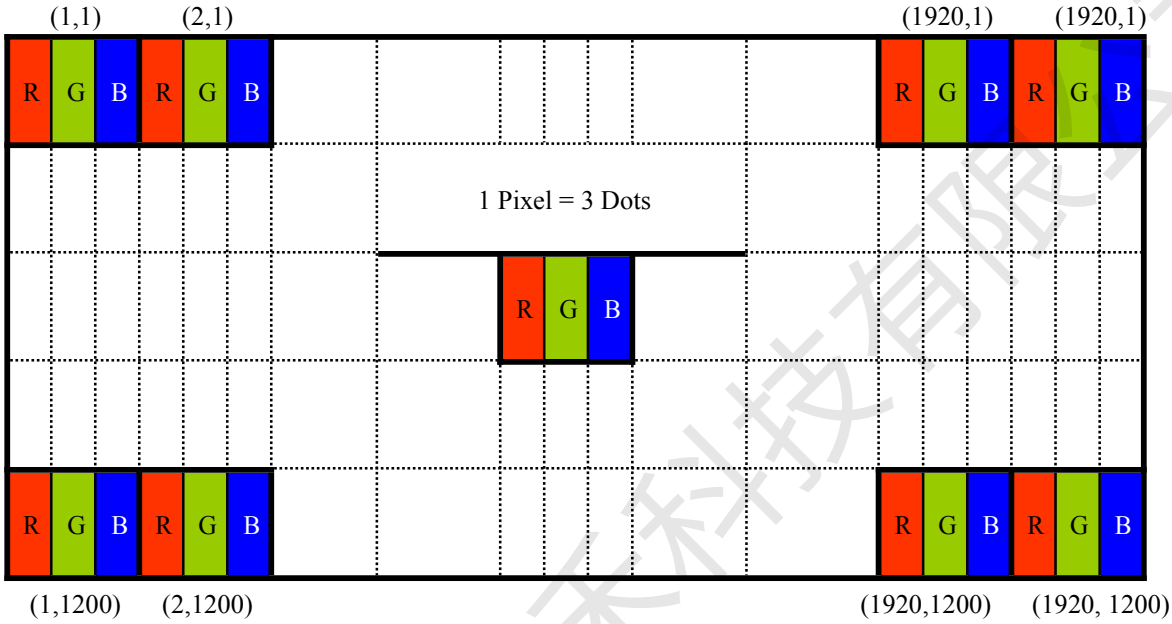
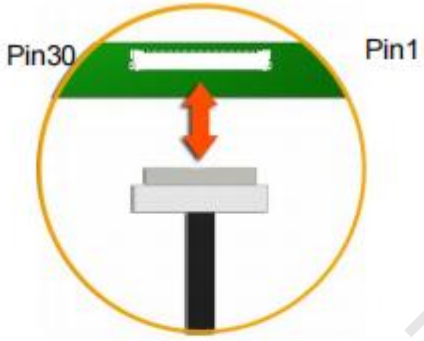


Figure 13. Display Position of Input Data (V-H)

5.4 Back-light & LCM Interface Connection

BLU Interface Connector: STAR CONN300E30-1010RC-G3.



Please refer Appendix Outline Drawing for detail design.

Connector Part No.: **STARCONN300E30-1010RC-G3**

<Table 7. Pin Assignments for the BLU Connector>

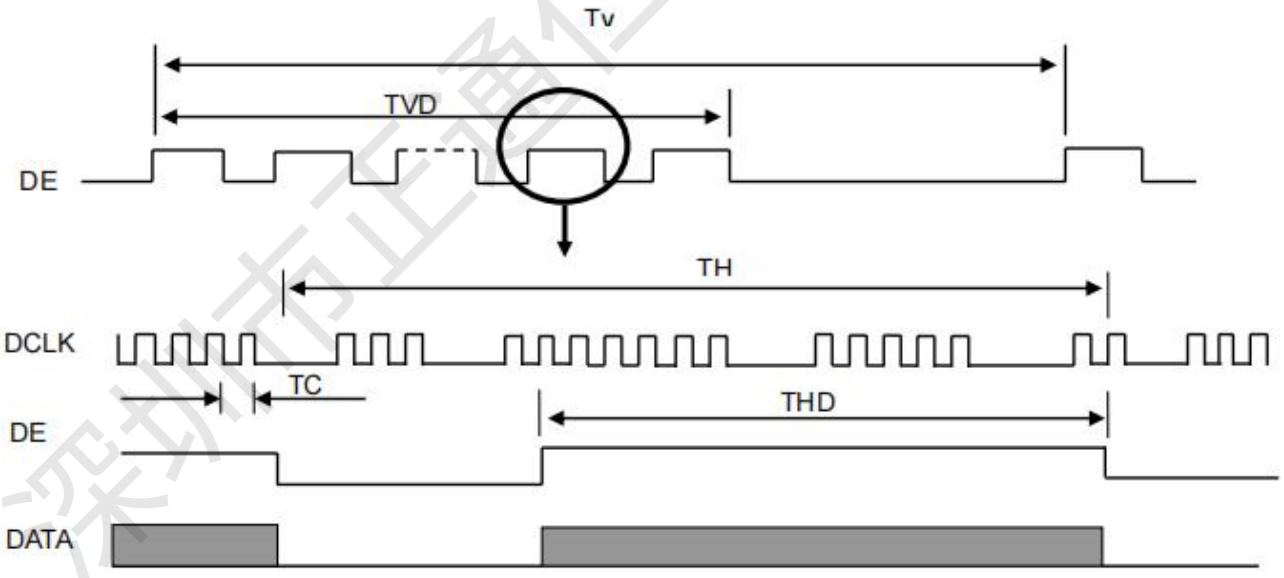
6.0 SIGNAL TIMING SPECIFICATION

6.1 The ZTM160HXXE6601 Is Operated

The input signal timing specification is showed as the following table and timing diagram.

Signal	Item	Symbol	Min.	Typ.	Max.	Unit	Note
DCLK	Frequency	1/Tc	-	158.5	-	MHz	-
DE	Vertical Total Time	TV	-	1246	-	TH	-
	Vertical Active Display Period	TVD	1200	1200	1200	TH	-
	Vertical Active Blanking Period	TVB	-	46	-	TH	-
	Horizontal Total Time	TH	-	2120	-	Tc	-
	Horizontal Active Display Period	THD	1920	1920	1920	Tc	-
	Horizontal Active Blanking Period	THB	-	200	-	Tc	-

Note (1) Display timing signal should be contained and transferred by Display Port Main Link stream data packing described in VESA Display Port Standard V1.4



6.2 eDP Rx Interface Timing Parameter

The specification of the eDP Rx interface timing parameter is shown in Table 10.

<Table 10. eDP Main-Link RX TP4 Package Pin Parameters>

Item	Symbol	Min	Typ	Max	Unit	Remark
Spread spectrum clock (Link clock down-spreading)	SSC	-	-	0.5	%	
Differential peak-to-peak input voltage at package pins	$V_{RX-DIFFp-p}$	120	-	1200	mV	
Rx input DC common mode voltage	$V_{RX\_DC\_CM}$	0	-	2	V	
Differential termination resistance	$R_{RX-DIFF}$	80	-	120	Ω	
Single-ended termination resistance	R_{RX-SE}	40	-	60	Ω	
Rx short circuit current limit	I_{RX_SHORT}	-	-	50	mA	
Intra-pair skew at Rx package pins (HBR) RX intra-pair skew tolerance at HBR	$L_{RX\_SKEW\_INTRA\_PAIR}$	-	-	60	ps	
AC Coupling Capacitor	C_{SOURCE_ML}	75		200	nF	Source side

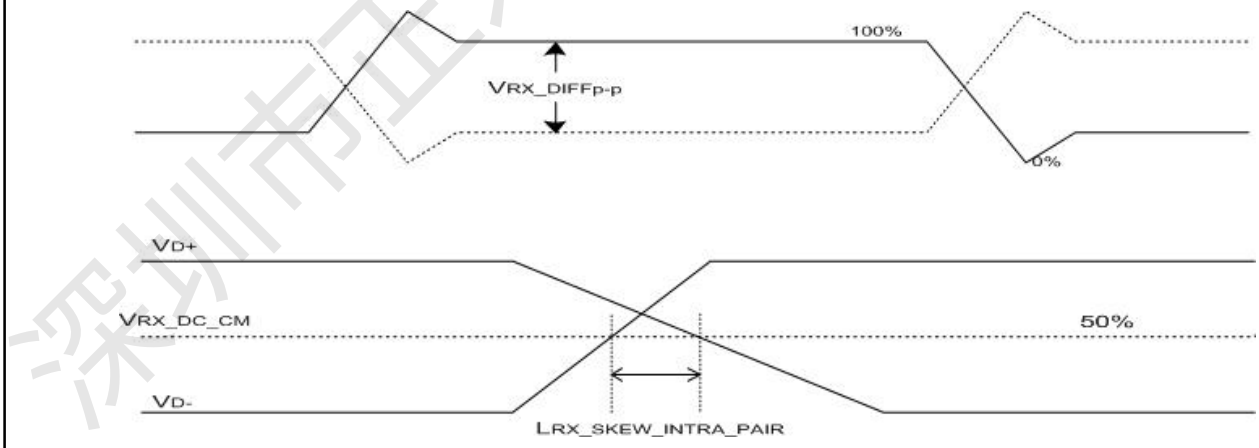


Figure 11. VRX-DIFFp-p & LRX_SKEW_INTRA_PAIR

7.0 INPUT SIGNALS, BASIC DISPLAY COLORS & GRAY SCALE OF COLORS

<Table 12. Input Signal & Basic Display Colors & Gray Scale of Colors >

	Colors & Gray scale	Data signal																			
		R0	R1	R2	R3	R4	R5	R6	R7	G0	G1	G2	G3	G4	G5	G6	G7	B0	B1	B2	B3	B4	B5	B6	B7
Basic colors	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Light Blue	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Purple	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
	Yellow	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
Gray scale of Red	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▿	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Red	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
Gray scale of Green	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	▿	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
	Green	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
Gray scale of Blue	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	1	1	1	1	1
	▿	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1
	Blue	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
Gray scale of White& Black	Black	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
	▵	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
	Darker	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1	0	0	0	0	0	0
	▵	↑								↑								↑							
	▿	↓								↓								↓							
	Brighter	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1
	▿	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1	0	1	1	1	1	1	1	1
	White	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1

8.0 POWER SEQUENCE

To prevent a latch-up or DC operation of the LCD module, the power on/off sequence shall be as shown in below.

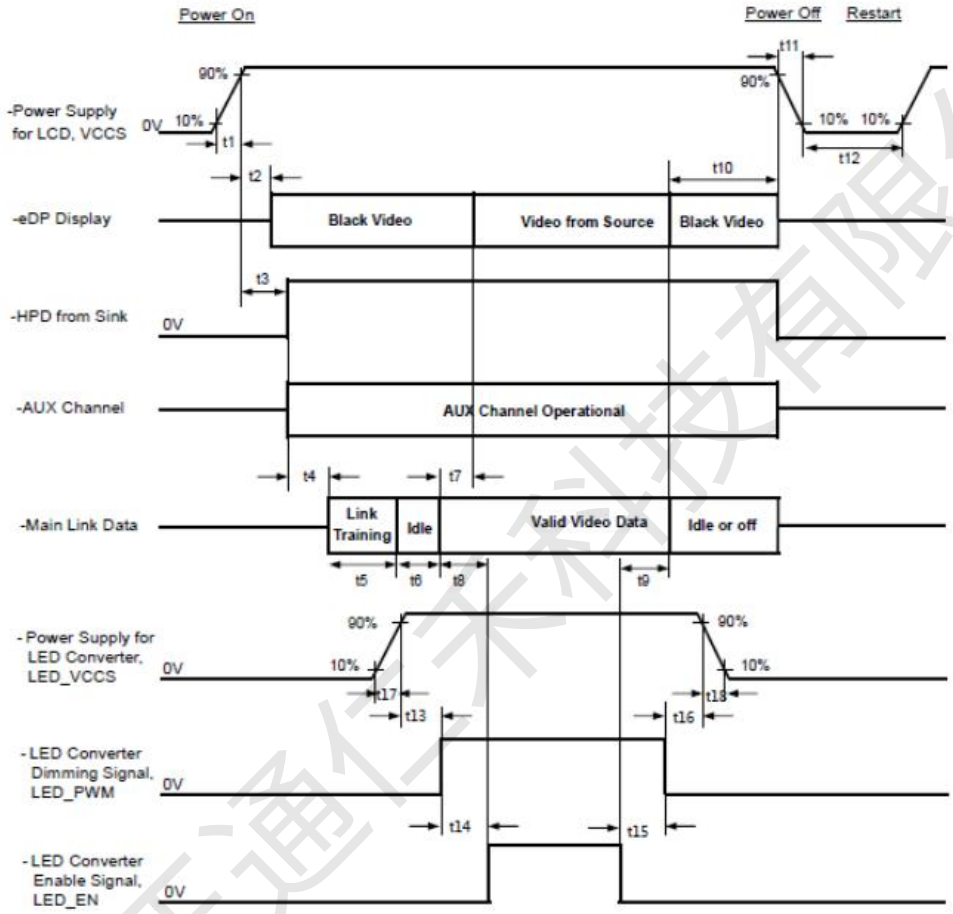


Figure 15. Power Sequence

- 0.5ms ≤ T1 ≤ 10 ms
- 0ms < T2 ≤ 200 ms
- 0ms < T3 ≤ 200 ms
- T3+T4+T5+T6+T8>200ms
- 0ms < T7 ≤ 50ms
- 50ms < T8
- 0ms < T9
- 0ms < T10 < 500 ms
- 1ms ≤ T11 ≤ 10 ms
- 500ms ≤ T12
- 0ms < T13
- 0ms < T14
- 0ms < T15
- 0ms < T16
- 0.5ms ≤ T17
- 0.5ms ≤ T18

Notes:

1. When the power supply VDD is 0V, keep the level of input signals on the low or keep high impedance.
2. Do not keep the interface signal high impedance when power is on. Back Light must be turn on after power for logic and interface signal are valid.

9.0 Connector Description

Physical interface is described as for the connector on LCM.
These connectors are capable of accommodating the following signals and will be following components.

9.1 TFT LCD Module

< Table 14. Signal Connector >

Connector Name /Description	For Signal Connector
Manufacturer	-
Type/ Part Number	-
Mating Housing/ Part Number	-

10.0 MECHANICAL CHARACTERISTICS

10.1 Dimensional Requirements

Figure 23 shows mechanical outlines for the model ZTM160HXXE6601-C2. Other parameters are shown in Table 15.

<Table 15. Dimensional Parameters>

Parameter	Specification	Unit
Active Area	344.6784(H) ×215.424(V)	mm
Number of pixels	1920(H) X 1200 (V) (1 pixel = R + G + B dots)	pixels
Pixel pitch	179.52(H) X59.84(V)	um
Pixel arrangement	RGB Vertical stripe	
Display colors	16.7M(8bit)	
Display mode	Normally black	
Dimensional outline	-	mm
Weight	-(Max)	g

10.2 Anti-Glare and Polarizer Hardness.

The surface of the LCD has an Anti-Glare coating to minimize reflection and to reduce scratching.

10.3 Light Leakage

There shall not be visible light from the back-lighting system around the edges of the screen as seen from a distance 50cm from the screen with an overhead light level of 350 lux.

11.0 RELIABILITY TEST

The reliability test items and its conditions are shown in below.

<Table 13. Reliability Test>

No	Test Items	Conditions	Remark
1	High temperature storage test	Ta = 60°C , 60%RH, 240 hrs	
2	Low temperature storage test	Ta = -20°C , 240 hrs	
3	High temperature & high humidity operation test	Ta = 50°C , 80%RH, 240 hrs	
4	High temperature operation test	Ta = 50°C , 60%RH, 240 hrs	
5	Low temperature operation test	Ta = 0°C , 240 hrs	
6	Thermal shock	Ta = -20 °C ↔ 60 °C (0.5 hr), 60%±3%RH, 100 cycle	
7	Vibration test (non-operating)	Ta = 25°C , 60%RH, 1.5G, 10~500Hz, Sine X,Y,Z / Sweep rate : 1 hour	Note 1
8	Shock test (non-operating)	Ta = 25°C , 60%RH, 220G, Half Sine Wave 2msec±X,±Y,±Z Once for each direction	Note 1
9	Electro-static discharge test (operating)	Air : 150 pF, 330Ω, ±15 KV Contact : 150 pF, 330Ω, ±8 KV Ta = 25°C , 60%RH,	Note 2

Notes :

1. The fixture must be hard enough , so that the module would not be twisted or bent.

2. Self- recovery and restart recovery is allowed. No hardware failures.

12.0 HANDLING & CAUTIONS

(1) Cautions when taking out the module
- Pick the pouch only, when taking out module from a shipping package.

(2) Cautions for handling the module
- As the electrostatic discharges may break the LCD module, handle the LCD module with care. Peel a protection sheet off from the LCD panel surface as slowly as possible.
- As the LCD panel and back - light element are made from fragile glass material, impulse and pressure to the LCD module should be avoided.
- As the surface of the polarizer is very soft and easily scratched, use a soft dry cloth without chemicals for cleaning.
- Do not pull the interface connector in or out while the LCD module is operating.
- Put the module display side down on a flat horizontal plane.
- Handle connectors and cables with care.

(3) Cautions for the operation
- When the module is operating, do not lose CLK, ENAB signals. If any one of these signals is lost, the LCD panel would be damaged.
- Obey the supply voltage sequence. If wrong sequence is applied, the module would be damaged.

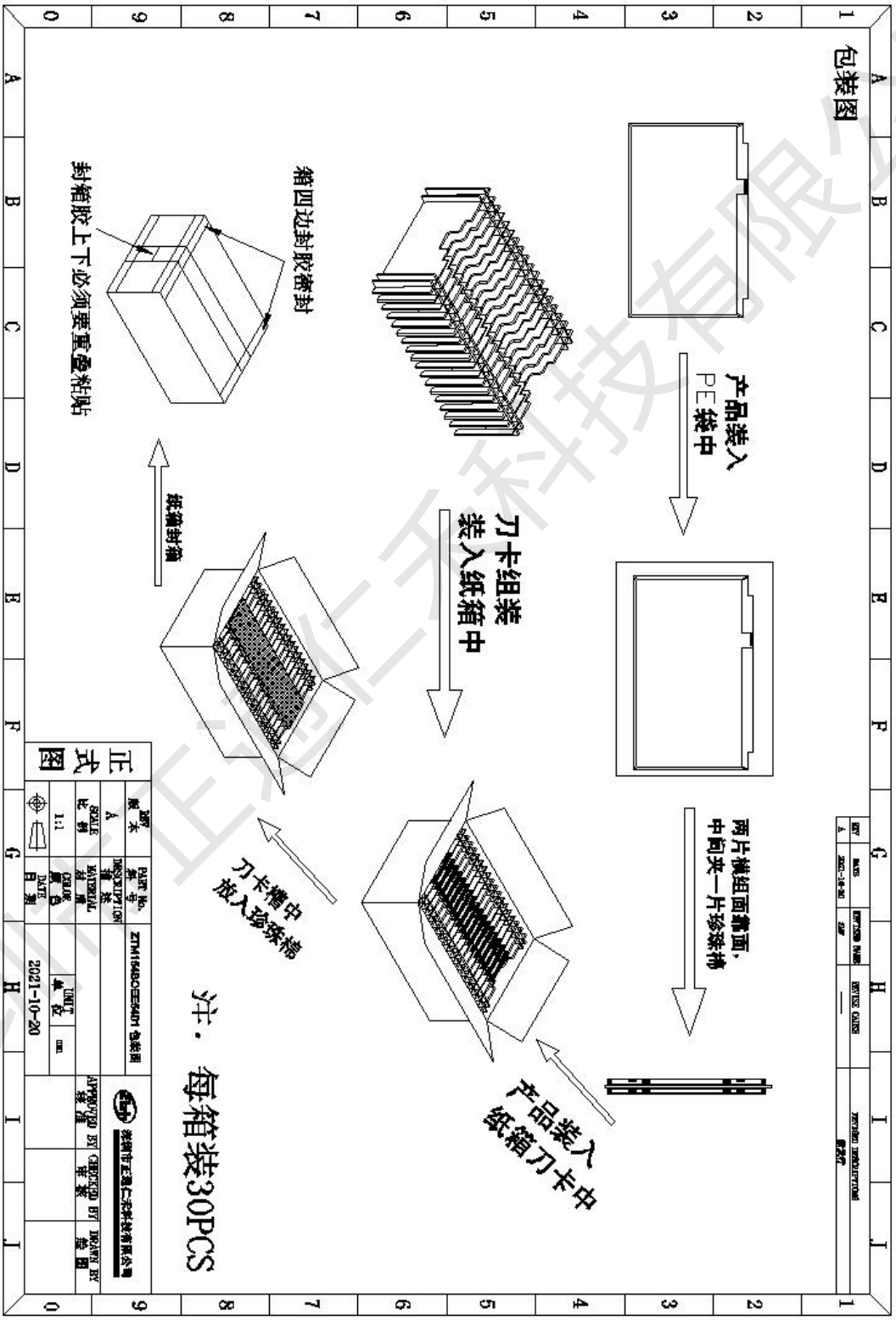
(4) Cautions for the atmosphere
- Dew drop atmosphere should be avoided.
- Do not store and/or operate the LCD module in a high temperature and/or humidity atmosphere. Storage in an electro-conductive polymer packing pouch and under relatively low temperature atmosphere is recommended.

(5) Cautions for the module characteristics
- Do not apply fixed pattern data signal to the LCD module at product aging.
- Applying fixed pattern for a long time may cause image sticking.

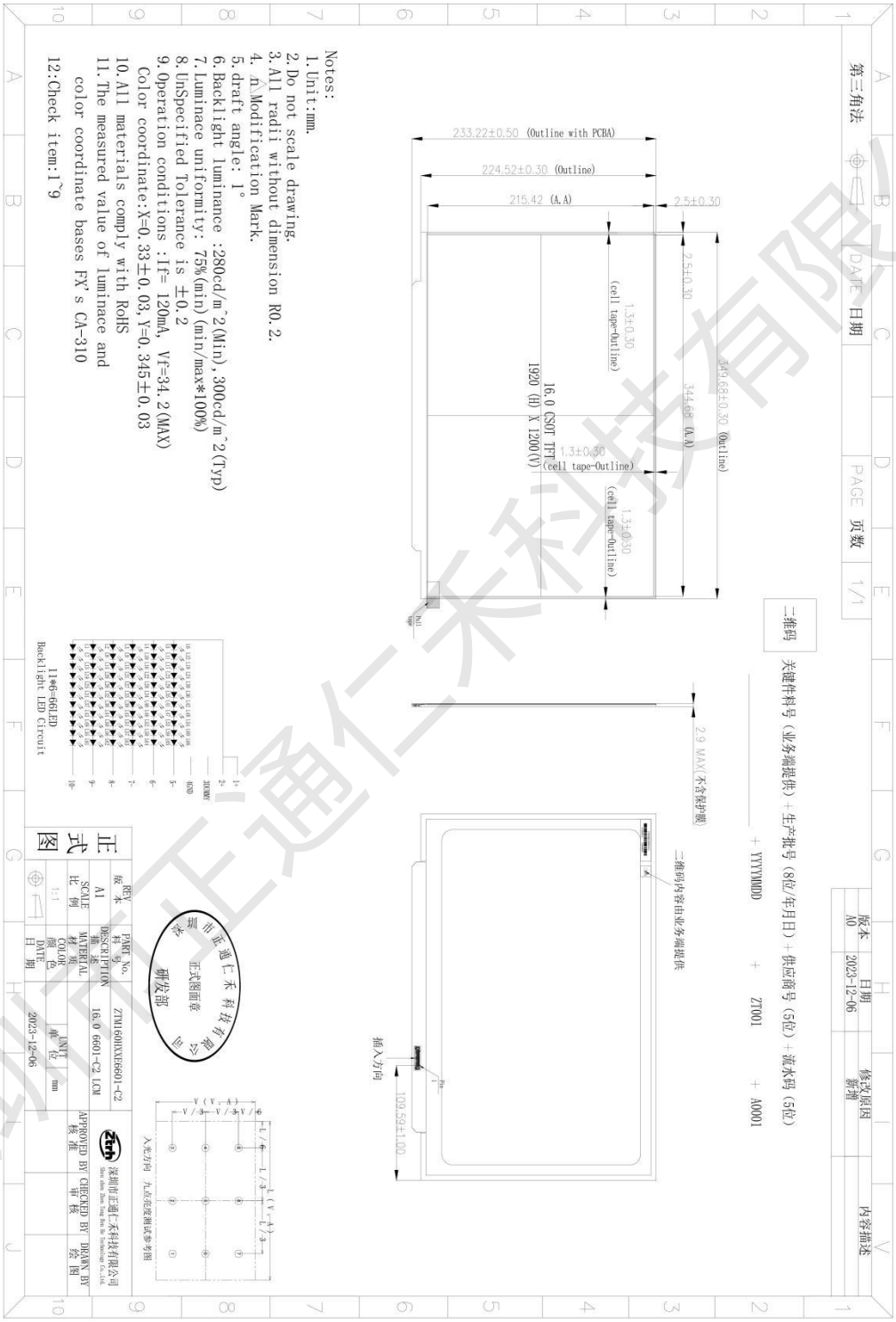
(6) Other cautions
- Do not disassemble and/or re-assemble LCD module.
- Do not re-adjust variable resistor or switch etc.
- When returning the module for repair or etc. Please pack the module not to be broken. We recommend to use the original shipping packages.

13.0 PACKING INGORMATION

13.1 Packing Order



14.0 MECHANICAL OUTLINE DIMENSION



15.0 EDID Table

EDID Table Format					
Address (DEC)	Address (HEX)	Field Name & Comments	Set Value (HEX)	Set Value (BIN)	Set Value (DEC)
0	00	Header	00	00000000	0
1	01	Header	FF	11111111	255
2	02	Header	FF	11111111	255
3	03	Header	FF	11111111	255
4	04	Header	FF	11111111	255
5	05	Header	FF	11111111	255
6	06	Header	FF	11111111	255
7	07	Header	00	00000000	0
8	08	manufacture code	0E	00001110	14
9	09	manufacture code	6F	01101111	111
10	0A	Product Code	2D	00101101	45
11	0B	Product Code	16	00010110	22
12	0C	LCD module Serial No –("0" if not used)	00	00000000	0
13	0D	LCD module Serial No –("0" if not used)	00	00000000	0
14	0E	LCD module Serial No –("0" if not used)	00	00000000	0
15	0F	LCD module Serial No –("0" if not used)	00	00000000	0

16	10	Week of manufacture	2E	00101110	46
17	11	Year of manufacture	20	00100000	32
18	12	EDID Structure Ver # = 1	01	00000001	1
19	13	EDID revision # = 4	04	00000100	4
20	14	Video I/P definition = Digital I/P (80h)	A5	10100101	165
21	15	Max H image size = (Rounded to cm)	23	00100011	35
22	16	Max V image size = (Rounded to cm)	16	00010110	22
23	17	Display Gamma	78	01111000	120
24	18	Feature support (no DPMS, Active off, no RGB, timing BLK 1)	03	00000011	3
25	19	Red/Green Low bits (RxRy/GxGy)	27	00100111	39
26	1A	Blue/White Low bits (BxBy/WxWy)	15	00010101	21
27	1B	Red X Rx	95	10010101	149
28	1C	Red Y Ry	5B	01011011	91
29	1D	Green X Gx	5A	01011010	90
30	1E	Green Y Gy	93	10010011	147
31	1F	Blue X Bx	29	00101001	41
32	20	Blue Y By	20	00100000	32
33	21	White X Wx	50	01010000	80
34	22	White Y Wy	54	01010100	84
35	23	Established timings 1 (00h if not used)	00	00000000	0
36	24	Established timing 2 (00h if not used)	00	00000000	0

37	25	Manufacturer's timings (00h if not used)	00	00000000	0
38	26	Standard timing ID1 (01h if not used)	01	00000001	1
39	27	Standard timing ID1 (01h if not used)	01	00000001	1
40	28	Standard timing ID2 (01h if not used)	01	00000001	1
41	29	Standard timing ID2 (01h if not used)	01	00000001	1
42	2A	Standard timing ID3 (01h if not used)	01	00000001	1
43	2B	Standard timing ID3 (01h if not used)	01	00000001	1
44	2C	Standard timing ID4 (01h if not used)	01	00000001	1
45	2D	Standard timing ID4 (01h if not used)	01	00000001	1
46	2E	Standard timing ID5 (01h if not used)	01	00000001	1
47	2F	Standard timing ID5 (01h if not used)	01	00000001	1
48	30	Standard timing ID6 (01h if not used)	01	00000001	1
49	31	Standard timing ID6 (01h if not used)	01	00000001	1
50	32	Standard timing ID7 (01h if not used)	01	00000001	1
51	33	Standard timing ID7 (01h if not used)	01	00000001	1
52	34	Standard timing ID8 (01h if not used)	01	00000001	1
53	35	Standard timing ID8 (01h if not used)	01	00000001	1
54	36	Pixel Clock LSB	EA	11101010	234

55	37	Pixel Clock HSB	3D	00111101	61
56	38	Horizontal Active (lower 8 bits)	80	10000000	128
57	39	Hor blanking (lower 8 bits)	C8	11001000	200
58	3A	Horizontal Active/Horizontal blanking (upper4:4 bits)	70	01110000	112
59	3B	Vertcal active(lower 8 bits)	B0	10110000	176
60	3C	Vertical blanking(lower 8 bits)	2E	00101110	46
61	3D	Vertical Active : Vertical Blanking (upper4:4 bits)	40	01000000	64
62	3E	Horizontal Sync Offset	30	00110000	48
63	3F	Horizontal Sync Pulse Width	20	00100000	32
64	40	Vertical Sync Offset , Sync Width	36	00110110	54
65	41	Horizontal Vertical Sync Offset/Width upper 2 bits	00	00000000	0
66	42	Horizontal Image Size	59	01011001	89
67	43	Vertical image Size	D7	11010111	215
68	44	Horizontal Image Size / Vertical image size	10	00010000	16
69	45	Horizontal Border = (0 for Notebook LCD)	00	00000000	0
70	46	Vertical Border = (0 for Notebook LCD)	00	00000000	0
71	47	Non-interlaced, Normal, no stereo, Separate sync, H/V pol Negatives,	1A	00011010	26
72	48	Detailed timing descriptor # 2 / Monitor Descriptor # 2	00	00000000	0
73	49	Flag (byte 2)	00	00000000	0
74	4A	Reserved	00	00000000	0
75	4B	Monitor Descriptor # 2	FD	11111101	253
76	4C	Vertical Rate Offsets are zero.	00	00000000	0
77	4D	Defines Minimum Vertical Rate	30	00110000	48
78	4E	Defines Maximum Vertical Rate	3C	00111100	60